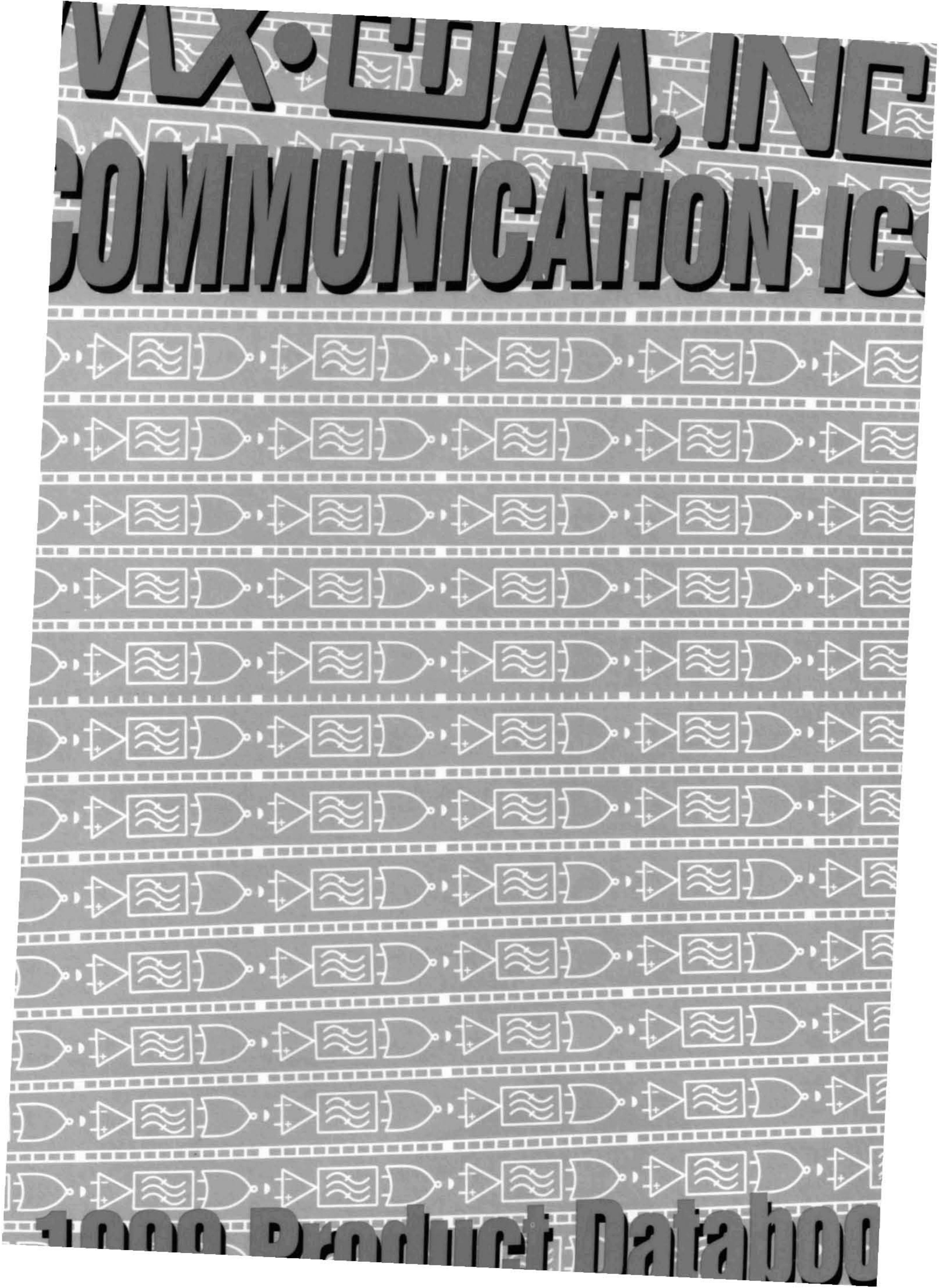

MX·COM, INC

COMMUNICATION ICS

1[illegible] Product Databoo

MX•COM, INC.
COMMUNICATION ICs

1999 PRODUCT DATABOOK

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INTRODUCTION 2
DATA BULLETINS 3
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GLOSSARY 6
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ORDERING INFORMATION

TO PLACE AN ORDER:

Contact the MX-COM Customer Service Department.

MX-COM, Inc.
4800 Bethania Station Rd.
Winston-Salem, NC 27105-1201
USA

Phone: (336) 744-5050 OR (800) 638-5577 (Toll-Free in the Continental U.S., Alaska and Canada)

Fax (336) 744-5054.

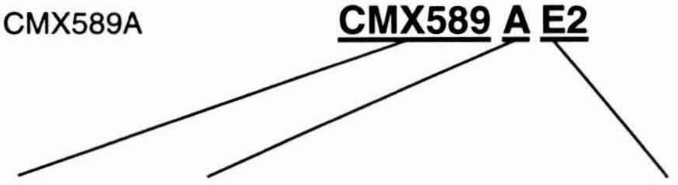
e-mail: mxsales@mxcom.com

The phones are staffed from 8AM to 5PM E.S.T., Monday through Friday.

Please specify the device package type when placing an order. Package type suffix codes are defined below. See the last section of the data book for package dimensions.

Package Description

Example: CMX589A



Device	**Major Revision Level**
CMX589	(A, B, C,...)

Package Style

E2	TSSOP	Thin Shrink Small Outline Package

(Please refer to the device data bulletin for specific package style when ordering.)

SECOND SOURCE:

A qualified second source for MX-COM integrated circuits is CML, the affiliate. Top marks on CML and MX-COM products are the same with the following exceptions:

1. Where MX-COM products bear the MX-COM logo, CML products bear the CML logo.
2. Where MX-COM products bear the "CMX" prefix, CML products also bear the "CMX" prefix and both the MX-COM and CML products have the same performance specifications.
3. Where MX-COM products bear an "MX" prefix, CML's products bear an "FX" prefix. For example, an MX-COM MX909A device may be second sourced by a CML FX909A.
4. MX-COM and CML products may not have identical pin-outs or package styles. Call the factory for more information
5. Some MX-COM and CML's package styles have different package designator suffixes. For a complete reference list refer to Appendix: Package Description.
6. In some rare instances, the device designator may differ between MX-COM and CML equivalent products. Please contact MX-COM to confirm the device designator for a second source part number.

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8-PSK
- MX980

ADC
- See **Analog-to-Digital Converter**

ALARM / SECURITY MONITORING
- See **Modems**
- See **Tone Signaling and Detection**
- **Other:**
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  - CMX018 UHF FM/FSK Receiver

AMPLIFIERS
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ANALOG-TO-DIGITAL CONVERTER
- MX839, MX980

ATTENUATION
- MX029, MX818, MX828, MX839, MX980

AUDIO PROCESSORS
- **Modems/Data:**
  - MX829
- **Telecom Call Progress / Pulse Metering:**
  - CMX605, MX633, MX643, MX663
- **Tone Signaling and Detection:**
  - MX102, MX818, MX828
- **Voice Scrambling:**
  - MX014, MX128
- **Other:**
  - MX019 Quad Digitally Controlled Amplifier
  - MX029 Dual Digitally Controlled Amplifier
  - MX839 Analog I/O Processor

AUTOCORRELATOR
- MX102

BELL 202
- CMX602A, CMX624, MX614

BELL 212A
- CMX644

BINARY PSK
- See **BPSK**

BPSK
- MX980

CALL PROGRESS
- CMX605, CMX644, CMX673, MX633, MX643, MX663

CALLER ID
- CMX602A, CMX605, CMX624, CMX654, MX604, MX614

CALLER ID ON CALL WAITING
- See **Caller ID**

CDPD
- CMX589A, MX019

CODECS
- MX609, MX619, MX629, MX802

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR
- MX609, MX619, MX629, MX802

CORDLESS TELEPHONE
- See **Caller ID**
- See **Modems**
- See **Tone Signaling and Detection**
- **Voice Coding:**
  - MX609, MX619, MX629
- **Voice Scrambling:**
  - MX128
- **Other:**
  - CMX017 UHF FM/FSK Transmitter
  - CMX018 UHF FM/FSK Receiver

CTCSS
- See **Tone Signaling and Detection**

CVSD CODECS
- See **Continuously Variable Slope Delta Modulator**

DAC
- See **Digital-to-Analog Converter**

DATA RADIO
- See **Digital Radio**

DATA TAC™
- MX929B

DCS
- See **Digitally Controlled Squelch**

DELTA MODULATION CODECS
- See **Continuously Variable Slope Delta Modulator**

DIRECT SEQUENCE SPREAD SPECTRUM
- See **Spread Spectrum**

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  - CMX018 UHF FM/FSK Receiver
  - MX019 Quad Digitally Controlled Amplifier
  - MX029 Dual Digitally Controlled Amplifier
  - MX839 Analog I/O Processor

DIGITAL-TO-ANALOG CONVERTER
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- MX019, MX029

DIGITALLY CONTROLLED SQUELCH
- MX805A, MX828

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DTMF DECODER
CMX605
See also **Tone Signaling and Detection**

DTMF ENCODER
CMX605, CMX624, CMX644, MX803A, MX829
See also **Tone Signaling and Detection**

FAMILY RADIO SERVICE
See **Digitally Controlled Squelch**
See **Tone Signaling and Detection, CTCSS**

FFSK
CMX469A, MX429A, MX469, MX809, MX829

FHSS
See **Spread Spectrum**

FM DISCRIMINATOR
CMX018

FM RECEIVER
CMX018

FM TRANSMITTER
CMX017

FREQUENCY HOPPING SPREAD SPECTRUM
See **Spread Spectrum**

FREQUENCY INVERSION SCRAMBLING
MX014, MX128, MX214, MX224, MX375

FRS, Family Radio Service
See **Digitally Controlled Squelch**
See **Tone Signaling and Detection, CTCSS**

FSK
CMX602A, CMX624, MX604, MX614, MX624
Other:
CMX017 UHF FM/FSK Transmitter
CMX018 UHF FM/FSK Receiver

GAIN
MX019, MX029, MX806A, MX828, MX828, MX829

GMSK
CMX589A, MX909A

HART®
CMX602A, CMX605, CMX624, MX614

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See **Tone Signaling and Detection**
Voice Coding:
MX609, MX619, MX629
Voice Scrambling:
MX014, MX128, MX214, MX224, MX375
Other:
MX019 Quad Digitally Controlled Amplifier
MX029 Dual Digitally Controlled Amplifier
MX806A Audio Processor
MX839 Analog I/O Processor

LMR
See **Land Mobile Radio**

LNA
See **Low Noise Amplifier**

LOW NOISE AMPLIFIER
CMX018

MILITARY CODECS
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MOBITEX™
CMX589A, MX909A

MODEM
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MX919B, MX929B
8-PSK:
MX980
Binary PSK, BPSK:
MX980
FFSK:
CMX469A, MX429A, MX469, MX809, MX829
FSK:
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GMSK:
CMX589A, MX909A
MSK:
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pi/4 DQPSK:
MX980
PSK:
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MPT 1306
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MX429A, MX829

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CMX017, CMX018

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pi/4 DQPSK
MX980

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PMR
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CMX018 UHF FM/FSK Receiver
MX019 Quad Digitally Controlled Amplifier
MX029 Dual Digitally Controlled Amplifier

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Modems/Data:
CMX602A, CMX624, CMX644, CMX654, MX604, MX614
Telecom Call Progress / Pulse Metering:
CMX605, CMX673, MX633, MX643, MX663

PRIVATE MOBILE RADIO
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PROGRAMMABLE GAIN AMPLIFIER
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PSK
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PUBLIC ACCESS MOBILE RADIO
See **Land Mobile Radio**

PULSE METERING DETECTION
CMX631A, MX641, MX651

QUADRATURE DEMODULATOR
CMX018

QUADRATURE INTERFACE
MX980

RD-LAP™
MX929B

RF MIXER
CMX017, CMX018

RF MODULATOR
CMX017

SCADA
See **Modem**

SELECTIVE CALLING
See **Digitally Controlled Squelch**
See **Tone Signaling and Detection**

SEQUENTIAL TONE ENCODER/DECODER
MX102, MX803A

SPEECH CODEC
See **CVSD CODECS**

SPM
See **Pulse Metering Detection**

SPREAD SPECTRUM
CMX017, CMX018, CMX589A

SUB-AUDIO TONE SIGNALING AND DETECTION
See **Digitally Controlled Squelch**
See **Tone Signaling and Detection, CTCSS**

SUBSCRIBER PULSE METERING
See **Pulse Metering Detection**

TELEMETRY
See **Modem**
Other:
CMX017 UHF FM/FSK Transmitter
CMX018 UHF FM/FSK Receiver

TELECOM
See **Telephony**

TELEPHONY
See **Caller ID**
See **Call Progress**
See **Pulse Metering Detection**
Other:
CMX017 UHF FM/FSK Transmitter
CMX018 UHF FM/FSK Receiver

TETRA
MX839, MX980

TIME DOMAIN SCRAMBLERS
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See **Tone Signaling and Detection**

TONE DETECTOR
See **Tone Signaling and Detection**

TONE ENCODER
See **Tone Signaling and Detection**

TONE SIGNALING AND DETECTION
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MX165C, MX315A, MX375, MX465, MX805A, MX818, MX828,
DTMF:
CMX605, CMX624, CMX644, MX803A, MX829
SelCall:
MX803A, MX828
Other:
MX102 Autocorrelator
MX105A Tunable Tone Detector

TRUNKED RADIO
Modems/Data:
CMX469A, MX429A, MX469, MX809, MX829
Tone Signaling and Detection:
MX102, MX165C, MX465, MX803A, MX805A, MX809, MX818, MX828, MX829

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V.22
CMX644

V.23
  CMX624, CMX654, MX604

VCO
  See **Voltage Controlled Oscillator**

VOICE SCRAMBLING
  Frequency Inversion and Variable Split Band:
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  Time Domain:
    MX609, MX619, MX629, MX802

VOLTAGE CONTROLLED OSCILLATOR
  CMX017

WIDEBAND FM
  CMX017, CMX018

WIRELESS DATA
  See Modem
  Other:
    CMX017 UHF FM/FSK Transmitter
    CMX018 UHF FM/FSK Receiver

WIRELESS INTERCOM
  See **Modem**
  See **Tone Signaling and Detection**
  See **Voice Scrambling**
  Other:
    CMX017 UHF FM/FSK Transmitter
    CMX018 UHF FM/FSK Receiver

WIRELESS LOCAL LOOP
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  See **Call Progress**
  See **Modem**
  See **POTS Interface**
  See **Pulse Metering Detection**
  Other:
    CMX017 UHF FM/FSK Transmitter
    CMX018 UHF FM/FSK Receiver

WIRELESS MODEMS
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  Other:
    CMX017 UHF FM/FSK Transmitter
    CMX018 UHF FM/FSK Receiver

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SPECIAL ORDER AND REPLACEMENT DEVICES

The integrated circuits and evaluation kits listed in the Special Order column have been replaced by the device listed in the Recommended Replacement Column or are available through special order.

Special Order	Recommended Replacement
DB600	EV6000 μController Companion Board for the EV6040
DB602	EV6021 Evaluation Kit for the CMX602A
DB604	EV6040 Evaluation Kit for the MX604 and MX614
DB800	EV8000 Evaluation Kit for the MX818, MX828, and MX829
DB900	EV9000 Evaluation Kit for the MX909A, MX919B, and MX929B
DBS800	N/A
MX003	MX803A Audio Signaling Processor
MX004	MX014 Half-Duplex Voice Band Frequency Inversion Scrambler
MX009	MX019 Quad Digitally Controlled Amplifier MX029 Dual Digitally Controlled Amplifier
MX013	MX803A Audio Signaling Processor
MX105	MX105A Tunable tone Detector
MX109	MX609 PCN / PCS Delta modulation CODEC
MX118	MX128 Full-Duplex Cordless Phone Voice Band Frequency Inversion Scrambler
MX165B	MX165C CTCSS Encoder / Deocder with Tx / Rx Filters
MX203	MX803A Audio Signaling Processor MX829 Baseband Signaling Processor
MX205	MX805A Sub-Audio Signaling Processor
MX275	MX375 CTCSS Encoder / Decoder with *Pvt*SQUELCH™
MX316	N/A
MX335	MX165C CTCSS Encoder / Deocder with Tx / Rx Filters MX465 CTCSS Encoder / Deocder with Tx / Rx Filters MX818 CTCSS Signaling Processor MX828 CTCSS / DCS / SelCall Signaling Processor
MX336	N/A
MX346	N/A
MX355	MX165C CTCSS Encoder / Deocder with Tx / Rx Filters MX465 CTCSS Encoder / Deocder with Tx / Rx Filters MX818 CTCSS Signaling Processor MX828 CTCSS / DCS / SelCall Signaling Processor
MX365	MX165C CTCSS Encoder / Deocder with Tx / Rx Filters MX465 CTCSS Encoder / Deocder with Tx / Rx Filters MX818 CTCSS Signaling Processor MX828 CTCSS / DCS / SelCall Signaling Processor
MX386	MX826 AMPS / NAMPS System Audio Processor
MX409	CMX469A 1200 / 2400 /4800bps MSK Modem with Serial Control MX469 1200 / 2400 /4800bps MSK Modem with Serial Control
MX419	CMX469A 1200 / 2400 /4800bps MSK Modem with Serial Control MX469 1200 / 2400 /4800bps MSK Modem with Serial Control
MX429	MX429A 1200 / 2400bps MSK Modem with Parallel Control MX829 Baseband Signaling Processor with MSK Modem, DTMF Encoder, and Level Controls for Trunked Radio Control
MX439	CMX469A 1200 / 2400 /4800bps MSK Modem with Serial Control MX469 1200 / 2400 /4800bps MSK Modem with Serial Control
MX489	CMX589A 4k to 200kbps High Speed GMSK Modem
MX503	MX803A Audio Signaling Processor
MX506	MX806A Audio Processor
MX589	CMX589A 4k to 200kbps High Speed GMSK Modem
MX611	CMX631A Low Voltage Subscriber Pulse Metering (SPM) Detector

Special Order	**Recommended Replacement**
	MX641 Dual Channel Subscriber Pulse Metering (SPM) Detector
MX621	CMX631A Low Voltage Subscriber Pulse Metering (SPM) Detector MX641 Dual Channel Subscriber Pulse Metering (SPM) Detector
MX623	MX663 Call Progress Tone detector CMX673 Call Progress Decoder
MX631	CMX631A Low Voltage Subscriber Pulse Metering (SPM) Detector MX641 Dual Channel Subscriber Pulse Metering (SPM) Detector
MX709	MX802 Digital Voice Storage and Retrieval CODEC
MX812	MX802 Digital Voice Storage and Retrieval CODEC
MX816	MX826 AMPS / NAMPS System Audio Processor
MX836	N/A
MX909	MX909A GMSK Modem Data Pump (Mobitex^{TM})
MX919	MX919B 4-Level FSK Modem Data Pump (General Purpose)
MX919A	MX919B 4-Level FSK Modem Data Pump (General Purpose)
MX929	MX929B 4-Level FSK Modem Data Pump (RD-LAP^{TM})
MX929A	MX929B 4-Level FSK Modem Data Pump (RD-LAP^{TM})
MX939	CMX589A 4k to 200kbps High Speed GMSK Modem
MX949	CMX589A 4k to 200kbps High Speed GMSK Modem

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INTRODUCTION

Introduction

This data book presents technical specifications and application notes for MX-COM's integrated circuits. Its purpose is to help customers select and apply our products and learn about how we delivery high quality service and products.

Contact Us

You can gather the latest information and contact us using our Internet web site, http://www.mxcom.com, or any of the following methods:

Internet web site	http://www.mxcom.com
Internet email	mxsales@mxcom.com
Telephone	336-744-5050
Telephone, U.S. only	800-638-5577
FAX	336-744-5054
Postal address	MX-COM, Inc. 4800 Bethania Station Rd. Winston-Salem, NC 27105 U.S.

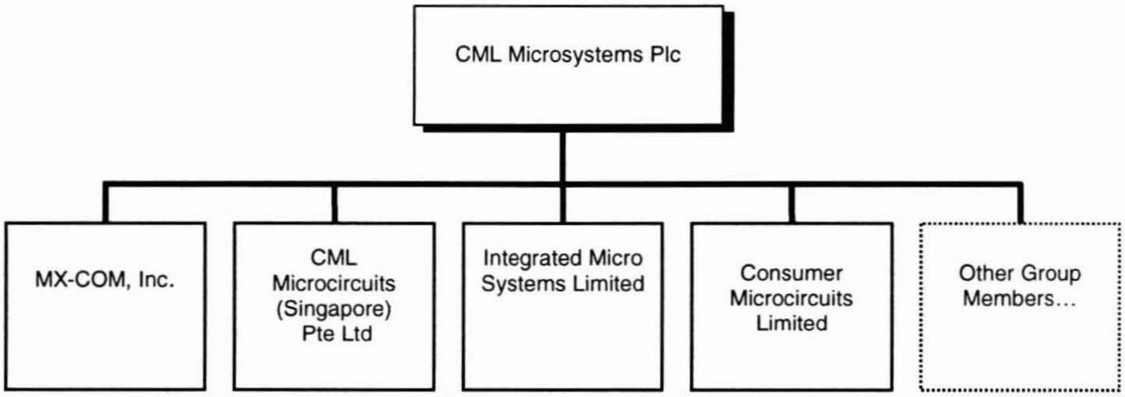
Company Profile

MX-COM, Inc. designs and manufactures integrated circuits, modules, and systems for the communication industries. With core competencies in IC design, manufacturing and customer service we serve a variety of commercial, consumer and industrial markets in both domestic and international territories.

MX-COM is a semiconductor manufacturer with complete sales, marketing, engineering, planning, and manufacturing functions operating according to certified ISO9002 quality procedures.

Conducting business since 1980, MX-COM is a subsidiary of CML Microsystems Plc, a group of technology source companies publicly traded on the London Stock Exchange. Our standard and specialized products are tailored with strong customer participation to meet market needs.

MX-COM shares design technology and expertise on a cooperative basis with other semiconductor oriented subsidiaries within the CML Microsystems Plc Group. This greatly enhances the technical depth and capability supporting new product developments and optimizes the distribution and support of product. The following partial organization chart identifies these subsidiaries within the CML Microsystems Plc corporate structure:


CML Microsystems Plc
MX-COM, Inc.
CML Microcircuits (Singapore) Pte Ltd
Integrated Micro Systems Limited
Consumer Microcircuits Limited
Other Group Members...

Coordinating closely with Consumer Microcircuits Limited ("CML" for short), a similarly fully functioning affiliate located in the U.K., MX-COM products can be confidently and reliably second sourced by virtue of their independent manufacturing capability.

MX-COM's focused designs provide an attractive balance of power, performance, size, and cost benefits to consistently satisfy customers ranging from small start-up companies to some of the worlds largest, high volume consumer electronics manufacturers.

Quality and Reliability

MX-COM's quality policy is to meet or exceed customer expectation, pursuing Total Customer Satisfaction in all aspects of each customer's relationship with us. Since January 1995, MX-COM has been registered to ISO-9002 through Underwriters Laboratories.

The principles guiding MX-COM are:

- Unquestionable ethics and integrity
- Respect for the individual
- Total customer satisfaction
- Quality first: profit is a by-product
- Provide equality and reward initiative

Product quality and reliability are an integral part of our product definition objectives and manufacturing practices. For instance, MX-COM products are implemented according to conservative design rules and fabricated using well-established, reliable processes at qualified foundries. Foundry processes are independently tested for reliability performance by MX-COM, in addition to reliability testing which is performed by the foundry. The product is then assembled at the MX-COM facility in North Carolina or by qualified third party assembly operations. Conformance to quality and reliability requirements is strictly monitored through inspection, audit procedures, and periodic reliability monitors. Electrical test, at wafer level and finished assembly, is performed at the Winston-Salem facility using proprietary hardware and software using calibration standards that are NIST traceable. Product traceability is provided throughout the production cycle.

We continue to build on this quality standard and extend it to all aspects of our business.

Product Profile

MX-COM's devices perform critical functions for many familiar end products. Although their most common purpose is to perform or facilitate electronic communications, this can take many forms. The following product examples illustrate some of MX-COM's product range:

- CMX017 UHF FM/MSK Transmitter and CMX018 UHF FM/FSK Receiver for spread spectrum applications.
- MX102 autocorrelator filters out random noise and preserves coherent tone information to increase S/N and the operating range of pagers.
- CMX589A 4kbps to 200kbps GMSK filter/modem supports Cellular Digital Packet Data (CDPD) engine to provide digital data messaging in cellular telephones.
- CMX602A Caller ID on Call Waiting telecom processor with ring detector, 1200bps FSK demodulator, 2nd call alert dual tone detector, and asynchronous/synchronous serial output port provides a very low cost, low power engine for competitive high volume designs.
- MX818 baseband signal processor streamlines FM land mobile trunked radio addressing/selective squelch applications with Rx and Tx audio processing (limiter, splatter filter, etc.), 15 parallel programmable sub-audio tone detectors, 2 sub-audio tone encoders, digitally controlled amplifiers for two point r.f. modulation support, and 23/24 tone address CODEC.
- MX839 digitally controlled analog I/O processor trims parts count and cost with four input intelligent 8/10 bit A/D monitoring subsystem, three 8/10 bit DACs, two digitally controlled attenuators, programmable A/D clock frequency, and IRQ generator.
- MX919B wireless modem data pump provides a low software overhead engine to achieve robust high performance data networks through the use of root raised cosine filtered four level FSK Tx and Rx demodulation, CRC error detection, interleaving, forward error correction, and embedded packet protocol primitives.
- MX980 digital radio 36kbps $\pi/4$ DQPSK baseband processor for portable radios and base stations includes an optimized DSP engine to provide configurable root raised cosine filters, quadrature I/O interfaces, and eight A/D and D/A converters for system support functions.

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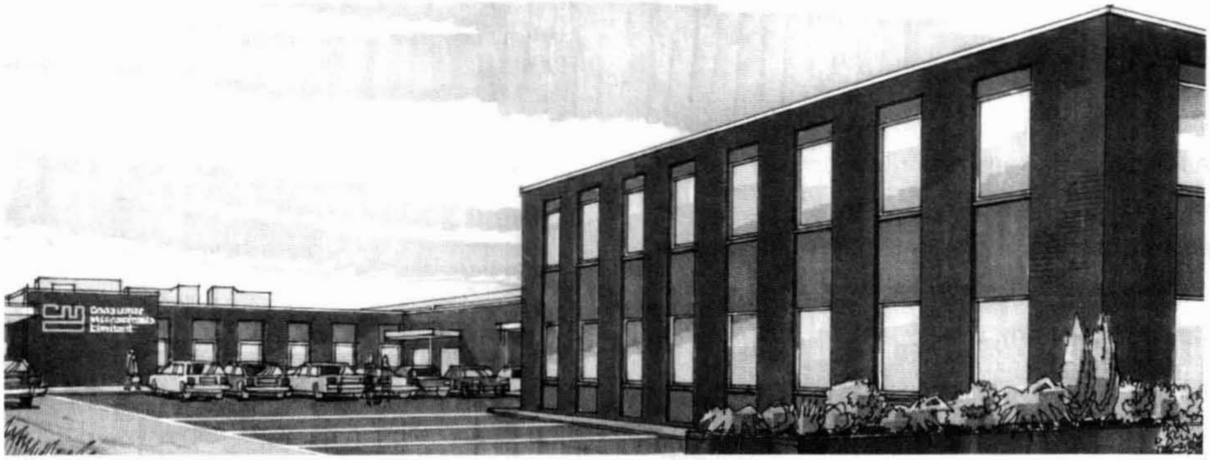

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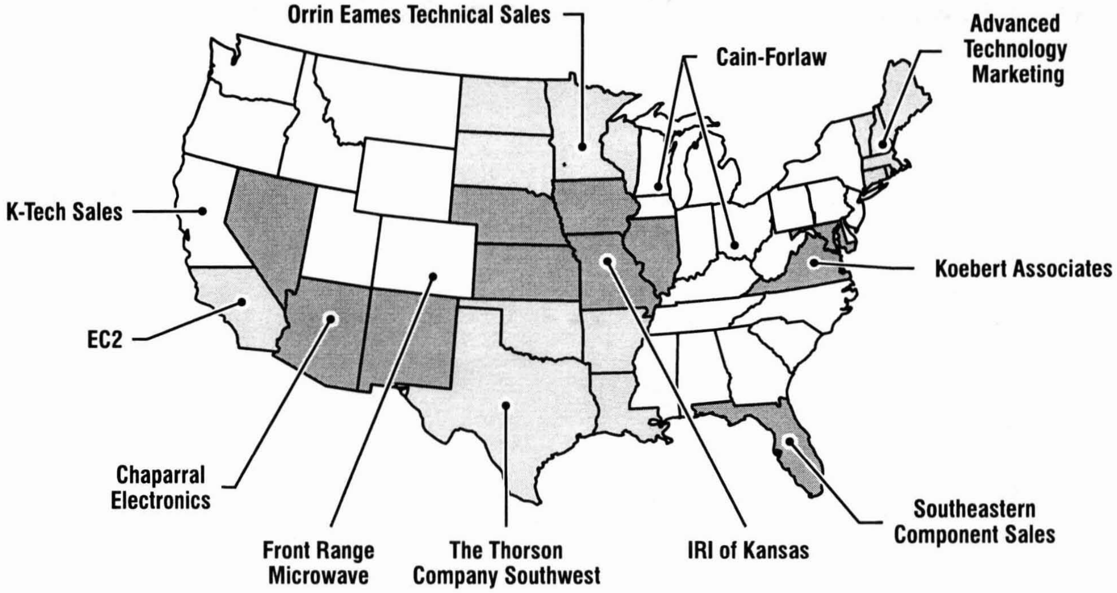
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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX017 UHF FM/FSK Transmitter

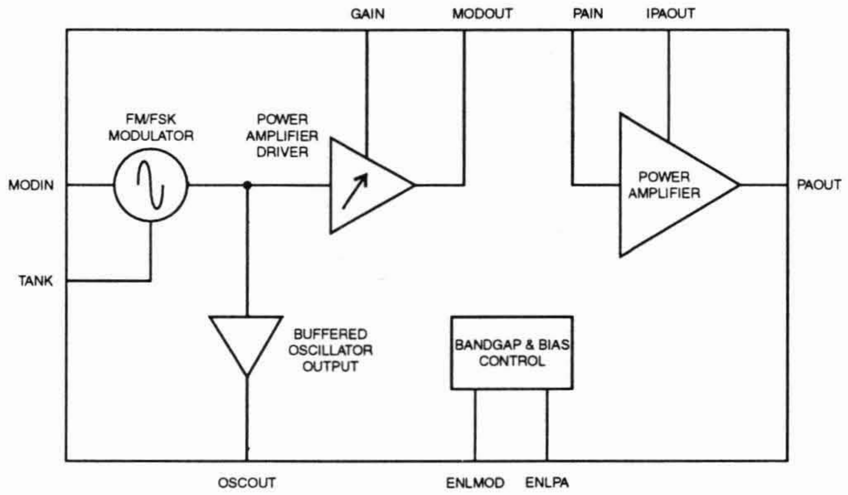
ADVANCE INFORMATION

Features

- Direct FM/FSK UHF Modulator
- Adjustable Modulator Output Power
- Integrated Power Amplifier with Output Power up to +20dBm
- Low Power 2.7V Operation
- Powersave and Zero-Power (<10µA) Modes
- 28-Pin SSOP Package

Applications

- General Radio Link 865-965 MHz
- General 915MHz ISM Band (USA)
- Spread Spectrum Wireless Systems
- Fixed Frequency Transmissions
- Analog/Digital Cordless Phones
- Handheld Data Terminals
- SO-HO Wireless Data Links


GAIN
MODOUT
PAIN
IPAOUT
FM/FSK MODULATOR
POWER AMPLIFIER DRIVER
MODIN
TANK
POWER AMPLIFIER
PAOUT
BUFFERED OSCILLATOR OUTPUT
BANDGAP & BIAS CONTROL
OSCOUT
ENLMOD
ENLPA

The CMX017 is a single chip UHF FM/FSK transmitter that combines both the RF VCO Modulator and RF Power Amplifier. It is suitable for both audio FM and digital FSK transmissions.

A buffered oscillator output provides the RF signal drive to an external synthesizer or fixed frequency phase-locked loop for channel frequency selection. Modulator output power is adjustable over a 20dB range and the integrated power amplifier delivers up to +20dBm. The device also includes a powersave mode: "Transmit Standby" and a zero-power mode: "Sleep". These allow independent power down control of both the modulator and power amplifier, thereby maximizing battery life. The device can be used in conjunction with the CMX018, a double-conversion super-heterodyne receiver, to implement a complete UHF radio link.

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1 Block Diagram

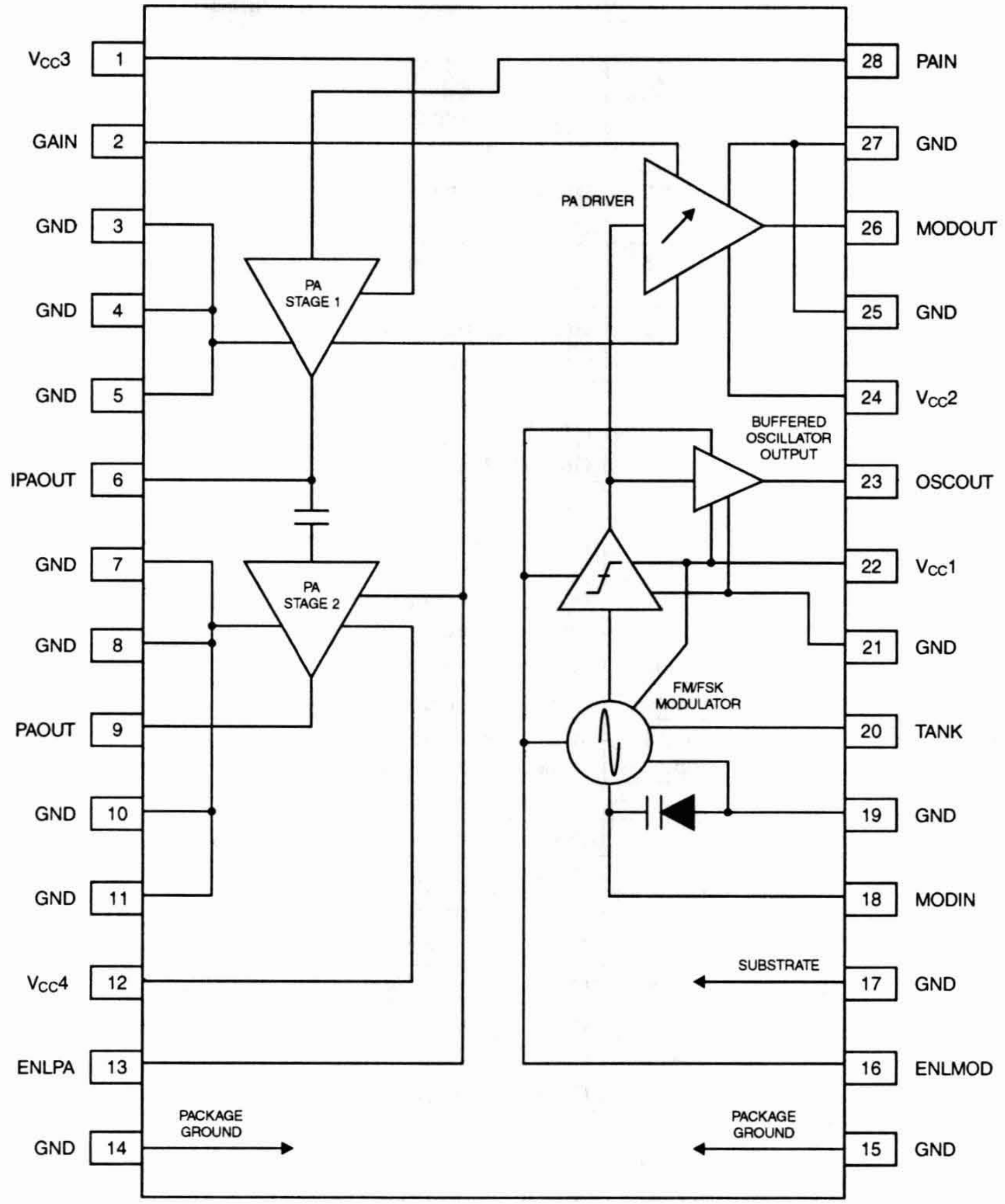

$V_{CC}3$
1
GAIN
2
GND
3
GND
4
GND
5
IPAOUT
6
GND
7
GND
8
PAOUT
9
GND
10
GND
11
$V_{CC}4$
12
ENLPA
13
GND
14
PA STAGE 1
PA STAGE 2
PACKAGE GROUND
28
PAIN
27
GND
26
MODOUT
25
GND
24
$V_{CC}2$
23
OSCOUT
22
$V_{CC}1$
21
GND
20
TANK
19
GND
18
MODIN
17
GND
16
ENLMOD
15
GND
PA DRIVER
BUFFERED OSCILLATOR OUTPUT
FM/FSK MODULATOR
SUBSTRATE
PACKAGE GROUND

Figure 1: Internal Block Diagram

2 Signal List

Pin No.	Signal		Description
D6 Package	Name	Type	
1	$V_{CC}3$	power	Power amplifier (first stage) power supply - nominally 3.0V
2	GAIN	input	Modulator output (pin 26) - Power control
3	GND	ground	Ground-plane connection to the power amplifier
4	GND	ground	Ground-plane connection to the power amplifier
5	GND	ground	Ground-plane connection to the power amplifier
6	IPAOUT	output	Output (open-collector) from the first stage of the power amplifier
7	GND	ground	Ground-plane connection to the power amplifier
8	GND	ground	Ground-plane connection to the power amplifier
9	PAOUT	output	Output (open-collector) from the second stage of the power amplifier
10	GND	ground	Ground-plane connection to the power amplifier
11	GND	ground	Ground-plane connection to the power amplifier
12	$V_{CC}4$	power	Power amplifier (second stage) power supply – nominally 3.0V
13	ENLPA	CMOS input	Power Amplifier powersave logic control. A logic "0" powers down the Power Amplifier and Driver stages
14	GND	ground	Ground-plane connection
15	GND	ground	Ground-plane connection
16	ENLMOD	CMOS input	Modulator zero-power logic control. A logic "0" powers down the Modulator and Buffered Oscillator stages
17	GND	ground	Ground-plane connection
18	MODIN	input	Baseband modulation input signal
19	GND	ground	Ground-plane connection to the VCO
20	TANK	input	VCO Tank circuit/Resonator connection
21	GND	ground	Ground-plane connection to the modulator and VCO buffer
22	$V_{CC}1$	power	Modulator power supply – nominally 3.0V
23	OSCOUT	output	Buffered Oscillator (open-collector) output
24	$V_{CC}2$	power	Power Amplifier Driver power supply - nominally 3.0V
25	GND	ground	Ground-plane connection for the Power Amplifier Driver
26	MODOUT	output	Modulator output
27	GND	ground	Ground-plane connection for the Power Amplifier Driver
28	PAIN	input	Power Amplifier input

Table 1: Signal List

3 External Components

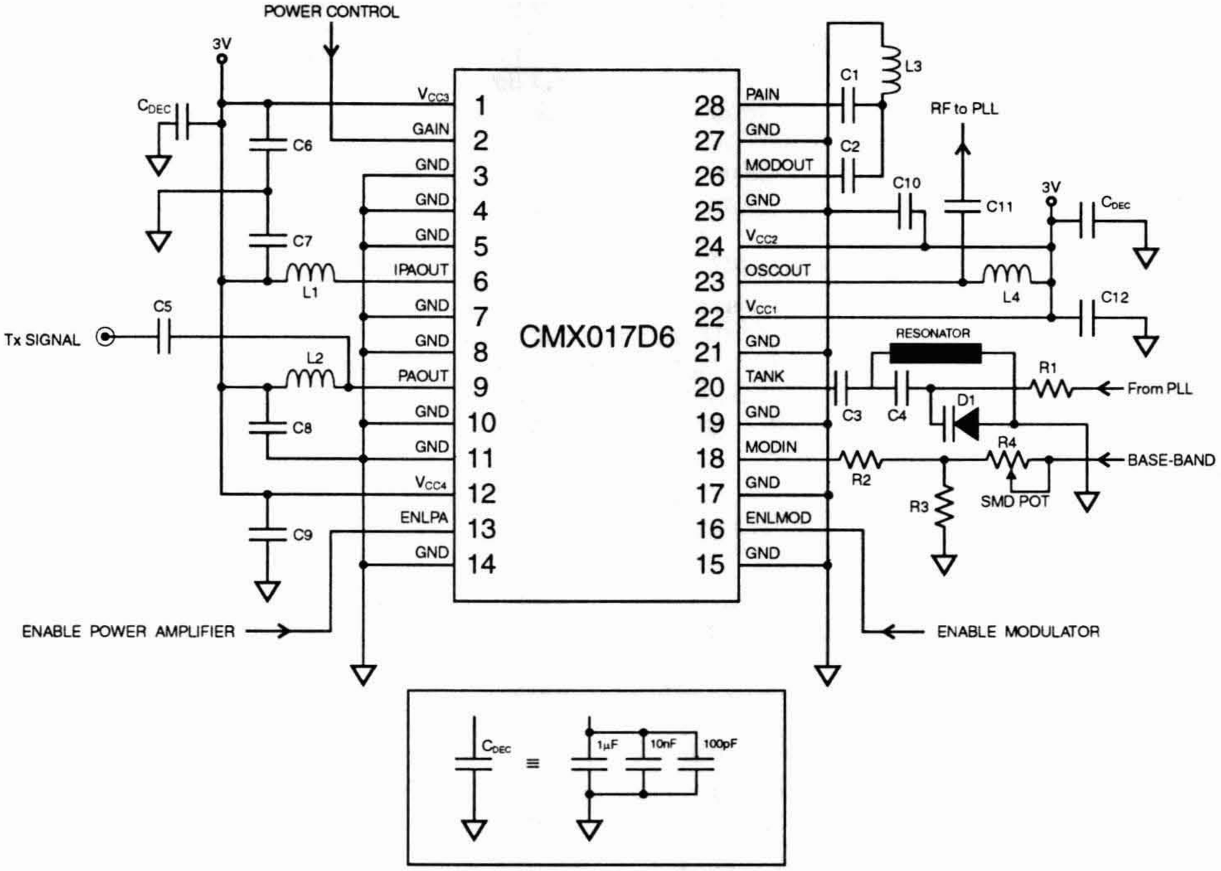

POWER CONTROL
3V
CDEC
C6
C7
L1
C5
Tx SIGNAL
L2
C8
C9
ENABLE POWER AMPLIFIER
VCC3
GAIN
GND
IPAOUT
PAOUT
VCC4
ENLPA
1
2
3
4
5
6
7
8
9
10
11
12
13
14
CMX017D6
28
27
26
25
24
23
22
21
20
19
18
17
16
15
PAIN
MODOUT
VCC2
OSCOUT
VCC1
TANK
MODIN
ENLMOD
C1
L3
C2
RF to PLL
C10
C11
3V
CDEC
L4
C12
RESONATOR
R1
From PLL
C3
C4
D1
R4
BASE-BAND
R2
R3
SMD POT
ENABLE MODULATOR
CDEC
≡
1µF
10nF
100pF

Figure 2: Example of CMX017 with External Components

C1	5.6pF
C2	33pF
C3	4.3pF
C4	TBD
C5	100pF
C6	100pF
C7	100pF
C8	100pF
C9	100pF
C10	100pF
C11	100pF

C12	100pF	
D1	Varactor	Varactor diode, type SMV1233-011
~	Resonator	Co-Axial Resonator, type RG402, length = 11mm, shorted end
L1	1.5nH	
L2	22nH	
L3	6.8nH	
L4	22nH	
R1	10kΩ	
R2	10kΩ	
R3	TBD	Value is application dependent
R4	TBD	SMD potentiometer - value is application dependent

Note: Components are surface mount, type SMD0603, unless otherwise indicated.

Figure 3: Example of CMX017 with External Components for 915MHz Operation

4 General Description

The CMX017 is a single chip UHF FM/FSK transmitter that combines both the RF VCO Modulator and RF Power Amplifier. It is suitable for both audio FM and digital FSK transmissions.

A buffered oscillator output provides the RF signal drive to an external synthesizer or fixed frequency phase-locked loop for channel frequency selection. Modulator output power is adjustable over a 20dB range and the integrated power amplifier delivers up to +20dBm. The device also includes a powersave mode: "Transmit Standby" and a zero-power mode: "Sleep". These allow independent power down control of both the modulator and power amplifier, thereby maximizing battery life. The device can be used in conjunction with the CMX018 a double-conversion super-heterodyne receiver, to implement a complete UHF radio link.

4.1 FM/FSK Modulator + PA Driver

The modulator circuit uses an integrated oscillator whose frequency can be directly modulated by the DC-coupled input base-band signal, at the MODIN pin, to generate a frequency modulated (FM or FSK) RF signal. The oscillator requires an external varactor and resonator circuit, connected at the TANK pin, to tune to the required RF channel. A buffered oscillator signal is provided from an open-collector output, at the OSCOUT pin, to drive an external frequency synthesizer for the channel selection.

The output power, at the MODOUT pin, is variable over a 20dB range. The output power is maximum when the GAIN pin is connected to V_{CC} and is reduced by typically 20dB when this pin is connected to 0V. The output impedance at the MODOUT pin is typically 50Ω.

4.2 Power Amplifier (PA)

The power amplifier has two internal stages, each biased for class-B operation, and is designed to have a fixed overall power gain. The input and output impedances are typically 50Ω. A typical power gain improvement f 2dB is achieved using simple external matching networks.

4.3 Powersave and Zero-Power Modes

The Modulator and Buffered Oscillator stages are powered down independently of the PA Driver + Power Amplifier stages by means of the ENLMOD and ENLPA logic inputs:

A logic '0' at ENLMOD powers down the Modulator and Buffered Oscillator stages.

A logic '0' at ENLPA powers down the PA Driver and Power Amplifier stages.

Refer to the block diagram in Figure 1 and to Section 5.

5 Application Notes

5.1 Generation of the Modulated RF Signal

The modulator on the CMX017 relies on the direct modulation of the RF Voltage Controlled Oscillator (VCO), which is stabilized to the channel center frequency by an external Frequency Synthesizer or Phase Locked Loop (PLL). The user has control over the external PLL filter and VCO tank components and choice of these components will have an impact upon the following PLL parameters:-

Closed loop bandwidth, settling time and transient response
Modulation linearity
VCO phase noise

Three modulation requirements may be achieved as follows:

5.1.1 The minimum modulation signal frequency is above the PLL Closed Loop Bandwidth

In applications where the transmit channel frequency is fixed or occasionally changed, a narrow PLL bandwidth can be chosen such that the minimum modulation frequency is in excess of the PLL bandwidth. With the PLL active whilst the base-band signal is applied to the modulator there will be negligible distortion of the modulated RF output signal. A benefit of this technique is that an output phase noise improvement is achieved, compared to the free running VCO phase noise characteristic.

5.1.2 The minimum modulation signal frequency is within the PLL Closed Loop Bandwidth

In Frequency Hopped Spread Spectrum applications the frequency synthesizer must be agile. Consequently the PLL bandwidth should be designed to achieve the required hop-rate and, in most systems this bandwidth will exceed the minimum modulation frequency. With the PLL active during modulation, the loop will compensate for the signal frequency components within the loop bandwidth, introducing a frequency dependant distortion of the modulated RF output signal.

To avoid the modulation distortion the carrier frequency is tuned by the external synthesizer chip, with no modulating signal applied. The synthesizer control is then disabled, by setting the charge-pump output of the synthesizer to tri-state. The DC coupled base-band signal, applied to the MODIN pin, then modulates the free running VCO to generate the FM or FSK output signal.

5.1.3 A flat modulator response is required down to DC, whilst benefiting from the phase noise improvements due to the PLL (Two-Point Modulation).

Unlike in the above two cases, where a fixed reference frequency is used in the PLL, the Two-Point Modulation technique requires modulation inputs to both the PLL reference oscillator and to the RF VCO circuits.

The modulation signal should be applied to both modulation inputs with suitable AC/DC levels and with the correct phase to achieve cancellation of the loop's feedback. This prevents the radio's PLL circuitry from counteracting the modulation process and so provides a clean flat modulation response down to DC.

5.2 Powersave and Zero-Power Modes

It is possible to power down each section of the transmitter independently. This feature may be useful when the CMX017 is configured, with the CMX018, as a radio transceiver. It allows the transmitter to be powered on and off, thereby saving power, during the sleep and standby periods.

In **SLEEP** mode (ENLMOD='0' and ENLPA='0') all sections of the device are powered down and the current consumption is reduced to less than 10µA. This is the zero-power mode.

In **TRANSMIT-STANDBY** mode (ENLMOD='1' and ENLPA='0') only the PA Driver and Power Amplifier stages are powered down, while the Modulator and Buffered Oscillator remain active. This powersave mode allows the external frequency synthesizer to stabilize the channel center frequency prior to the RF transmission.

In **TRANSMIT** mode (ENLMOD='1' and ENLPA='1') both the Modulator and the Power Amplifier sections of the device are fully operational.

Note: The device can be used as a stand alone "**UHF Power Amplifier**" by forcing (ENLMOD='0' and ENLPA='1'). The efficiency is maximized by connecting the $V_{CC}2$ pin to 0V. (The $V_{CC}1$ pin must remain connected to 3.0V.)

5.3 Lower Output Power Applications

For very short range applications the antenna drive can be taken from the modulator output, MODOUT, at pin 26. The Power Amplifier is powered down by connecting $V_{CC}3$ and $V_{CC}4$ (pins 1 and 12) to 0V. This allows the supply current to be minimized and the Modulator output to be enabled or disabled using the ENLPA input at pin 13.

5.4 Example Schematic and Layout

The following schematic (Figure 4) and printed circuit layout (Figure 5 and Figure 6) present a typical application interface for the CMX017. To aid legibility, the schematic and layout are available electronically from the MX-COM website http://www.mxcom.com.

Alternative components and component values are shown on the schematic. These should be selected according to the intended application. The schematic uses the following ICs:

U2	IC Works	WB1315X
U4	Analog Devices	AD8532-SO8

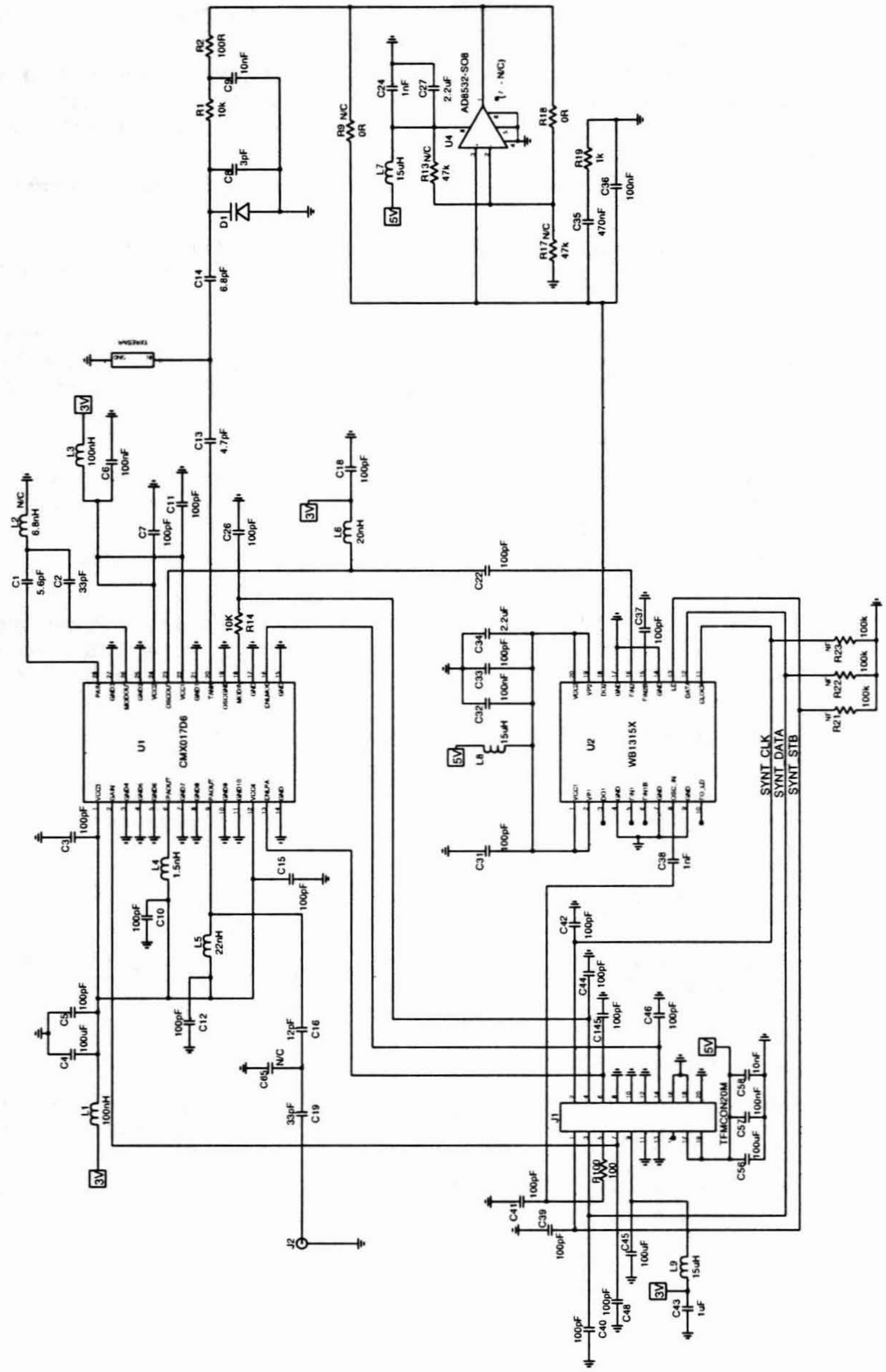

U1
CMX017D6
U2
WB1315X
U4
AD8532-SO8
J1
TFMCON20M
J2
SYNT CLK
SYNT DATA
SYNT STB
5V
3V
C1 5.6pF
C2 33pF
C3 100pF
C4 100uF
C5 100pF
C6 100nF
C7 100pF
C11 100pF
C12 100pF
C13 4.7pF
C14 6.8pF
C15 100pF
C16 12pF
C18 100pF
C19 33pF
C22 100pF
C24 1nF
C26 100pF
C27 2.2uF
C31 100pF
C32
C33 100nF
C34 2.2uF
C35 470nF
C36 100nF
C37 100pF
C38 1nF
C43 1uF
C45 100uF
C65 N/C
D1
L1 100nH
L2 6.8nH N/C
L3 100nH
L4 1.5nH
L5 22nH
L6 20nH
L7 15uH
L8 15uH
L9 15uH
R1 10k
R2 100R
R9 N/C 0R
R13 N/C 47k
R14 10K
R17 N/C 47k
R18 0R
R19 1k
R21 100k
R22 100k
R23 100k

Figure 4: Application Schematic

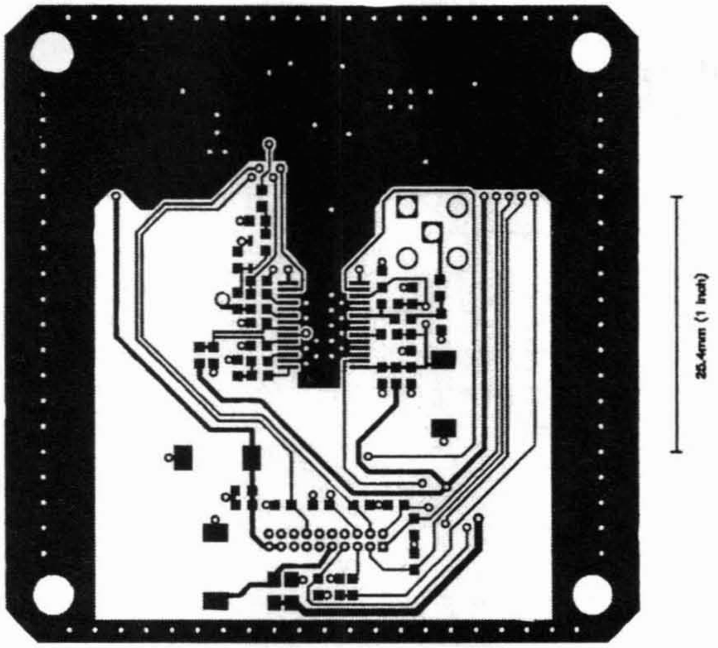

25.4mm (1 inch)

Figure 5: Application Layout - Top Copper

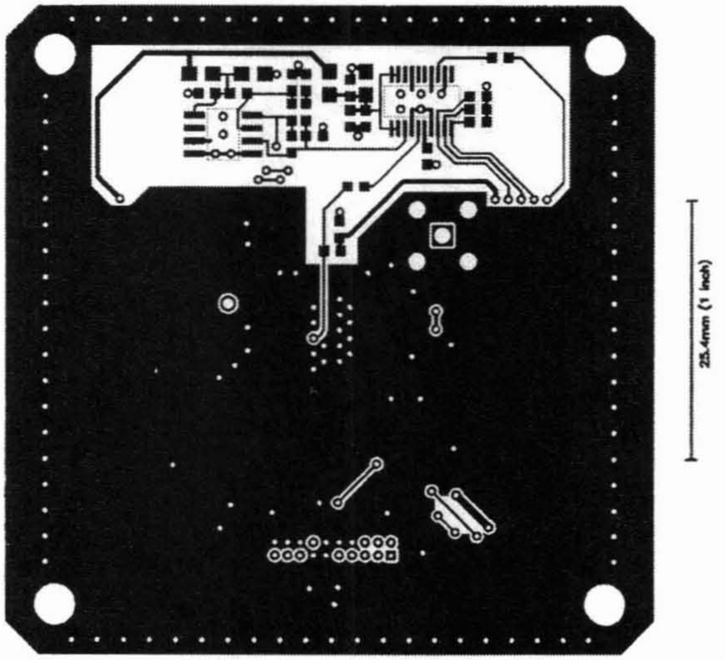

25.4mm (1 inch)

Figure 6: Application Layout - Bottom Copper

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Pins	Min.	Max.	Units
Supply Voltage (V_{CC})	17, 22, 25	-0.3	7.0	V
Input Voltage	27, 28	-0.3	V_{CC} + 0.3	V
LNA Input Power	1		0	dBm
D6 Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	+125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply Voltage (V_{CC})		2.7	3.3	V
RF Input Range		865	965	MHz
Operating Temperature		-10	+60	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{CC} = 2.7V to 3.3V, T_{AMB} = - 10°C to +60°C,
RF = 915MHz, 50Ω source and load impedance.

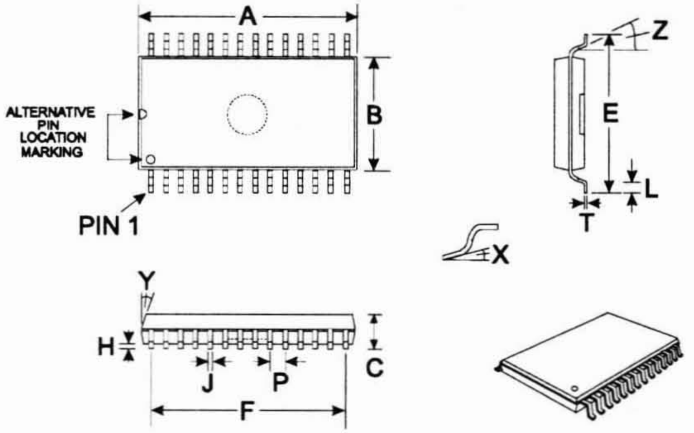
	Pin	Min.	Typ.	Max.	Units
DC Parameters					
I_{CC} (ENABLE = V_{CC} and GAINSEL = 0V)	17, 22, 25		50		mA
I_{CC} (ENABLE = V_{CC} and GAINSEL = V_{CC})	17, 22, 25		42		mA
I_{CC} (ENABLE = 0V)	17, 22, 25			10	µA
AC Parameters					
LNA (RF = 915MHz)					
Power Gain (GAINSEL = 0V)	1, 3		16		dB
Power Gain (GAINSEL = V_{CC})	1, 3		-6.0		dB
Noise Figure	1, 3		3.0		dB
Input 1dB Gain Compression Point (GAINSEL = 0V)	1		-20		dBm
Input 1dB Gain Compression Point (GAINSEL = V_{CC})	1		16		dBm
Input Third Order Intercept Point (GAINSEL = 0V)	1		-10		dBm
Input Third Order Intercept Point (GAINSEL= V_{CC})	1		25		dBm
Reverse Isolation (GAINSEL = 0V)	3, 1		-35		dB
Reverse Isolation (GAINSEL = V_{CC})	3, 1		-6.0		dB
Input Impedance	1		50		Ω
Output Impedance	3		50		Ω
Input Return Loss (50Ω source)	1		*10*		dB
Output Return Loss (50Ω load)	3		*15*		dB
VCO to LNA Leakage	1		-45		dBm
First Down Converter (RF = 915MHz and IF = 70MHz)					
Conversion Gain	5, 6		15		dB
Noise Figure	5, 6		15		dB
Input 1dB Gain Compression Point	6		-12		dBm
Input Third Order Intercept Point	6		-4.0		dBm
Input Impedance	5		50		Ω
Output Impedance	6		100		Ω
Input Return Loss (50Ω source)	5		TBD		dB
Output Return Loss (50Ω load)	6		TBD		dB
Buffered oscillator output power	21		-10		dBm
RF to IF Leakage	5, 6		TBD		dB
LO to IF Leakage	6		TBD		dBm
LO to RF Leakage	5		TBD		dBm

	Pin	Min.	Typ.	Max.	Units
Second Down Converter (RF = 70MHz and IF = 10.7MHz)					
Conversion Gain	8, 9		24		dB
Noise Figure	8, 9		13		dB
Output 1dB Gain Compression Point	9		-11		dBm
Output Third Order Intercept Point	9		-2		dBm
Input Impedance	8		100		Ω
Output Impedance	9		430		Ω
Limiting Amplifier and RSSI (IF = 10.7MHz)					
Bandwidth	11, 16		40		MHz
Internal Voltage Gain	11		74		dBV
Input Impedance	11		430		Ω
RSSI Dynamic Range	14		*TBD*		dB
RSSI Slope	14		*TBD*		V/dB
RSSI Voltage Range [1]	14		*TBD*		V
Demodulator (IF = 10.7MHz)					
Output Swing [2]	18		*TBD*		mVp-p
Output Impedance	18		1		kΩ

Notes:

1. Input power = TBD to TBD
2. 125kHz Deviation, 1kΩ Load

6.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	0.396 (10.06)		0.407 (10.34)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.333 (8.45)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 28-Pin Plastic SSOP Mechanical Outline: ***Order as part no. CMX018D6***

6.3 Handling Precautions

This device is a high performance RF integrated circuit and is ESD sensitive.
Adequate precautions must be taken during handling and assembly of this device.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX018 UHF FM/FSK Receiver

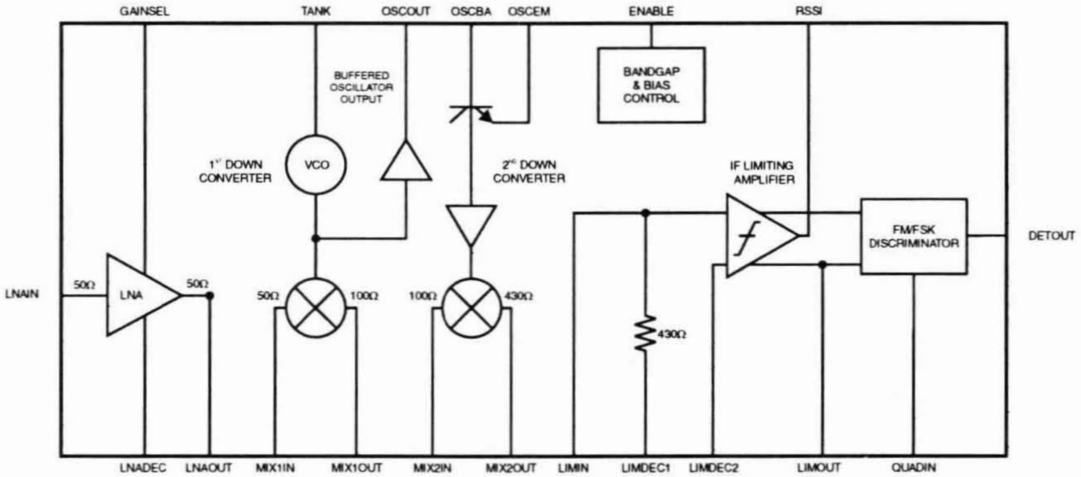
ADVANCE INFORMATION

Features

- **Double Conversion Super-Heterodyne Receiver and FM/FSK Demodulator**
- **LNA with Switched Gain**
- **High Performance UHF Down-Converter Stage with Integrated VCO**
- **2.7V Operation**
- **Zero-Power Mode (<10μA)**
- **Temperature Compensated RSSI**
- **28-Pin SSOP Package**

Applications

- **High Performance Analog/Digital Radio Links (865-965MHz)**
- **General ISM 915MHz Band**
- **Analog/Digital Cordless Phones**
- **Spread Spectrum Receivers**
- **Analog FM Receivers**
- **Handheld Data Terminals**
- **SO-HO Wireless Data Links**


GAINSEL
TANK
OSCOUT
OSCBA
OSCEM
ENABLE
RSSI
BUFFERED OSCILLATOR OUTPUT
BANDGAP & BIAS CONTROL
1st DOWN CONVERTER
VCO
2nd DOWN CONVERTER
IF LIMITING AMPLIFIER
FM/FSK DISCRIMINATOR
DETOUT
LNAIN
50Ω
LNA
50Ω
50Ω
100Ω
100Ω
430Ω
430Ω
LNADEC
LNAOUT
MIX1IN
MIX1OUT
MIX2IN
MIX2OUT
LIMIN
LIMDEC1
LIMDEC2
LIMOUT
QUADIN

The CMX018 is a single chip UHF FM/FSK double-conversion super-heterodyne receiver. It combines a dual gain mode Low Noise Amplifier (LNA), two down-converters (including integrated oscillators), limiting amplifier, RSSI, FM/FSK demodulator and zero-power mode control.

The CMX018 can be used in conjunction with the CMX017, an integrated FM/FSK modulator and transmitter, to implement a complete UHF radio link.

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3 External Components....................3 - 21

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- 4.2 First Down-Converter....................3 - 22
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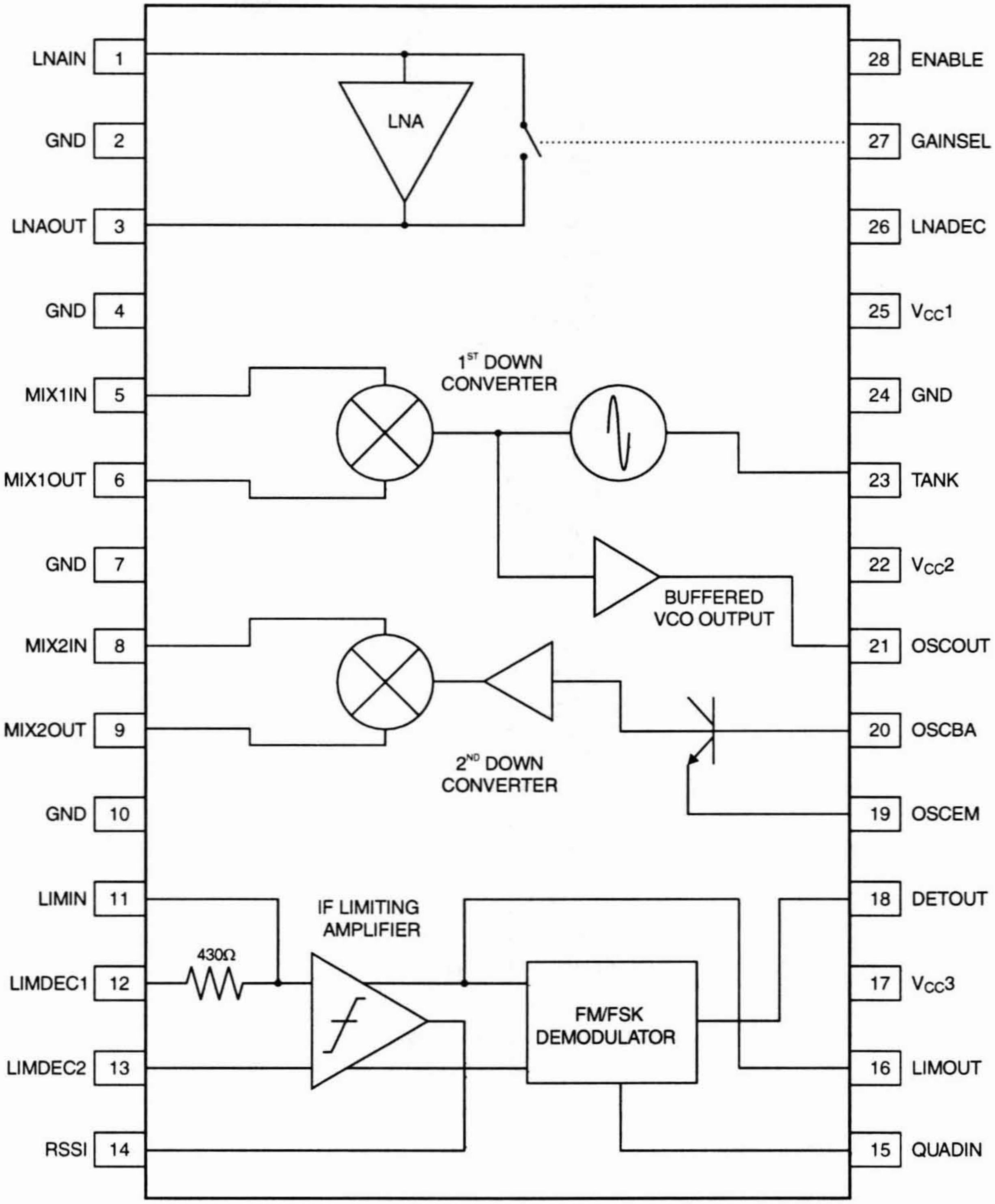
1 Internal Block Diagram



LNAIN
1
GND
2
LNAOUT
3
GND
4
MIX1IN
5
MIX1OUT
6
GND
7
MIX2IN
8
MIX2OUT
9
GND
10
LIMIN
11
LIMDEC1
12
LIMDEC2
13
RSSI
14
LNA
1ST DOWN CONVERTER
BUFFERED VCO OUTPUT
2ND DOWN CONVERTER
IF LIMITING AMPLIFIER
430Ω
FM/FSK DEMODULATOR
28
ENABLE
27
GAINSEL
26
LNADEC
25
VCC1
24
GND
23
TANK
22
VCC2
21
OSCOUT
20
OSCBA
19
OSCEM
18
DETOUT
17
VCC3
16
LIMOUT
15
QUADIN

Figure 1: Internal Block Diagram

2 Signal List

Pin No.	Signal		Description
Package D6	Name	Type	
1	LNAIN	input	LNA RF Input
2	GND	ground	LNA Ground connection
3	LNAOUT	output	LNA RF Output
4	GND	ground	LNA Ground connection
5	MIX1IN	input	RF Input to the First Down-Converter
6	MIX1OUT	output	IF Output from the First Down-Converter
7	GND	ground	First Down-Converter Ground connection
8	MIX2IN	input	RF Input to the Second Down-Converter
9	MIX2OUT	output	IF Output from the Second Down-Converter
10	GND	ground	Second Down-Converter, Limiting Amplifier, RSSI, and Demodulator stages - Ground connection
11	LIMIN	input	Input to the Limiting Amplifier
12	LIMDEC1	input	External Decoupling capacitors – one required at each limiting Amplifier Inputs
13	LIMDEC2	input	
14	RSSI	output	Receive Signal Strength Indicator output
15	QUADIN	input	Quadrature input to the FM Demodulator
16	LIMOUT	output	Output from the Limiting Amplifier
17	Vcc3	power	Power supply to the Second Down-Converter, Limiting Amplifier, RSSI and Demodulator stages – nominally 3.0V
18	DETOUT	output	Output of the FM/FSK Quadrature Demodulator
19	OSCEM		Emitter connection to the Second Down-Converter Local Oscillator transistor
20	OSCBA		Base connection to the Second Down-Converter Local Oscillator transistor
21	OSCOUT	output	Buffered Local Oscillator (Open-Collector) output from the First Down-Converter
22	Vcc2	power	First Down-Converter 3V Supply
23	TANK	input	First Down-Converter Local Oscillator (VCO) TANK/Resonator connection
24	GND	ground	First Down-Converter VCO Ground connection
25	Vcc1	power	LNA Power Supply – nominally 3.0V
26	LNADEC		External LNA bias decoupling capacitor
27	GAINSEL	CMOS input	LNA Gain control logic input. A logic '0' provides a typical power gain of 16dB and a logic '1' provides an attenuation of 6dB
28	ENABLE	CMOS input	Zero-Power logic control. A logic '0' powers down the device.

Table 1: Signal List

3 External Components

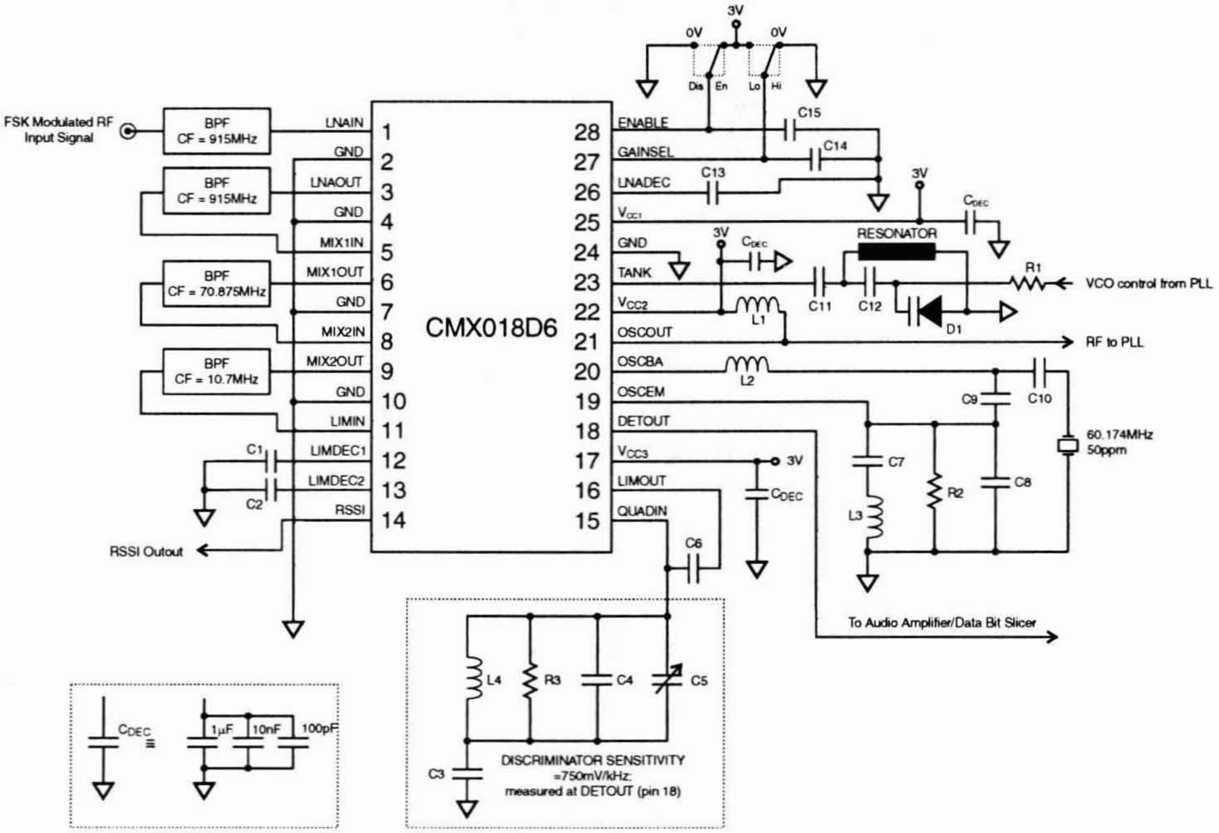

3V
0V
0V
Dis
En
Lo
Hi
C15
C14
C13
3V
CDEC
3V
CDEC
RESONATOR
R1
VCO control from PLL
C11
C12
D1
L1
RF to PLL
L2
C9
C10
60.174MHz
50ppm
C7
R2
C8
L3
3V
CDEC
C6
To Audio Amplifier/Data Bit Slicer
FSK Modulated RF
Input Signal
BPF
CF = 915MHz
BPF
CF = 915MHz
BPF
CF = 70.875MHz
BPF
CF = 10.7MHz
C1
C2
RSSI Outout
CMX018D6
LNAIN 1
GND 2
LNAOUT 3
GND 4
MIX1IN 5
MIX1OUT 6
GND 7
MIX2IN 8
MIX2OUT 9
GND 10
LIMIN 11
LIMDEC1 12
LIMDEC2 13
RSSI 14
28 ENABLE
27 GAINSEL
26 LNADEC
25 VCC1
24 GND
23 TANK
22 VCC2
21 OSCOUT
20 OSCBA
19 OSCEM
18 DETOUT
17 VCC3
16 LIMOUT
15 QUADIN
L4
R3
C4
C5
C3
DISCRIMINATOR SENSITIVITY
=750mV/kHz;
measured at DETOUT (pin 18)
CDEC
≡
1µF
10nF
100pF

Figure 2: Example of CMX018 with External Components

C1	100nF
C2	100nF
C3	100nF
C4	200pF
C5	8 – 50pF Trimmer
C6	5pF
C7	220pF
C8	6.8pF
C9	15pF
C10	33pF
C11	4.7pF
C12	6.2pF
C13	10nF
C14	100pF

C15	100pF	
D1	Varactor	Varactor diode, type SMV1233-011
~	Resonator	Co-Axial Resonator, type RG402, length = 11mm, shorted end
L1	22nH	
L2	680nH	
L3	680nH	
L4	1µH	
R1	10kΩ	
R2	10kΩ	
R3	2.0kΩ	Value is application dependent
X1	60.175MHz	50ppm crystal

Note: Components are surface mount, type SMD0603, unless otherwise indicated.

Table 2: Example of CMX018 with External Components

4 General Description

The CMX018 is a single chip UHF FM/FSK double-conversion super-heterodyne receiver. It combines a dual gain mode Low Noise Amplifier (LNA), two down-converters (including integrated oscillators), limiting amplifier, RSSI, FM/FSK demodulator and zero-power mode control.

The receiver frequency is selected using an external PLL or synthesizer which is driven by the buffered RF oscillator signal from the first down-converter.

The CMX018 can be used in conjunction with the CMX017, an integrated FM/FSK modulator and transmitter, to implement a complete UHF radio link.

4.1 Low Noise Amplifier

The LNA includes a switched gain function which is used to increase the dynamic range of the receiver. The gain is selected using the GAINSEL logic input at pin 2. With a logic '0' at the GAINSEL input a high gain is selected and the amplifier achieves the lowest noise figure. This mode is used where maximum sensitivity is required for low level input signals. Where high level signals are present at the receiver input, which cause difficulties due to inter-modulation, the gain of the LNA can be reduced by typically 22dB from about +16dB to about –6dB. The attenuation is selected by applying a logic '1' at the GAINSEL input which minimises the amount of non-linear distortion in the overall receiver at the expense of small signal sensitivity. The input and output impedances of the LNA are typically 50Ω.

4.2 First Down-Converter

The first down-converter includes a double balanced mixer with a low noise pre-amplifier, and on-chip oscillator components. The oscillator is configured as a 'high-sided' voltage controlled local oscillator, using an external varicap diode and tank resonator circuit, such that the first IF is typically centred at 70MHz. A buffered oscillator signal (OSCOUT at pin 21) is provided to drive the frequency synthesizer which controls the frequency tuning. The input impedance is typically 50Ω and the output impedance is typically 100Ω.

4.3 Second Down-Converter

The second down-converter also includes a double balanced mixer with a low noise pre-amplifier, and on-chip oscillator components. The oscillator is configured as a 'low-sided' local oscillator, using an external crystal at typically 60MHz, such that the second IF is centred at 10.7MHz. The input impedance is typically 100Ω and the output impedance is typically 430Ω.

4.4 Limiting Amplifier and RSSI

The limiting amplifier provides the IF amplification and limiting prior to the FM/FSK demodulator. An RSSI circuit is included which has temperature compensation. An RF signal level of -100dBm at the LNA input will produce an RSSI voltage of typically TBD mV. The RSSI voltage will increase with increasing RF input level at a rate of 20mV/dB up to a typical voltage of TBD V at a -60dBm RF input. In practice the absolute RSSI voltage will depend upon the insertion losses associated with each of the IF filters. The input impedance is typically 430Ω.

4.5 FM/FSK Demodulator

A quadrature detector is employed together with an external discriminator and phase shift network to demodulate the FM or FSK signal.

4.6 Zero-Power Mode

The device is powered down by applying a logic '0' level at the ENABLE input (pin 28). In this mode the device current is reduced to less than 10µA. This feature is useful when the device is operating within a transceiver where the receiver needs to be enabled and disabled.

A delay should be allowed for the receiver to settle after power-up. This is likely to be less that the crystal oscillator stabilization time, which may be altered by adjusting the value of R2, shown in Figure application.

5 Application Notes

5.1 General

Example Schematic and Layout

The following schematic (Figure 3) and printed circuit layout (Figure 4 and Figure 5) show a typical application interface for the CMX018. To aid legibility, the schematic and layout are available electronically from the MX-COM website http://www.mxcom.com.

Alternative components and component values are shown on the schematic. These should be selected according to the intended application. The schematic uses the following ICs:

U2	Motorola	MC34072D-SO8
U3	IC Works	WB1315X
U4	Analog Devices	AD8532-SO8

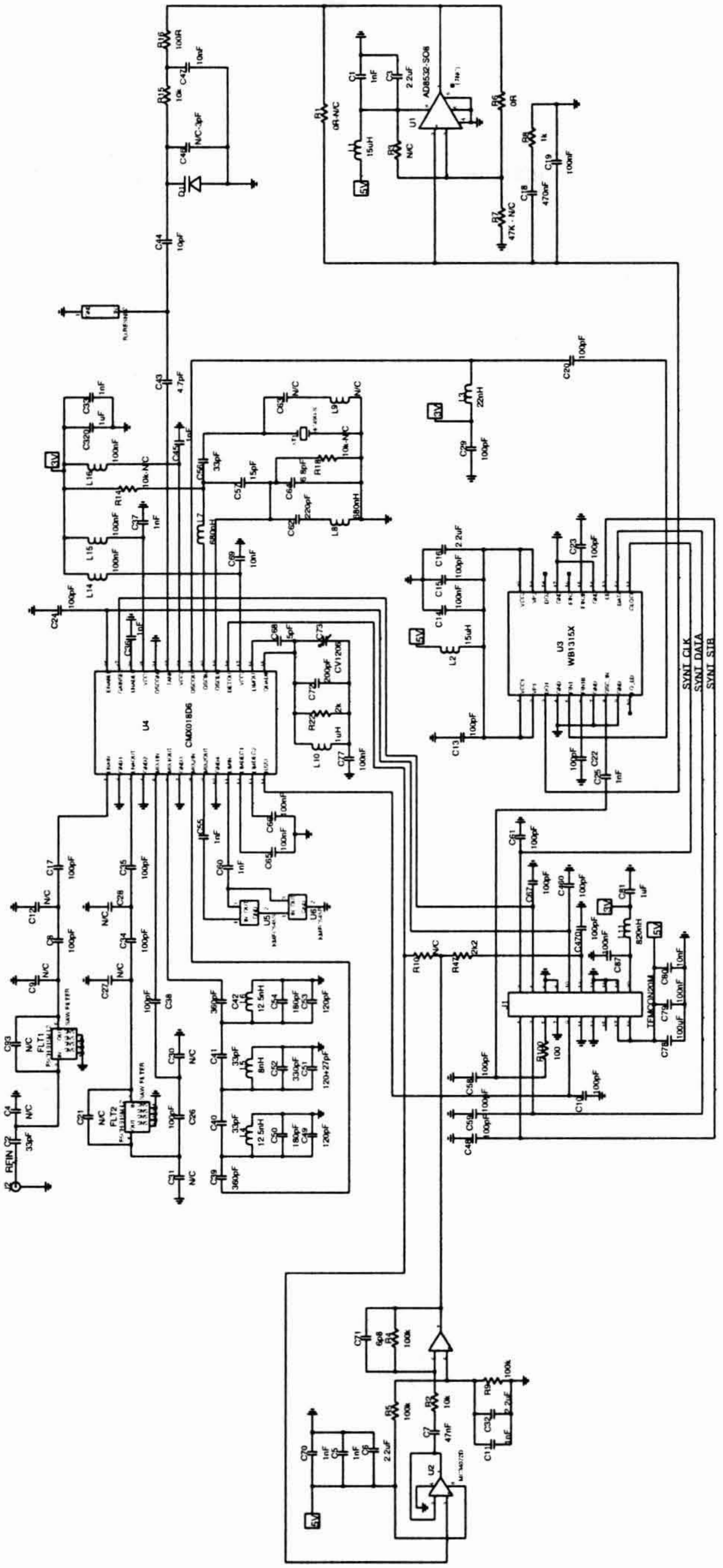

U4
CMX018D6
U3
WB1315X
U1
AD8532-SO8
U2
SYNT CLK
SYNT DATA
SYNT STB
RFIN
J2
FLT1
FLT2
SAW FILTER
5V

Figure 3: Application Schematic

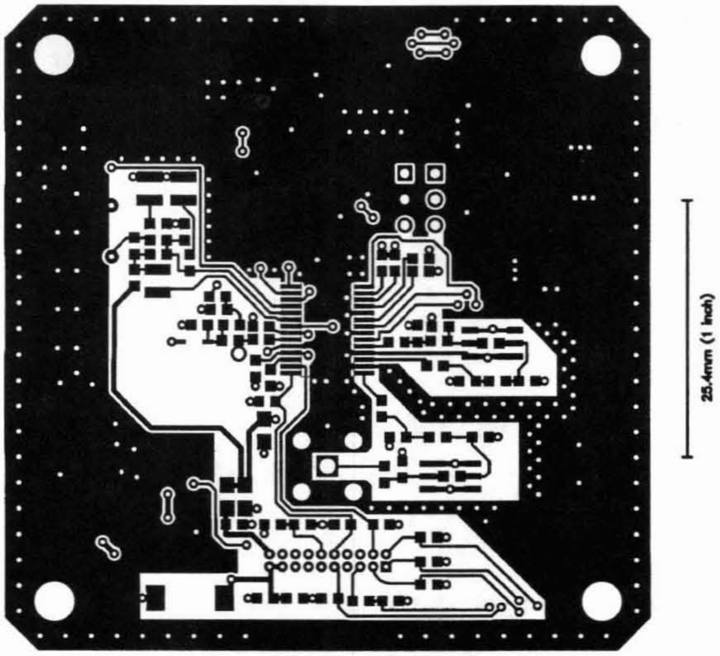

25.4mm (1 inch)

Figure 4: Application Layout - Top Copper

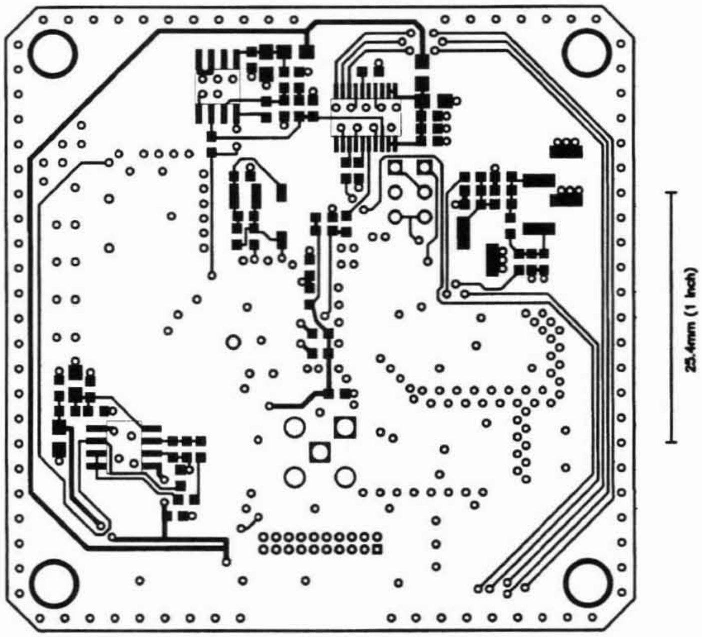

25.4mm (1 inch)

Figure 5: Application Layout - Bottom Copper

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Pins	Min.	Max.	Units
Supply Voltage (V_{CC})	17, 22, 25	-0.3	7.0	V
Input Voltage	27, 28	-0.3	V_{CC} + 0.3	V
LNA Input Power	1		0	dBm
D6 Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	+125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply Voltage (V_{CC})		2.7	3.3	V
RF Input Range		865	965	MHz
Operating Temperature		-10	+60	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{CC} = 2.7V to 3.3V, T_{AMB} = - 10°C to +60°C,
RF = 915MHz, 50Ω source and load impedance.

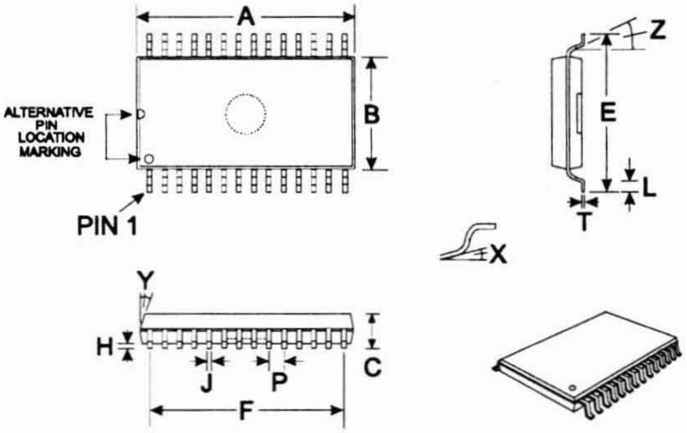
	Pin	Min.	Typ.	Max.	Units
DC Parameters					
I_{CC} (ENABLE = V_{CC} and GAINSEL = 0V)	17, 22, 25		50		mA
I_{CC} (ENABLE = V_{CC} and GAINSEL = V_{CC})	17, 22, 25		42		mA
I_{CC} (ENABLE = 0V)	17, 22, 25			10	µA
AC Parameters					
LNA (RF = 915MHz)					
Power Gain (GAINSEL = 0V)	1, 3		16		dB
Power Gain (GAINSEL = V_{CC})	1, 3		-6.0		dB
Noise Figure	1, 3		3.0		dB
Input 1dB Gain Compression Point (GAINSEL = 0V)	1		-20		dBm
Input 1dB Gain Compression Point (GAINSEL = V_{CC})	1		16		dBm
Input Third Order Intercept Point (GAINSEL = 0V)	1		-10		dBm
Input Third Order Intercept Point (GAINSEL= V_{CC})	1		25		dBm
Reverse Isolation (GAINSEL = 0V)	3, 1		-35		dB
Reverse Isolation (GAINSEL = V_{CC})	3, 1		-6.0		dB
Input Impedance	1		50		Ω
Output Impedance	3		50		Ω
Input Return Loss (50Ω source)	1		*10*		dB
Output Return Loss (50Ω load)	3		*15*		dB
VCO to LNA Leakage	1		-45		dBm
First Down Converter (RF = 915MHz and IF = 70MHz)					
Conversion Gain	5, 6		15		dB
Noise Figure	5, 6		15		dB
Input 1dB Gain Compression Point	6		-12		dBm
Input Third Order Intercept Point	6		-4.0		dBm
Input Impedance	5		50		Ω
Output Impedance	6		100		Ω
Input Return Loss (50Ω source)	5		TBD		dB
Output Return Loss (50Ω load)	6		TBD		dB
Buffered oscillator output power	21		-10		dBm
RF to IF Leakage	5, 6		TBD		dB
LO to IF Leakage	6		TBD		dBm
LO to RF Leakage	5		TBD		dBm

	Pin	Min.	Typ.	Max.	Units
Second Down Converter (RF = 70MHz and IF = 10.7MHz)					
Conversion Gain	8, 9		24		dB
Noise Figure	8, 9		13		dB
Output 1dB Gain Compression Point	9		-11		dBm
Output Third Order Intercept Point	9		-2		dBm
Input Impedance	8		100		Ω
Output Impedance	9		430		Ω
Limiting Amplifier and RSSI (IF = 10.7MHz)					
Bandwidth	11, 16		40		MHz
Internal Voltage Gain	11		74		dBV
Input Impedance	11		430		Ω
RSSI Dynamic Range	14		*TBD*		dB
RSSI Slope	14		*TBD*		V/dB
RSSI Voltage Range [1]	14		*TBD*		V
Demodulator (IF = 10.7MHz)					
Output Swing [2]	18		*TBD*		mVp-p
Output Impedance	18		1		kΩ

Notes:

1. Input power = TBD to TBD
2. 125kHz Deviation, 1kΩ Load

6.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	0.396 (10.06)		0.407 (10.34)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.333 (8.45)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 28-Pin Plastic SSOP Mechanical Outline: ***Order as part no. CMX018D6***

6.3 Handling Precautions

This device is a high performance RF integrated circuit and is ESD sensitive.
Adequate precautions must be taken during handling and assembly of this device.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX469A

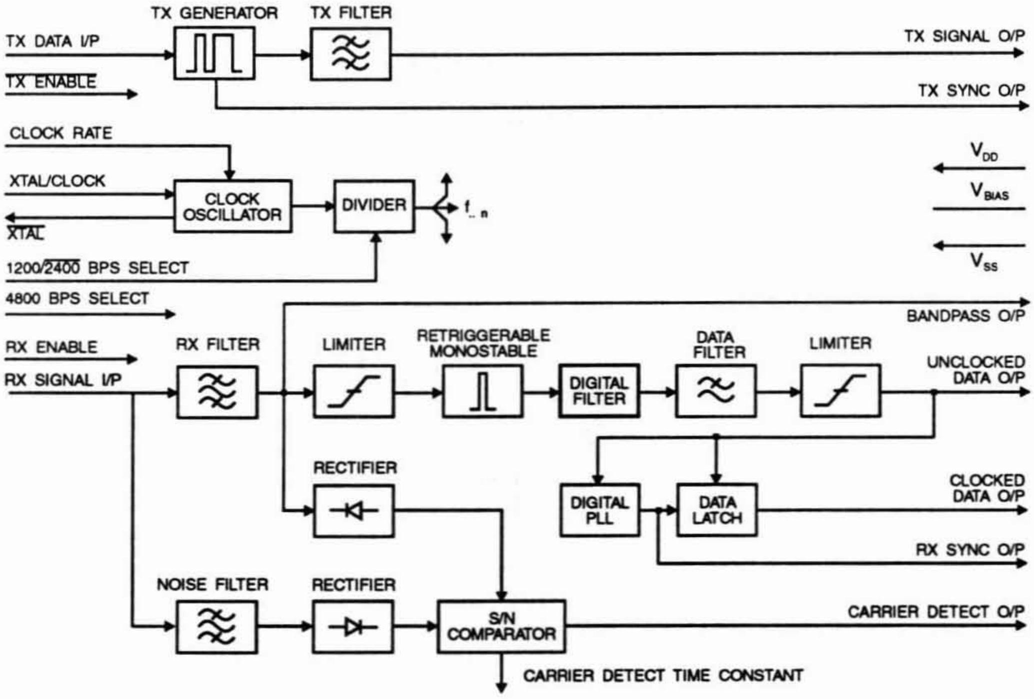
1200/2400/4800bps MSK Modem

Features

- **Selectable Data Rates 1200/2400/4800bps**
- **Full-Duplex MSK**
- **RX and TX Bandpass Filters**
- **Clock Recovery and Carrier Detect Capabilities**
- **Pin Selected Xtal/Clock Inputs 1.008MHz or 4.032MHz**

Applications

- **Radio and General Applications**
- **Data-Over-Radio**
- **PMR/Cellular Signaling**
- **Portable Data Terminals**
- **Personal/Cordless Telephone**


TX GENERATOR
TX FILTER
TX DATA I/P
TX ENABLE
TX SIGNAL O/P
TX SYNC O/P
CLOCK RATE
XTAL/CLOCK
CLOCK OSCILLATOR
DIVIDER
f_n
XTAL
1200/2400 BPS SELECT
4800 BPS SELECT
V_DD
V_BIAS
V_SS
BANDPASS O/P
RX ENABLE
RX SIGNAL I/P
RX FILTER
LIMITER
RETRIGGERABLE MONOSTABLE
DIGITAL FILTER
DATA FILTER
LIMITER
UNCLOCKED DATA O/P
RECTIFIER
DIGITAL PLL
DATA LATCH
CLOCKED DATA O/P
RX SYNC O/P
NOISE FILTER
RECTIFIER
S/N COMPARATOR
CARRIER DETECT O/P
CARRIER DETECT TIME CONSTANT

The CMX469A is a full-duplex pin-selectable 1200/2400/4800bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800, 1200/2400, and 2400/4800Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. The use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies, and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The CMX469A includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins. RX, TX and Carrier Detect circuits contain bandpass filters to provide high quality signals in their respective paths. The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

The CMX469A demonstrates high sensitivity and good bit-error-rate under adverse signal conditions.

The CMX469A operates with a 3.0V to 5.5V supply and is available in the following packages: 24-pin TSSOP (CMX469AE2), 20-pin SOIC (CMX469AD3), and 22-pin PDIP (CMX469AP6).

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX589A

HIGH-SPEED GMSK MODEM

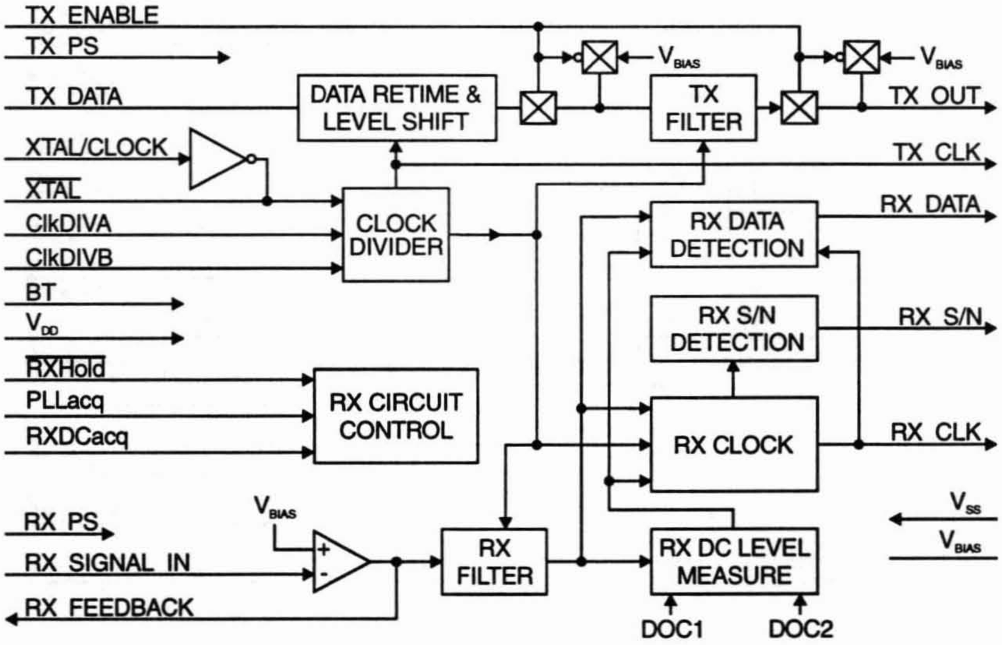
PRELIMINARY INFORMATION

Features

- **Data Rates from 4kbps to 200kbps**
- **Full or Half Duplex Gaussian Filter & Data Recovery for Minimum Shift Keying (GMSK) Designs**
- **Selectable BT: (0.3 or 0.5)**
- **Low Power**
  3.0V, 20kbps, 1.5mA typ.
  5.0V, 64kbps, 4.0mA typ.
- **Low Current Non-DSP Solution**
- **Small TSSOP size fits PCMCIA / PC CARDs**

Applications

- **Portable Wireless Data Applications**
  Cellular Digital Packet Data (CDPD)
  Mobitex™ Mobile Data System
- **Spread Spectrum Data Links**
- **GPS/Differential GPS Wireless Links**
- **Point of Sale Terminals**
- **Low Power Wireless Data Link for PCs, Laptops, and Printers**


TX ENABLE
TX PS
TX DATA
XTAL/CLOCK
XTAL
ClkDIVA
ClkDIVB
BT
V_DD
RXHold
PLLacq
RXDCacq
RX PS
RX SIGNAL IN
RX FEEDBACK
DATA RETIME & LEVEL SHIFT
V_BIAS
TX FILTER
V_BIAS
TX OUT
TX CLK
CLOCK DIVIDER
RX DATA DETECTION
RX DATA
RX S/N DETECTION
RX S/N
RX CIRCUIT CONTROL
RX CLOCK
RX CLK
V_BIAS
+
-
RX FILTER
RX DC LEVEL MEASURE
DOC1
DOC2
V_SS
V_BIAS

The CMX589A is a single-chip synchronous data pump/modem designed for Wireless Data Applications. Employing Gaussian filtering for Minimum shift Keying (GMSK) baseband modulation applications, the CMX589A features a wide range of available data rates from 4k to 200kbps. Data Rates and the choice of BT (0.3 or 0.5) are pin programmable to provide for different system requirements.

The Tx and Rx digital data interfaces are bit serial, synchronized to generated Tx and Rx data clocks. Separate Tx and Rx Powersave inputs allow full or half-duplex operation. Rx input levels can be set by suitable AC and DC level adjusting circuitry built with external components around an on-chip Rx Input Amplifier.

Acquisition, Lock, and Hold of Rx data signals are made easier and faster by the use of Rx Control Inputs to clamp, detect, and /or hold input data levels and can be set by the µProcessor as required. The Rx S/N output provides an indication of the quality of the received signal.

The CMX589A may be used with a 3.0V to 5.5V power supply and is available in the following packages: 24-pin TSSOP (CMX589AE2), 24-pin SSOP (CMX589AD5), 24-pin SOIC (CMX589AD2), and 24-pin PDIP (CMX589AP4).

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- 4.2 Receive .... 3 - 41
  - 4.2.1 Rx Signal Path Description .... 3 - 41
  - 4.2.2 Rx Circuit Control Modes .... 3 - 42
  - 4.2.3 Rx Clock Extraction .... 3 - 43
  - 4.2.4 Rx Data Extraction .... 3 - 43
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1 Block Diagram

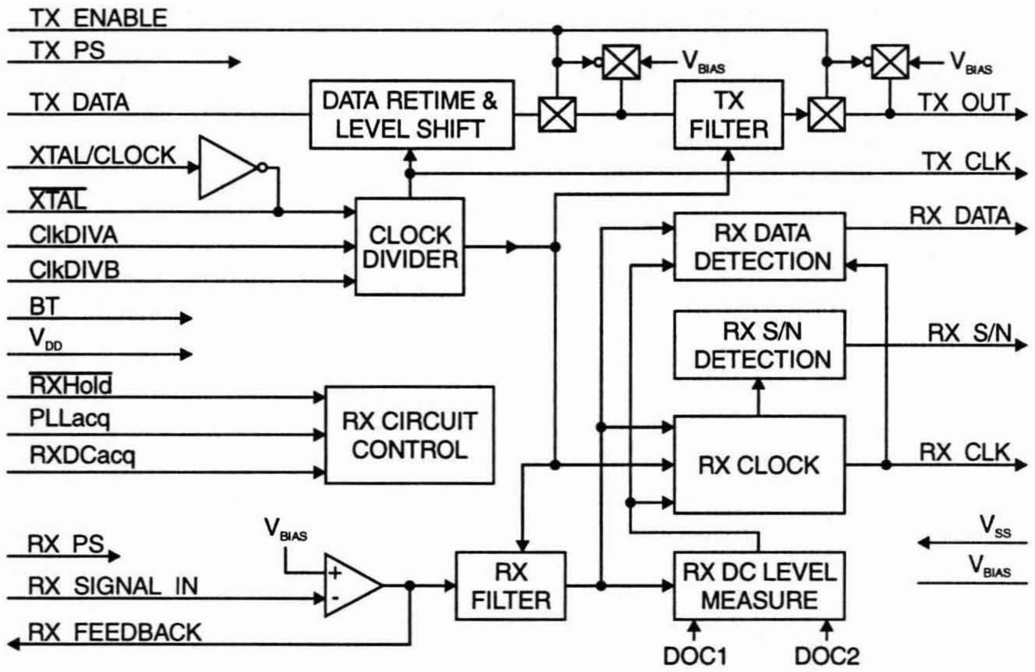

TX ENABLE
TX PS
TX DATA
XTAL/CLOCK
XTAL
ClkDIVA
ClkDIVB
BT
V_{DD}
RXHold
PLLacq
RXDCacq
RX PS
RX SIGNAL IN
RX FEEDBACK
V_{BIAS}
DATA RETIME & LEVEL SHIFT
CLOCK DIVIDER
RX CIRCUIT CONTROL
TX FILTER
RX FILTER
RX DATA DETECTION
RX S/N DETECTION
RX CLOCK
RX DC LEVEL MEASURE
DOC1
DOC2
TX OUT
TX CLK
RX DATA
RX S/N
RX CLK
V_{SS}
V_{BIAS}

Figure 1: Block Diagram

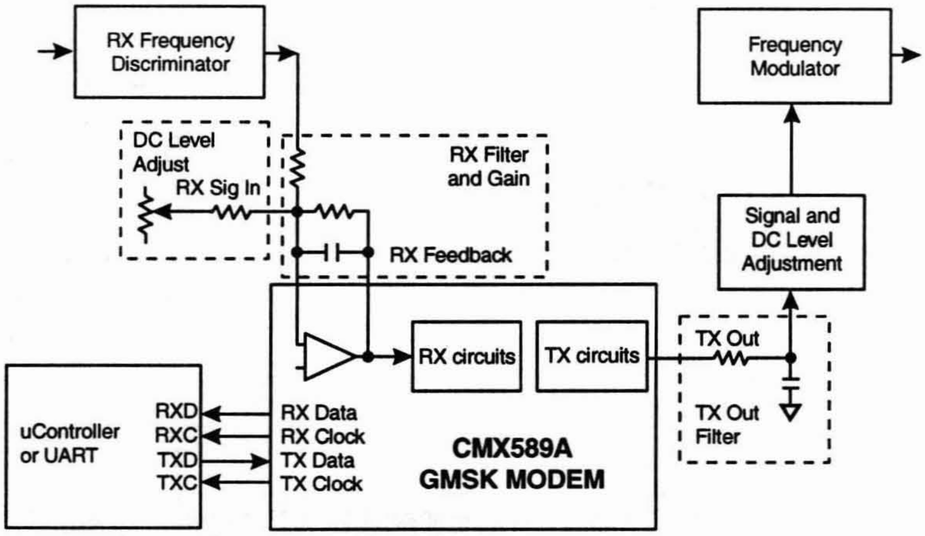

RX Frequency Discriminator
DC Level Adjust
RX Sig In
RX Filter and Gain
RX Feedback
RX circuits
TX circuits
CMX589A GMSK MODEM
uController or UART
RXD
RXC
TXD
TXC
RX Data
RX Clock
TX Data
TX Clock
TX Out
TX Out Filter
Signal and DC Level Adjustment
Frequency Modulator

Figure 2: System Block Diagram

2 Signal List

Pin No. E2/D5/ D2/P4	Signal	Type	Description
1	$\overline{\text{XTAL}}$	output	The output of the on-chip clock oscillator.
2	XTAL/CLOCK	input	The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{\text{XTAL}}$ pin left unconnected. Note: Operation without a suitable Xtal or clock input may cause device damage.
3	ClkDivA	input	Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 4.
4	ClkDivB	input	Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 4.
5	$\overline{\text{Rx HOLD}}$	input	A logic 0 applied to this input will freeze the Clock Extraction and Level Measurement circuits unless they are in 'Acquire' mode.
6	RxDCacq	input	A logic 1 applied to this input will set the RX Level Measurement circuitry to the Acquire mode.
7	PLLacq	input	A logic 1 applied to this input will set the RX Clock Extraction circuitry to the 'Acquire' mode. See Table 6.
8	Rx PSAVE	input	A logic 1 applied to this input will powersave all receive circuits except for RX CLK output (which will continue at the set bit-rate) and cause the RX Data and RX S/N outputs to go to a logic 0.
9	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the pin.
10	Rx FB		Output of the RX Input Amplifier.
11	Rx Signal In	input	Input to RX input amplifier.
12	V_{SS}	power	Negative supply (GND).
13	DOC1		Connections to the RX Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}.
14	DOC2		Connections to the RX Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}.
15	BT		A logic level to select the modem BT (the ratio of the TX Filter's -3dB frequency to the Bit-Rate). A logic 1 = BT of 0.5 and a logic 0 = BT of 0.3.
16	Tx Out	output	Gaussian filtered TX output signal. In powersave mode the Tx Out pin is a high impedance open.
17	Tx Enable	input	A logic 1 applied to this input, enables the transmit data path, through the TX Filter to the TX Out pin. A logic 0 will place the TX Out pin to V_{BIAS} via a high impedance.
18	Tx PSAVE	input	A logic 1 applied to this input will powersave all transmit circuits except for the TX Clock.
19	Tx Data	input	The logic level input for the data to be transmitted. This data should be synchronous with TX CLK.
20	Rx Data	output	A logic level output carrying the received data, synchronous with RX CLK.
21	Rx CLK	output	A logic level clock output at the received data bit-rate.
22	Tx CLK	output	A logic level clock output at the transmit-data rate.

Pin No. E2/D5/ D2/P4	Signal	Type	Description
23	Rx S/N	output	A logic level output which may be used as an indication of the quality of the received signal.
24	V_{DD}	power	Positive supply. Levels and voltages within the device are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the pin.

Table 1: Signal List

3 External Components

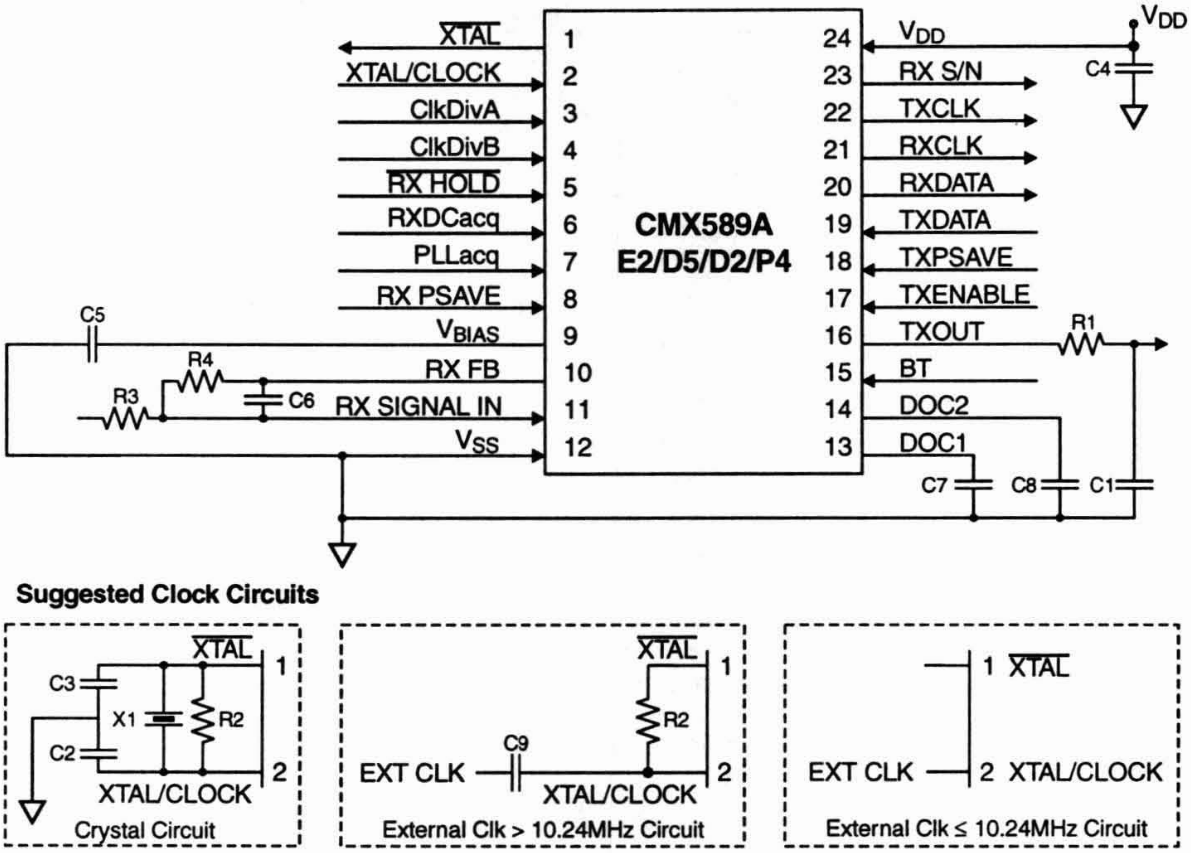

XTAL
XTAL/CLOCK
ClkDivA
ClkDivB
RX HOLD
RXDCacq
PLLacq
RX PSAVE
VBIAS
RX FB
RX SIGNAL IN
VSS
CMX589A
E2/D5/D2/P4
VDD
RX S/N
TXCLK
RXCLK
RXDATA
TXDATA
TXPSAVE
TXENABLE
TXOUT
BT
DOC2
DOC1
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
C4
C5
R4
R3
C6
R1
C7
C8
C1
Suggested Clock Circuits
C3
X1
R2
C2
XTAL
XTAL/CLOCK
Crystal Circuit
EXT CLK
C9
External Clk > 10.24MHz Circuit
1 XTAL
2 XTAL/CLOCK
External Clk ≤ 10.24MHz Circuit

Figure 3: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±5%
R2		1.0MΩ	±10%
R3	2		±10%
R4	3		±10%
C1	1		±10%
C2	4		
C3	4		

Component	Notes	Value	Tolerance
C4		0.1µF	±20%
C5		1.0µF	±20%
C6	5		±20%
C7	6		
C8	6		
C9	7	100pF	
X1	8		

Table 2: Recommended External Components

Recommended External Component Notes:

1. The RC network formed by R1 and C1 is required between the TX Out pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance and the capacitance is:

   For a BT of 0.3 R1C1 = 0.34/bit rate (bps)
   For a BT of 0.5 R1C1 = 0.22/bit rate (bps)

Data Rates (kbps)	BT = 0.3		BT = 0.5	
	R1	C1	R1	C1
4	120kΩ	680pF	120kΩ	470pF
4.8	100kΩ	680pF	100kΩ	470pF
8	91kΩ	470pF	120kΩ	220pF
9.6	91kΩ	390pF	47kΩ	470pF
16	47kΩ	470pF	91kΩ	150pF
19.2	100kΩ	180pF	91kΩ	120pF
32	47kΩ	220pF	47kΩ	150pF
38.4 *	47kΩ	180pF	47kΩ	120pF
64 *	56kΩ	100pF	51kΩ	68pF
80 *			39kΩ	68pF
128 *			82kΩ	22pF
144 *			68kΩ	22pF
160 *			62kΩ	22pF
176 *			56kΩ	22pF
192 *			51kΩ	22pF

* $V_{DD} \geq 4.5V$, external clock

Table 3: Data Rate vs. BT and Selected External Component Values

Note: In all cases, the value of R1 should not be less than 20.0kΩ, and that the calculated value of C1 includes calculated parasitic capacitance.

2. R3, R4 and C6 form the gain components for the RX Input signal. R3 should be chosen as required by the signal input level.
3. For bit rate ≤ 64kbps, R4 = 100kΩ. For bit rate > 64kbps, R4 = 10kΩ.
4. The values chosen for C2 and C3 (including stray capacitance) should be suitable for the applied V_{DD} and the frequency of X1.
   As a guide: C2 = C3 = 33pF at 1.0MHz falling to 18pF at the maximum frequency.
   At 3.0V, C2 = C3 = 33pF falling to 18pF at 5.0MHz the equivalent series resistance of X1 should be less than 2.0KΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimized.
5. For bit rate ≤ 64kbps, C6 = 22pF. For bit rate > 64kbps, $C6 = \dfrac{1}{3 \times \text{bit rate} \times 2\pi \times 10\text{k}\Omega}$ e.g. for 128kbps, C6 = 41.1pF.
6. C7 and C8 should both be .015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 0.030µF at 4kbps, 1800pF at 64kbps, 680pF at 192kbps.
7. The tolerance of C9 is not very critical because it primarily serves as a DC blocking capacitor.
8. The CMX589A can operate correctly with the Xtal/Clock frequencies between 1.0MHz and 8.2MHz (V_{DD} = 5.0V) and 1.0MHz to 5.0MHz (V_{DD} = 3.0V). External clock frequencies up to 25.6MHz ($V_{DD} \geq$ 4.5V) are also supported. (See Table 4 for examples.) For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4 General Description

4.1 Clock Oscillator Divider

The TX and (nominal) RX data rates are determined by division of the frequency present at the $\overline{\text{Xtal}}$ pin as generated by the on-chip Xtal oscillator, with external components, or supplied from an external source.

The division ratio is controlled by the logic level inputs on ClkDivA and ClkDivB pins as shown in Table 4, together with an indication of how various standard data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clk Frequency}}{\text{Division Ratio (ClkDiv A/B)}}$$

			Xtal/Clock Frequency (MHz)					
			24.576*	8.192	4.9152	4.096	2.4576	2.048
Inputs						12.288/3	12.288/5	6.144/3
ClkDivA	ClkDivB	Xtal/Clk Freq / Data Rate	Data Rate (kbps)					
0	0	128	192*	64*	38.4*	32	19.2	16
0	1	256	96*	32	19.2	16	9.6	8
1	0	512	48*	16	9.6	8	4.8	4
1	1	1024	24*	8	4.8	4		

* $V_{DD} \geq 4.5V$

Table 4: Example Clock/Data Rates

Note: The device operation is not guaranteed above 200kbps or below 4kbps at the relevant supply voltage.

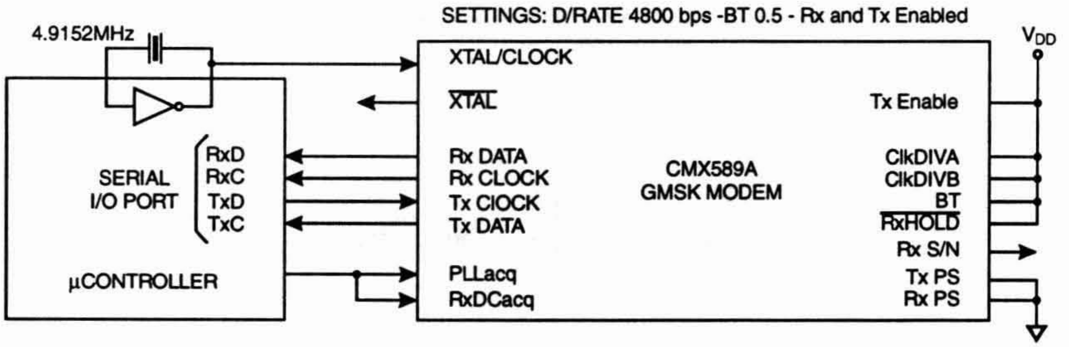

SETTINGS: D/RATE 4800 bps -BT 0.5 - Rx and Tx Enabled
4.9152MHz
V_{DD}
XTAL/CLOCK
$\overline{\text{XTAL}}$
Tx Enable
SERIAL
I/O PORT
RxD
RxC
TxD
TxC
Rx DATA
Rx CLOCK
Tx ClOCK
Tx DATA
CMX589A
GMSK MODEM
ClkDIVA
ClkDIVB
BT
$\overline{\text{RxHOLD}}$
Rx S/N
µCONTROLLER
PLLacq
RxDCacq
Tx PS
Rx PS

Figure 4: Minimum µController System Connections

4.2 Receive

4.2.1 Rx Signal Path Description

The function of the RX circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide RX data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the CMX589A's RX Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip RX Input Amplifier. The gain should be set so that the signal level at the RX Feedback pin is nominally 1V peak to peak (for V_{DD}=5.0V) centered around V_{BIAS} when receiving a continuous 1111000011110000.. data pattern.

Positive going signal excursions at RX Feedback pin will produce a logic 0 at the RX Data Output. Negative going excursions will produce a logic 1.

The received signal is fed through the lowpass RX Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the positive parts of the received signal. The other measures the amplitude of the negative portions. (Positive refers to signal levels higher than $V_{DD}/2$, and negative to levels lower than $V_{DD}/2$.) External capacitors are used by these detectors, via the Doc1 & Doc2 pins, to form voltage 'hold' or 'integrator' circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the RX signal amplitude and any DC offset.

4.2.2 Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 6, by logic level inputs applied to the PLLacq, $\overline{\text{Rx HOLD}}$, and RxDCacq pins to suit a particular application, or to cope with changing reception conditions, reference Figure 5.

In general, a data transmission will begin with a preamble, for example, 1100110011001100, to allow the receive modem to establish timing and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the RxDCacq and PLLacq Inputs should be switched from a logic 0 to a logic 1 so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The $\overline{\text{Rx HOLD}}$ input should normally be held at a logic 1 while data is being received, but may be driven to a logic 0 to freeze the Level Measuring Clock Extraction circuits during a fade. If a fade lasts for less than 200 bit periods, normal operation can be resumed by returning the $\overline{\text{Rx HOLD}}$ input to a logic 1 at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the RxDCacq to a logic 1 for 10 to 20 bit periods.

$\overline{\text{Rx HOLD}}$ has no effect on the Level Measuring circuits while RxDCacq is at a logic 1, and has no effect on the PLL while PLLacq is at a logic 1.

A logic 0 on $\overline{\text{Rx HOLD}}$ does not disable the Rx Clock output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

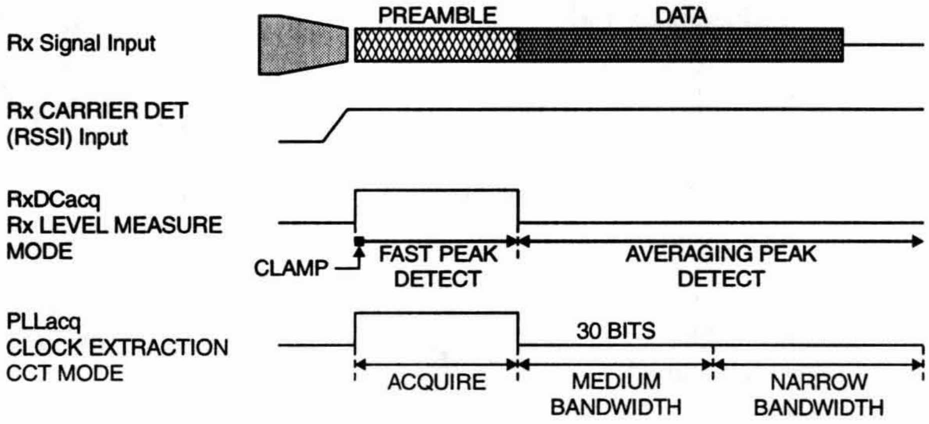


Figure 5: Rx Mode Control Diagram

PLLacq	$\overline{\text{RxHOLD}}$	PLL Action	
1	1	Acquire	Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic "1".
1 to 0	1	Medium Bandwidth	The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a 1 to 0 transition of the PLLacq input, provided that the $\overline{\text{Rx HOLD}}$ input is a logic 1.
0	1	Narrow Bandwidth	The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the $\overline{\text{Rx HOLD}}$ Input is a logic 1 and PLLacq has been a logic 0 for at least 30 bit periods (after Medium Bandwidth operation for instance).
0	0	Hold	The PLL feedback loop is broken, allowing the RX Clock to freewheel during signal fade periods.

Table 5: PLL Action Measurement Operational Modes

RxDCacq	$\overline{\text{RxHOLD}}$	Rx Level Measure Action	
0 to 1	X	Clamp	Operates for one bit-time after a 0 to 1 transition of the RXDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5 bit-time.
1	X	Fast Peak Detect	The voltage detectors act as peak-detectors, one capacitor is used to capture the positive-going signal peaks of the RX Filter output signal and the other capturing the negative-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic 1, except for the initial 1-bit Clamp-mode time.
0	1	Averaging Peak Detect	Provides a slower but more accurate measurement of the signal peak amplitudes.
0	0	Hold	The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

X = Do not care

Table 6: Rx Level Measurement Operational Modes

4.2.3 Rx Clock Extraction

Synchronized by a PLL circuit to zero-crossings of the incoming data, the Rx Clock Extraction circuitry controls the Rx Clock output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the Rx Circuit Control inputs PLLacq and $\overline{\text{Rx HOLD}}$ to operate in one of four PLL modes as described in Table 5 and Table 6.

4.2.4 Rx Data Extraction

The RX Data Extraction circuit decides whether each received bit is a 1 or 0 by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the Level Measuring circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter. Extracted data is output from the RX Data pin, and should be sampled externally on the rising edge of the RX CLK.

4.2.5 Rx S/N Detection

The RX S/N Detector system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the RX S/N pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output, it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

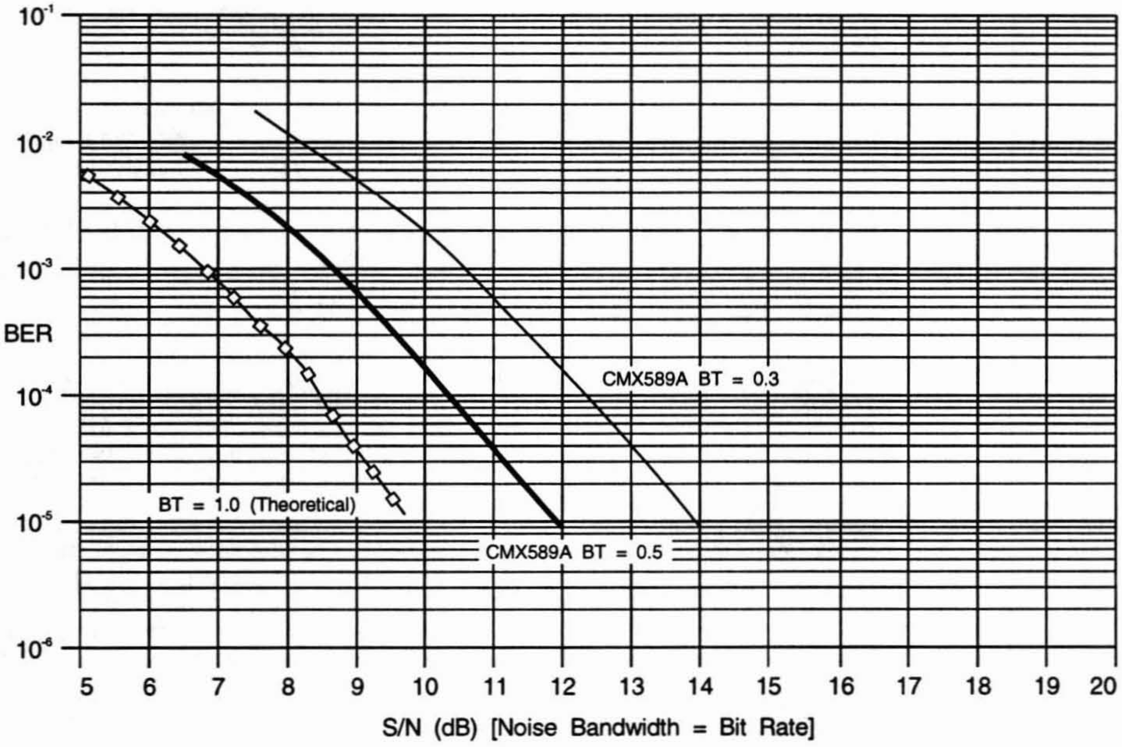


Figure 6: Typical Bit-Error-Rate Performance

Note: Figure 6 indicates typical performance, independent of bit rate (although the applied noise bandwidth is considered to match the bit rate used), radio performance (e.g. IF filter distortion), supply voltage (higher bit rates require $V_{DD} \geq 4.5V$), and other 'real world' factors."

4.2.6 Rx Signal Quality

The effect of input Rx Signal quality on the Rx S/N output is shown in Figure 7.

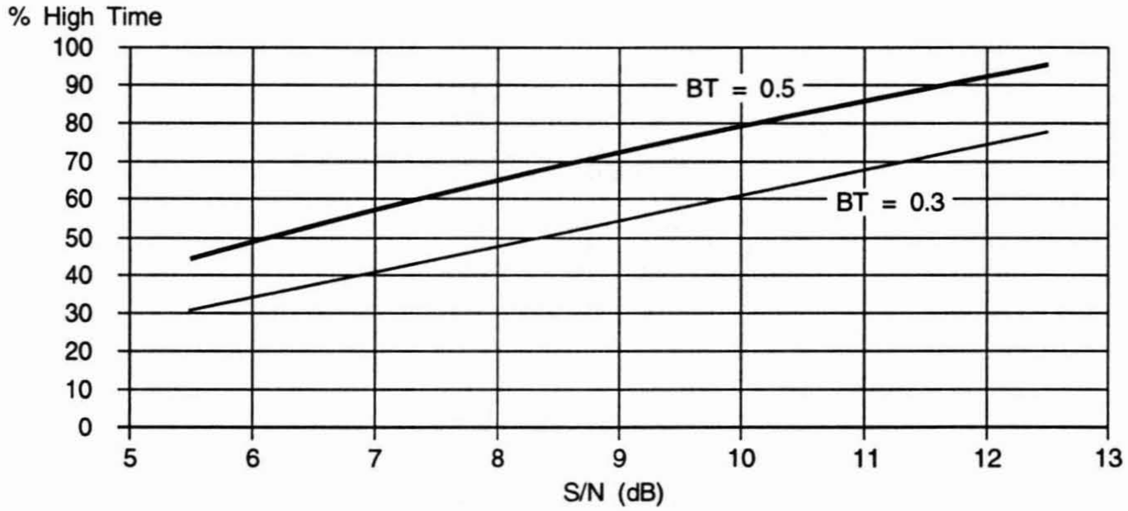


Figure 7: Typical Rx S/N Output High time (%) vs. Input S/N

4.3 Transmit

4.3.1 TX Signal Path Description

The binary data applied to the TX Data input is retimed within the chip on each rising edge of the TX Clock and then converted to a 1-volt peak-to-peak binary signal centered at V_{BIAS} (for V_{DD}= 5.0V)

If the TX Enable input is high, then this internal binary signal will be connected to the input of the lowpass TX Filter, and the output of the filter connected to the TX Out pin.

Tx Enable	Tx Filter Input	Tx Out Pin
1	Data @ $\frac{V_{DD}}{5}$ V_{P-P} e.g. 1V_{P-P} for V_{DD}=5V	Filtered 'Tx Filter Input'
0	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the TX Enable will connect the input of the TX Filter to V_{BIAS}, and disconnect the TX Out pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The TX Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs.-frequency response of the transmit filtering provided by the CMX589A has been designed to meet the specifications for most GMSK modem systems that are -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note: An external RC network is required between the TX Out pin and the input to the Frequency Modulator (see Figure 2 and Figure 3). This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The signal at Tx Out is centered around V_{BIAS}, going positive for logic 1 (high) level inputs to the Tx Data input and negative for logic 0 (low) inputs.

When the transmit circuits are put into a powersave mode (by a logic 1 to the Tx PS pin) the output voltage of the Tx Filter will go to high impedance. When power is subsequently restored to the Tx filter, its output will take several bit-times to settle. The Tx Enable input can be used to prevent these abnormal voltages from appearing at the Tx Out pin.

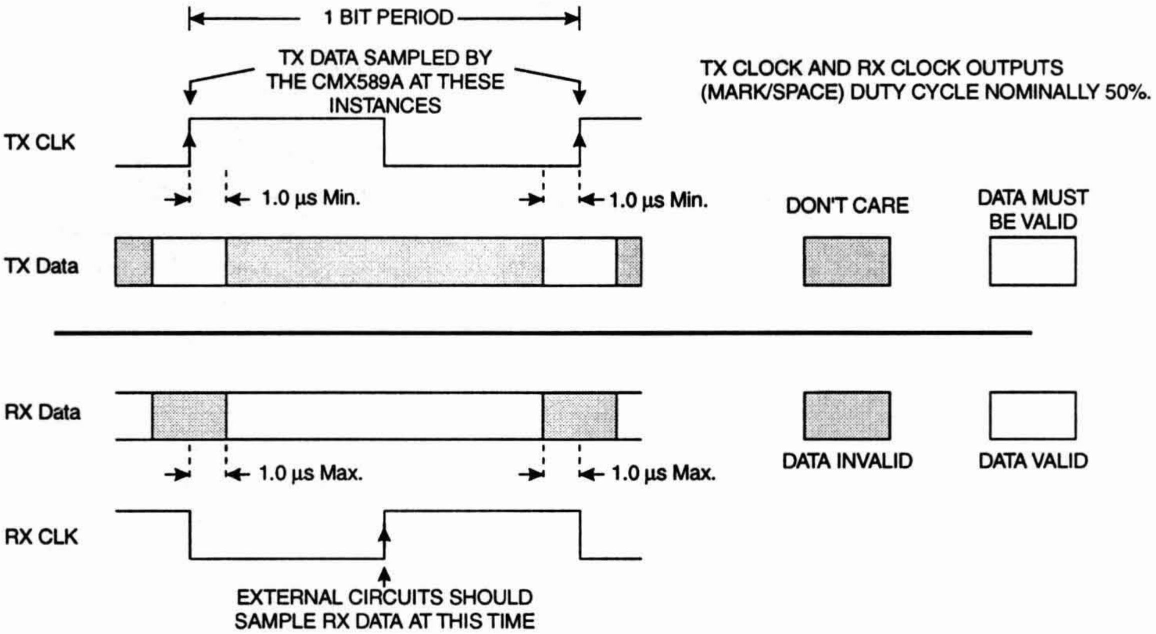

1 BIT PERIOD
TX DATA SAMPLED BY THE CMX589A AT THESE INSTANCES
TX CLOCK AND RX CLOCK OUTPUTS (MARK/SPACE) DUTY CYCLE NOMINALLY 50%.
TX CLK
1.0 µs Min.
1.0 µs Min.
DON'T CARE
DATA MUST BE VALID
TX Data
RX Data
DATA INVALID
DATA VALID
1.0 µs Max.
1.0 µs Max.
RX CLK
EXTERNAL CIRCUITS SHOULD SAMPLE RX DATA AT THIS TIME

Figure 8: Rx and Tx Clock Data Timings

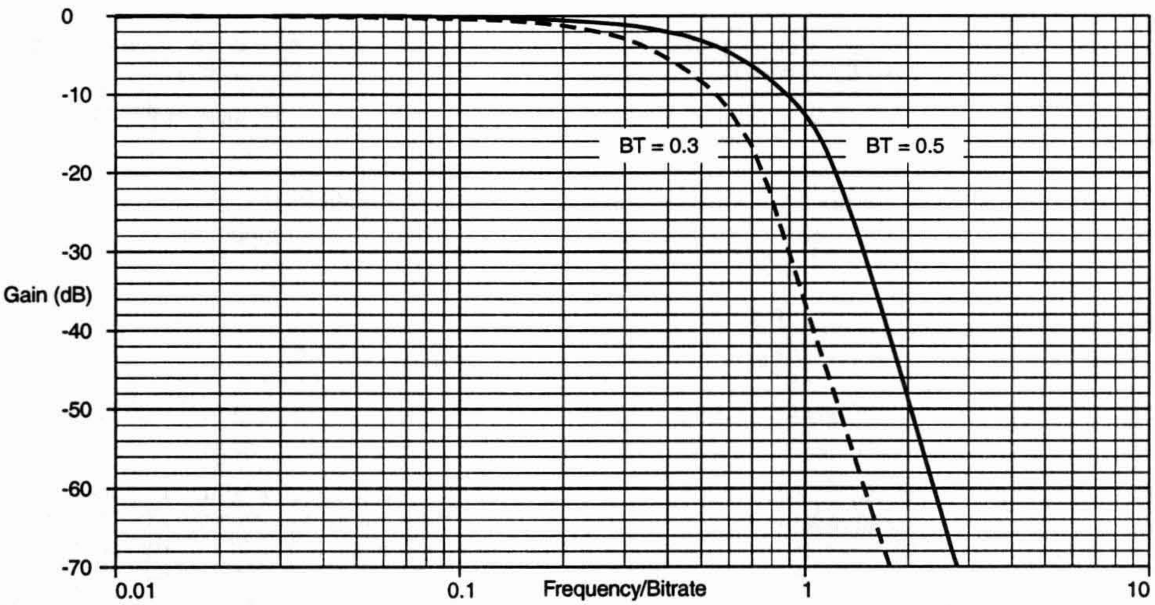


Figure 9: Tx Filter Response

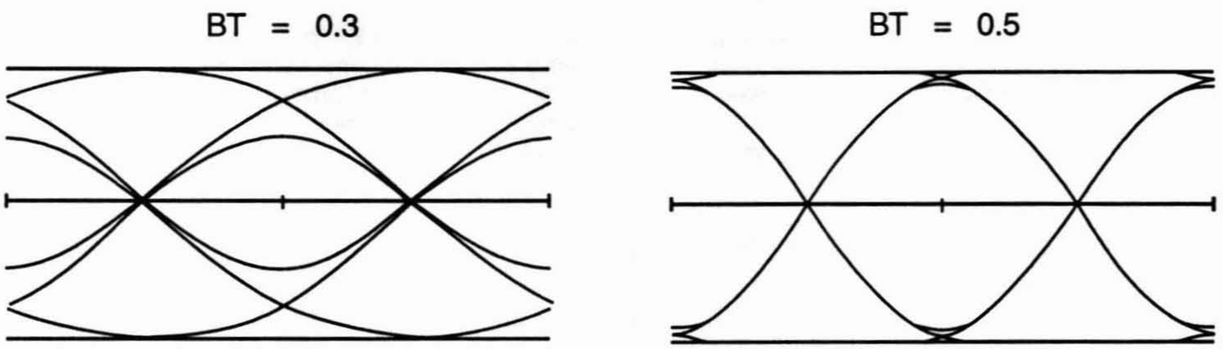


Figure 10: Typical Transmit Eye Patterns

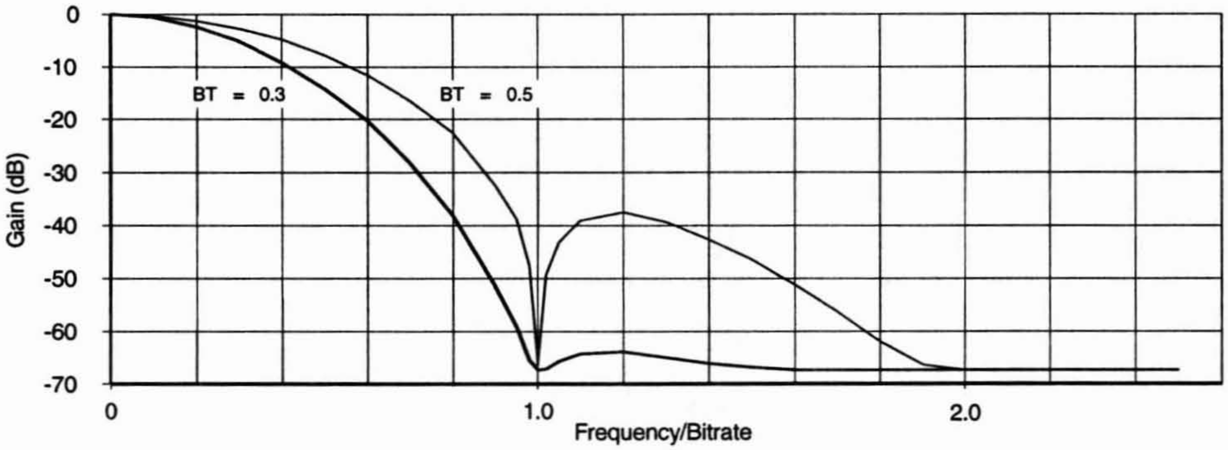


Figure 11: Tx Output Spectrum (Random Data)

4.4 Data Formats

The receive section of the CMX589A works best with data which has a reasonably random structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (>100 bits) of consecutive ones or zeroes. Also, long sequences (>100 bits) of 10101010 ... patterns should be avoided.

For this reason, it is recommended that data be made random in some manner before transmission, for example by exclusive-ORing it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT=0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of ones and zeros i.e. 110011001100....; the eye of pattern 10101010 .... has the most gradual slope and will yield poor peak levels for the RX circuits. For BT=0.5 the eye pattern of 10101010... has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 6.

4.5 Acquisition and Hold Modes

The RXDCacq and PLLacq inputs must be pulsed High for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, the above inputs should be taken Low again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the remote transmitter is turned on.

The CMX589A can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}, (measured at the RX Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the Low to High transition of the RXDCacq and PLLacq inputs should occur after the mean input voltage to the CMX589A has settled to within about 0.1V of its final value.

Note: This can place restrictions on the value of any series signal coupling capacitor.

As well as using the RX Hold input to freeze the Level Measuring and Clock Extraction circuits during a signal fade, it may also be used in systems which use a continuously transmitting control channel to freeze the RX circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the CMX589A Xtal clock needs to be accurate enough that the derived RXClock output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the RXHold input is 'Low'.

However; the RXDCacq input may need to be pulsed High for 2 bit durations to re-establish the level measurements if the RXHold input is Low for more that a few hundred bit-times (exact number depends on system crystal tolerances).

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note: These pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

5 Application

5.1 Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required. For optimum channel utilization, (e.g. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

5.1.1 Bit Rate, BT, and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing
Allowable adjacent channel interference
TX filter bandwidth
Peak carrier deviation (Modulation Index)
TX and RX carrier frequency accuracies
Modulator and Demodulator linearity
RX IF filter frequency and phase characteristics
Use of error correction techniques
Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable - depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx & Rx carrier frequencies. Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4.8kbps would allow the BT to be increased to 0.5, improving the error-rate performance.

5.1.2 FM Modulator, Demodulator and IF

For optimum performance, the eye pattern of the received signal (when receiving random data) applied to the CMX589A should be as close as possible to the Transmit eye pattern examples shown in Figure 10.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to:

Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.

Bandwidth & phase response of the RX IF filters.

Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be DC coupled to the CMX589A RX Signal In pin (with a DC bias added to center the signal at the RX Feedback pin at $V_{DD}/2$ [V_{BIAS}]). However, AC coupling can be used provided that:

The 3dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).

The data does not contain long sequences of consecutive ones or zeroes.

Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a RF carrier) for the voltage into the CMX589A to settle before the RXDCacq line is strobed.

5.1.3 Two-Point Modulation

When designing the CMX589A into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to DC.

Figure 12 shows a suggested basic configuration to provide a two-point modulation drive from the CMX589A TX Output using MX-COM's MX019 Digitally Controlled Quad Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the MX019 is via an 8-bit data word. Note that the MX019 frequency response supports data rates as high as 8kbps.

With reference to Figure 12:

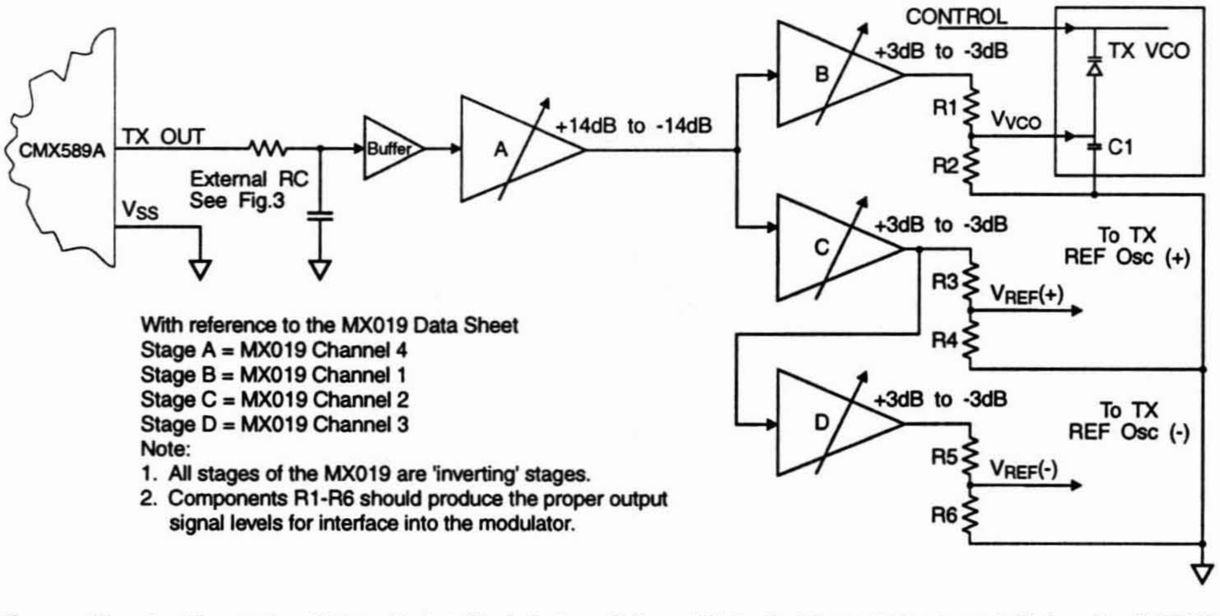
The buffer amplifier is required to prevent loading of the CMX589A external RC circuit.

Stage B, with R1/R2, provides suitable signal and DC levels for the VCO varactor; C1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R3/R4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum AC signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required.

Stage A provides buffering and overall level control.



With reference to the MX019 Data Sheet
Stage A = MX019 Channel 4
Stage B = MX019 Channel 1
Stage C = MX019 Channel 2
Stage D = MX019 Channel 3
Note:
1. All stages of the MX019 are 'inverting' stages.
2. Components R1-R6 should produce the proper output signal levels for interface into the modulator.

Figure 12: An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019

5.2 AC Coupling of Tx and Rx Signals

In practical applications, it is possible to arrange AC coupling between the CMX589A Tx Output and the frequency modulator to cut-off at a very low frequency, such as 5.0Hz. AC coupling between the receive discriminator and the input of the CMX589A may need a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum –3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.0Hz in the Rx path.

Figure 13 shows the typical static Bit-Error-Rate performance of the CMX589A operating under nominal conditions for various degrees of AC coupling at the Rx input and the Tx output.

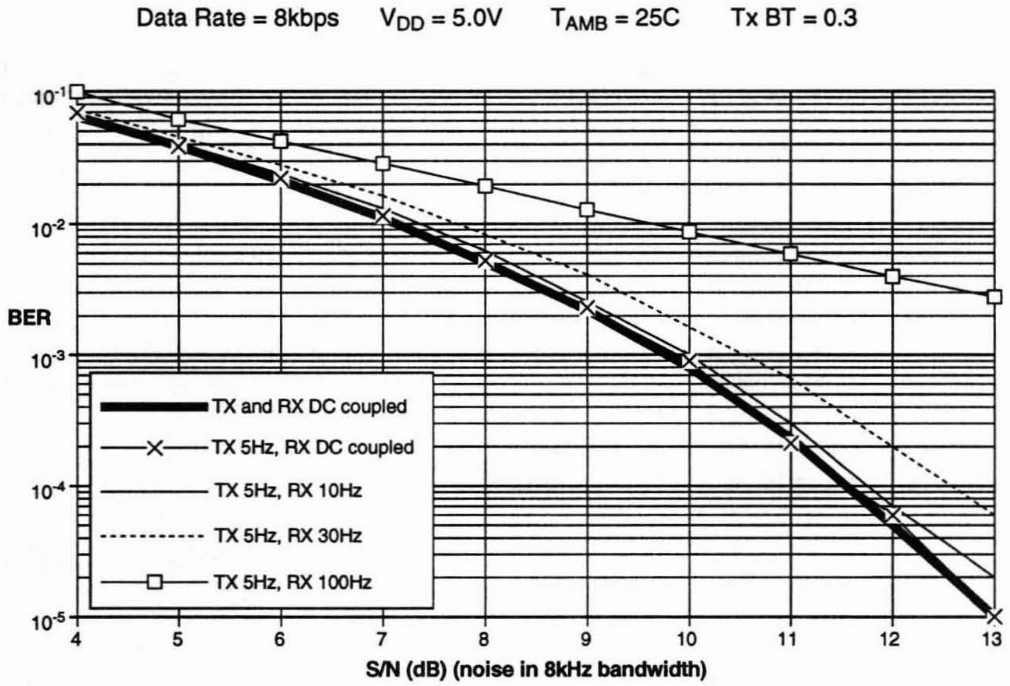


Figure 13: Effect of AC Coupling on Typical Bit-Error Rate

Any AC Coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 14, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = \frac{1}{2\pi(\text{the 3dB cutoff frequency of the RC network})}$$

which is 32ms, or 256 bit times at 8kbps, for a 5Hz network.

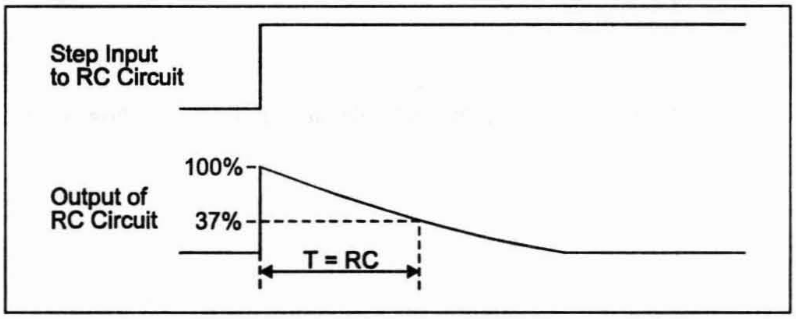


Figure 14: Decay time-AC Coupling

6 Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
D2 / P4 Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			13		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
D5 / E2 Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				550	mW
Derating above 25°C			9		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 7: Absolute Maximum Ratings

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		3.0	3.3/5.0	5.5	V
Operating Temperature		-40		85	°C
Rx and Tx Data Rate					
$V_{DD} \geq 3.0V$		4		32	kbps
$V_{DD} \geq 4.5V$		4		200	kbps
Xtal Frequency					
$V_{DD} \geq 3.0V$		1.0		5.0	MHz
$V_{DD} \geq 4.5V$		1.0		25.6	MHz
High Pulse Width	1	15			ns
Low Pulse Width	1	15			ns

Table 8: Operating Limits

Operating Limits Notes

1. Timing for an external clock input to the Xtal/Clock pin.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.096MHz, Data Rate = 8kbps, Noise Bandwidth = Bit Rate

Static Values			**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Current	Tx PS	Rx PS	1				
I_{DD} (V_{DD} = 3.0V)							
	1	1			0.5		mA
	0	1			1.0		mA
	1	0			1.0		mA
	0	0			1.5		mA
I_{DD} (V_{DD} = 5.0V)							
	1	1			1.0		mA
	0	1			2.0		mA
	1	0			3.0		mA
	0	0			4.0		mA
Input Logic Level							
Logic 1 Input Level				3.5			V
Logic 0 Input Level						1.5	V
Logic Input Current			2	-5.0		5.0	µA
Output Logic Level							
Logic 1 Output Level (I_{OH} = 120µA)				4.6			V
Logic 0 Output Level (I_{OL} = -120µA)						0.4	V
Transmit Parameters							
Tx OUT pin DC bias shift caused by change from Tx Enable = 0 to Tx Enable = 1 while Tx PSAVE = 0 at 25°C				-85		85	mV
Tx OUT, Output Impedance			3		1.0		kΩ
Tx Out, Level			4, 10	0.8	1.0	1.2	V_{P-P}
Output DC Offset			12	-0.125		0.125	V
Tx Data Delay							
BT = 0.3			5		2.0	2.5	bit-periods
BT = 0.5			5		1.5	2.0	bit-periods
Tx PS to Output-Stable time			6		4.0		bit-periods
Receive Parameters							
Rx Amplifier							
Input Impedance				1.0			MΩ
Output Impedance			7		10.0		KΩ
Voltage Gain					50.0		dB
Rx Filter Signal Input Level			8, 10	0.7	1.0	1.3	V_{P-P}
Rx Time Delay			9			3.0	bit-periods

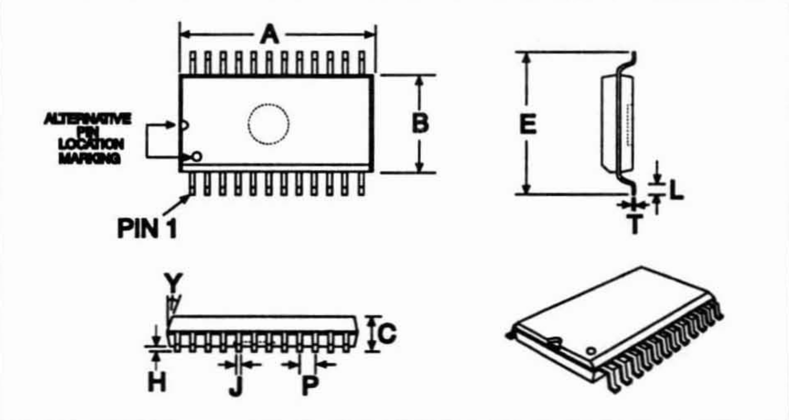
Static Values	Notes	Min.	Typ.	Max.	Units
On-Chip Xtal Oscillator					
R_{IN}		10.0			MΩ
R_{OUT}	11		50.0		kΩ
Voltage Gain	11		25.0		dB

Table 9: Operating Characteristics

Operating Characteristics Notes:

1. Not including current drawn from the CMX589A pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3. For a load of 10KΩ or greater. Tx PS input at logic 0; Tx Enable = 1.
4. Data pattern of 1111000011110000…
5. Measured between the rising edge of Tx Clock and the center of the corresponding bit at Tx Out.
6. Time between the falling edge of the Tx PS and the Tx Out voltage stabilizing to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic 0.
8. For optimum performance, Measured at the Rx Feedback pin for an 1111000011110000… pattern.
9. Measured between the center of bit at Rx Signal In and corresponding rising edge of the Rx Clock.
10. Levels are proportional to applied V_{DD}
11. Small signal measurement at 1.0kHz with no load on Xtal output.
12. (Tx OUT enabled DC level) – (Tx Out disabled DC level) when transmitting a repeating 11110000 bit pattern.

6.2 Packages

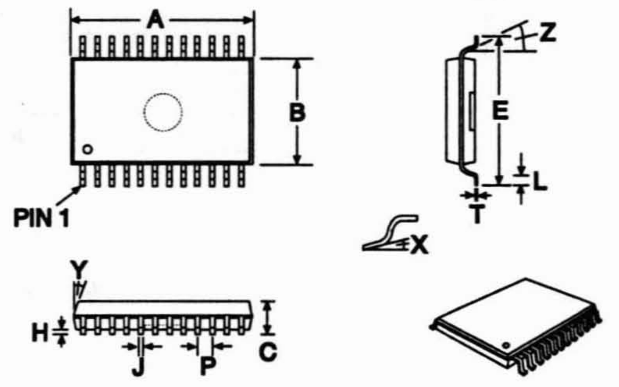


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin TSSOP Mechanical Outline: ***Order as part no. CMX589AE2***

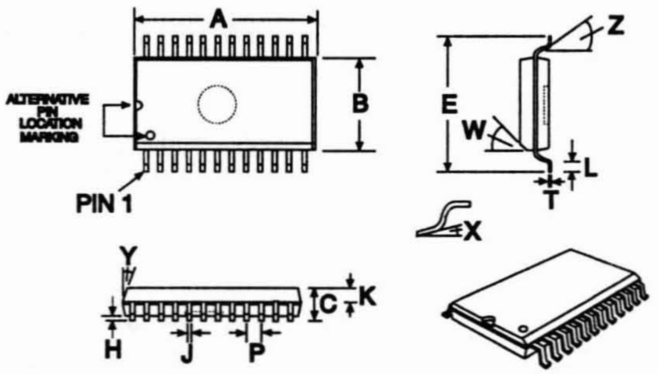


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin SSOP Mechanical Outline: ***Order as part no. CMX589AD5***

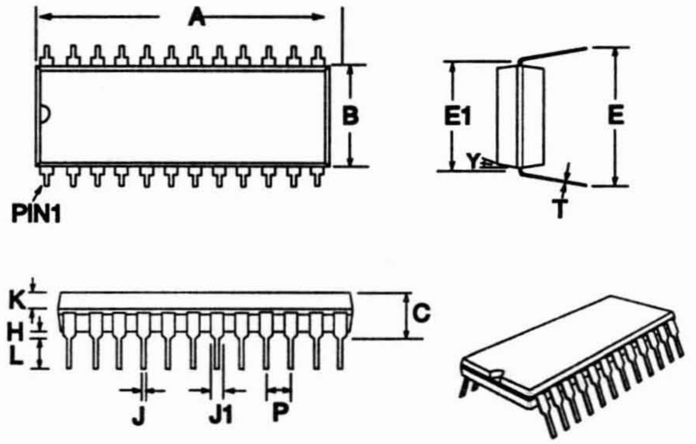


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin SOIC Mechanical Outline: ***Order as part no. CMX589AD2***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 18: 24-pin PDIP Mechanical Outline: ***Order as part no. CMX589AP4***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX602A

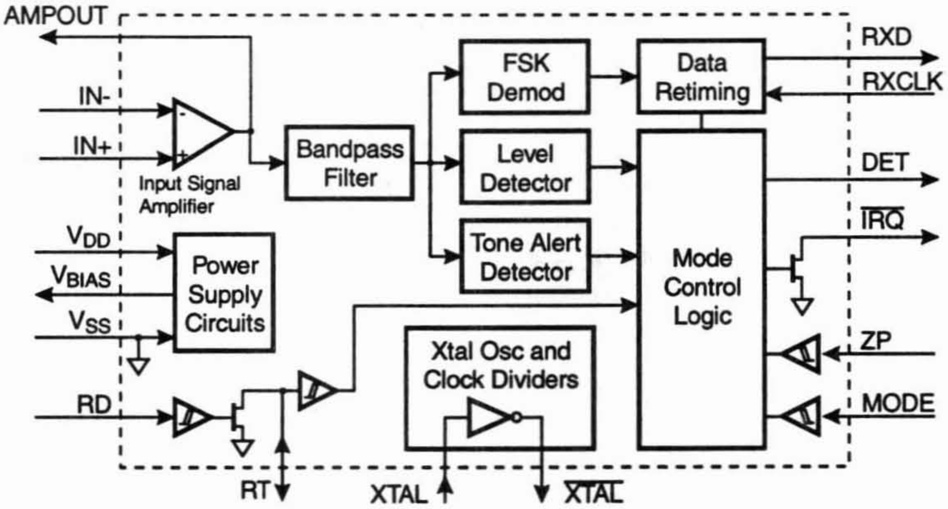
PRELIMINARY INFORMATION

Features

- Automatic CAS Dual Tone Detector
  High Sensitivity, Low Falsing
  Automatic CAS Duration Checking
- 1µA max. 'Zero-Power' Ring or Line Polarity Reversal Detector
- V23/Bell202 FSK Demodulator with Data Retiming facility
- µC Interrupt / Wake-up output to minimize system operating power
- Low Power Operation 0.5mA at 2.7V_{DD}

Applications

- Caller ID/Caller ID on Call Waiting
  Telephones
  Adjunct Boxes
- Bellcore, ETSI, British Telecom, and Mercury Systems
- Computer Telephone Integration
- Call Logging Systems
- Voice Mail Equipment


AMPOUT
IN-
IN+
Input Signal Amplifier
Bandpass Filter
FSK Demod
Level Detector
Tone Alert Detector
Data Retiming
Mode Control Logic
RXD
RXCLK
DET
IRQ
ZP
MODE
VDD
VBIAS
VSS
Power Supply Circuits
RD
RT
Xtal Osc and Clock Dividers
XTAL
XTAL

The CMX602A is a low power CMOS device used for the reception of physical layer signals in Bellcore's Calling Identity Delivery (CID) and Calling Identity on Call Waiting (CIDCW) systems, British Telecom Calling Line Identification Service (CLIP), the Cable Communications Association's Caller Display Services (CDS), and similar evolving services. The CMX602A also meets the requirements of emerging Caller Identity with Call Waiting Services (CIDCW).

This device includes a 'zero-power' ring or line polarity reversal detector, a dual-tone (2130Hz plus 2750Hz) internally timed CPE Alerting Signal (CAS) detector, and a 1200-baud FSK Bell202/V23 compatible asynchronous data demodulator with data retiming circuitry which removes the need for a UART in the associated µC.

The CMX602A is suitable for use in systems using Bellcore specifications GR-30-CORE and SR-TSV-002476, British Telecom specifications SIN227 and SIN242, CCA TW/P&E/312, ETSI: ETS 300 659 parts 1 and 2 and ETS 300 778 parts 1 and 2, and Mercury Communications MNR 19.

This device may be used with a 2.7V to 5.5V supply and is available in the following packages:
16-pin SOIC (CMX602AD4) and a 16-pin PDIP (CMX602AP3).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

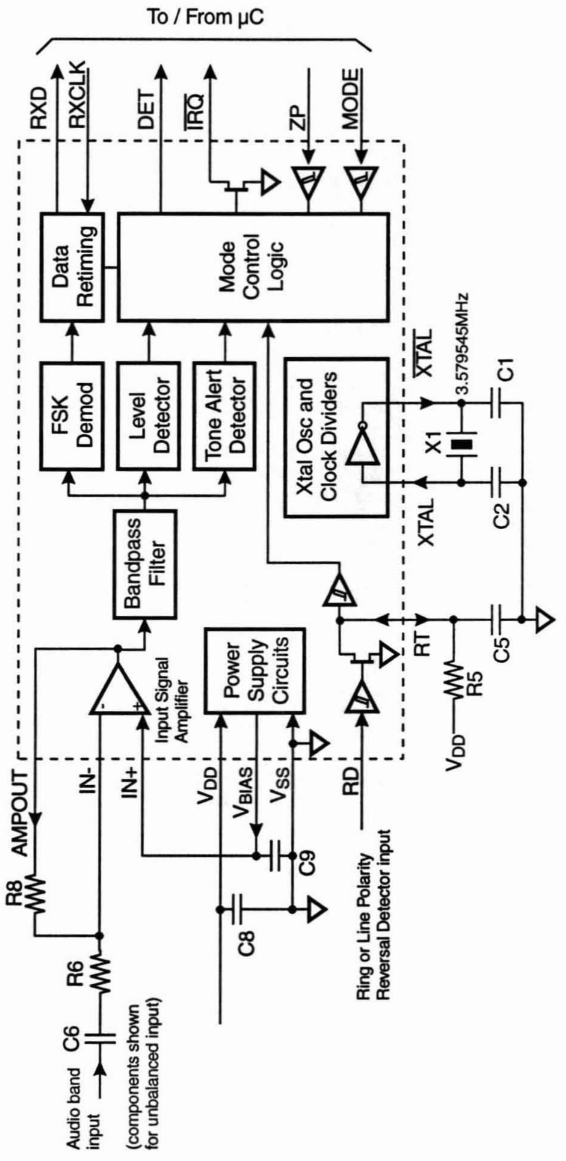

To / From µC
RXD
RXCLK
DET
IRQ
ZP
MODE
Data Retiming
Mode Control Logic
FSK Demod
Level Detector
Tone Alert Detector
Xtal Osc and Clock Dividers
Bandpass Filter
Power Supply Circuits
Input Signal Amplifier
AMPOUT
R8
IN-
IN+
R6
C6
Audio band input
(components shown for unbalanced input)
VDD
VBIAS
VSS
C8
C9
RD
Ring or Line Polarity Reversal Detector input
RT
R5
VDD
C5
XTAL
XTAL
X1
3.579545MHz
C2
C1

Figure 1: Block Diagram

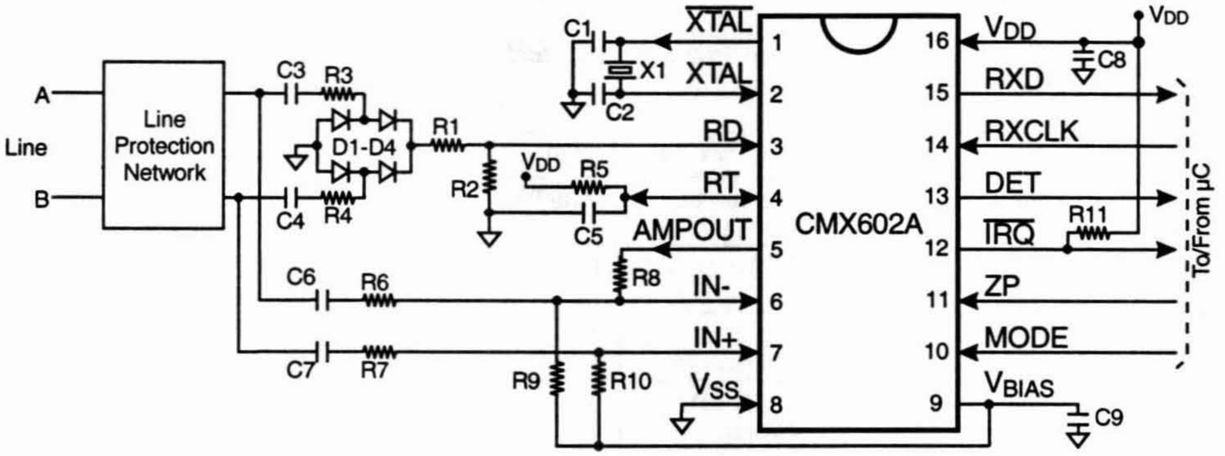
2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{\text{XTAL}}$	output	Output of the on-chip Xtal oscillator inverter
2	XTAL	input	Input to the on-chip Xtal oscillator inverter
3	RD	input (S)	Input to the Ring or Line Polarity Reversal Detector
4	RT	input / output	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V_{DD} and a capacitor to V_{SS} should be connected to RT to filter and extend the RD input signal
5	AMPOUT	output	Output of the on-chip Input Signal Amplifier
6	IN -	input	Inverting input to the on-chip Input Signal Amplifier
7	IN +	input	Non-inverting input to the on-chip Input Signal Amplifier
8	V_{SS}	power	Negative supply
9	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	MODE	input (S)	Input used to select the Tone Alert or FSK Level Detection operating mode. See Section 4.1
11	ZP	input (S)	High level on this input selects 'Zero-Power' mode, a low level input enables the V_{BIAS} supply, the Input signal amplifier, the Bandpass Filter , and either the FSK or the Tone alert circuits depending on the MODE input
12	$\overline{\text{IRQ}}$	output	Open-drain output (active low) that may be used as an Interrupt Request / Wake-up input to the associated µC. Indicates CAS Dual Tone event of correct duration when device is in Tone Alert Detect Mode. An external pull-up resistor should be connected between this output and V_{DD}.
13	DET	output	Logic level output driven by the Ring or Line Polarity Reversal Detector, the Tone Alert Detector or the FSK Level detect circuits, depending on the operating mode. When device is in Tone Alert Mode, it may be used as a near end voice mute control signal. See Section 4.1
14	RXCLK	input	Logic level input, which may be used to clock, received data bits out of the FSK Data Retiming block. When held high disables FSK Data Retiming block.
15	RXD	output	Logic level output carrying either the raw output of the FSK Demodulator or re-timed 8-bit characters depending on the state of the RXCLK input. See Section 4.6
16	V_{DD}	power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Notes: input (S) = Schmitt trigger input

Table 1 : Signal List

3. External Components


A
B
Line
Line Protection Network
C3
R3
C4
R4
D1-D4
R1
R2
VDD
R5
C5
C1
C2
X1
R8
C6
R6
C7
R7
R9
R10
XTAL
XTAL
RD
RT
AMPOUT
IN-
IN+
VSS
1
2
3
4
5
6
7
8
CMX602A
16
15
14
13
12
11
10
9
VDD
RXD
RXCLK
DET
IRQ
ZP
MODE
VBIAS
C8
C9
R11
VDD
To/From µC

Note: It is recommended that the printed circuit board provide a ground plane in the CMX602A area to provide a low impedance ground connection to the V_{SS} pin and to the bypass capacitors C8 and C9.

Figure 2 : Recommended External Components for Bellcore and/or British Telecom Application

R1		470kΩ	±1%
R2	Note 1		±1%
R3, R4 R5, R6 R7		470kΩ	±1%
R8	Note 2, 3	470kΩ @ 3.3V 680kΩ @ 5.0V	±1%
R9	Note 2	240kΩ @ 3.3V 200kΩ @ 5.0V	±1%
R10		160kΩ	±1%

R11		100kΩ	±20%
C1, C2		18pF	±20%
C3, C4		0.1µF	±20%
C5		0.33µF	±20%
C6, C7		680pF	±20%
C8,C9		0.1µF	±20%
X1	Note 4	3.579545MHz	±0.1%
D1 - D4		1N4004	

Table 2: Recommended External Components

Recommended External Component Notes:

1. See Section 4.8
2. See Section 4.2
3. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656kΩ @ 5.0V.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Mode Control Logic

The CMX602A's operating mode and the source of the DET and $\overline{\text{IRQ}}$ outputs are determined by the logic levels applied to the MODE and ZP input pins.

ZP	MODE	Mode	DET output from	$\overline{\text{IRQ}}$ output from
0	0	Tone Alert Detect	Tone Alert Signal Detection	Valid 'off-hook' CAS Duration. Ring or Line Polarity Reversal Detector
0	1	FSK Receive	FSK Level Detector	FSK Data Retiming (if enabled). Ring or Line Polarity Reversal Detector.
1	0	Zero-Power	Ring or Line Polarity Reversal Detector	Ring or Line Polarity Reversal Detector.
1	1	Zero-Power	Ring or Line Polarity Reversal Detector	None

In the 'Zero-Power' modes, power is removed from all of the internal circuitry except for the Ring or Line Polarity Reversal Detector and the DET and $\overline{\text{IRQ}}$ outputs.

4.2 Input Signal Amplifier

The Input Signal Amplifier is used to convert the balanced FSK and Tone Alert signals received over the telephone line to an unbalanced signal of the correct amplitude for the FSK receiver and Tone Alert Detector circuits.

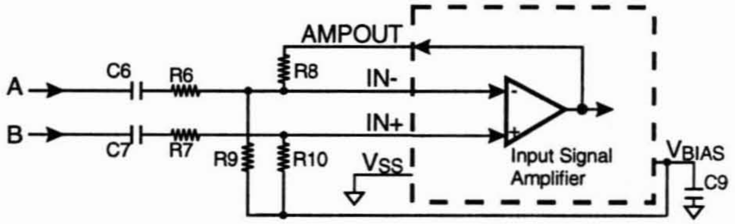


Figure 3: Input Signal Amplifier, balanced input configuration

The design equations for this circuit are:

$$\text{Differential Voltage Gain } \frac{V_{AMPOUT}}{V_{(B-A)}} = \frac{R8}{R6} \qquad R9 = \frac{R8 \times R10}{(R8 - R10)}$$

$$R6 = R7 = 470k\Omega \qquad R10 = 160k\Omega$$

The target differential voltage gain depends on the expected A and B input signal levels and the CMX602A's internal overload and threshold levels, which are proportional to the supply voltage.

The CMX602A has been designed to meet the applicable specifications when R8 = 430kΩ at V_{DD} = 3.0V nominal, rising to 680kΩ at V_{DD} = 5.0V (see note) and R9 = 240kΩ at V_{DD} = 3.0V dropping to 200kΩ at V_{DD} = 5.0V as indicated in Section 3 and as shown in Figure 5. Reference Notes found in Section 3.

The Input Signal Amplifier may also be used to allow the CMX602A to operate from an unbalanced signal source as shown in Figure 4. In this unbalanced signal configuration, the values of R6 and R8 are the same as used for the balanced input configuration.

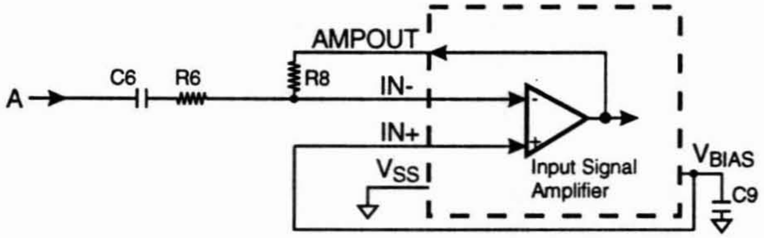


Figure 4: Input Signal Amplifier, unbalanced input configuration

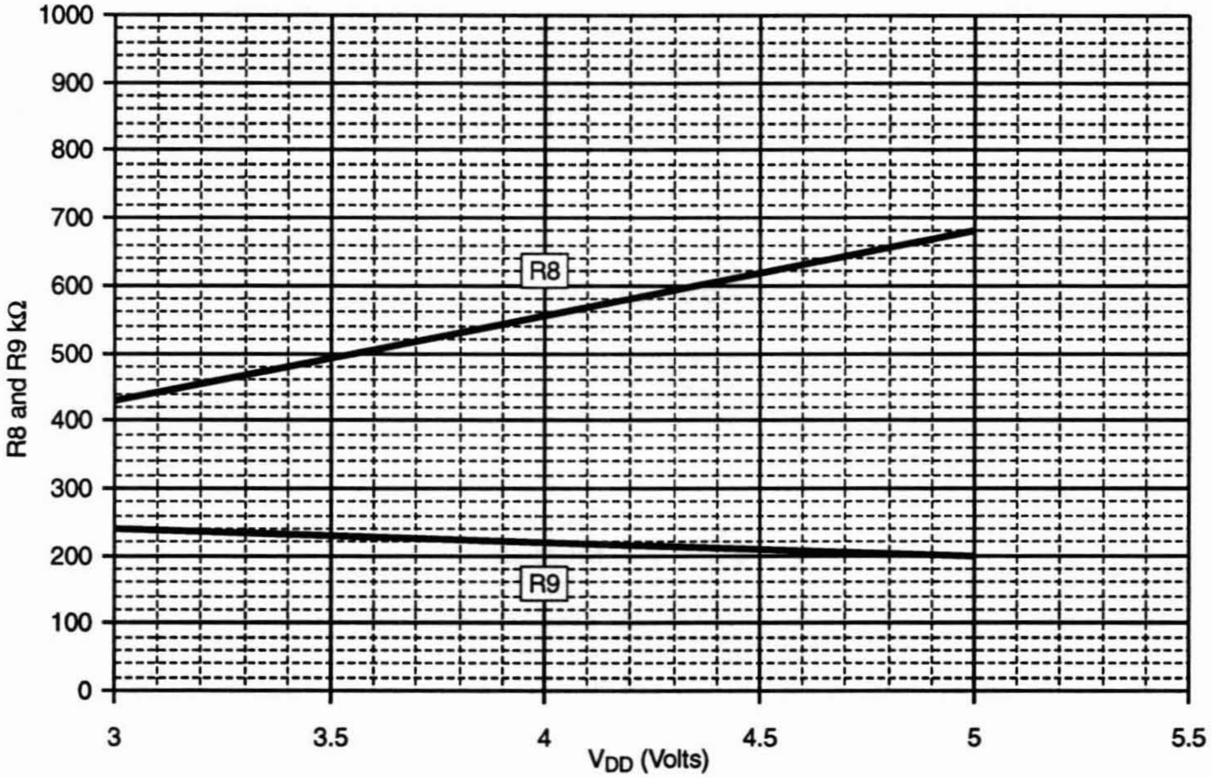


Figure 5: Input Signal Amplifier, Optimum Values of R8 and R9 vs. V_{DD}

4.3 Bandpass Filter

The Bandpass Filter is used to attenuate out of band noise and interfering signals from reaching the FSK Demodulator, Tone Alert Detector and Level Detector circuits. The characteristics of this filter differ between FSK and Tone Alert modes. Switched Capacitor filter stages clocked at 57.7kHz provide primary filtering. If the input signal is band limited to below 28.85kHz then external anti-aliasing filtering is not required.

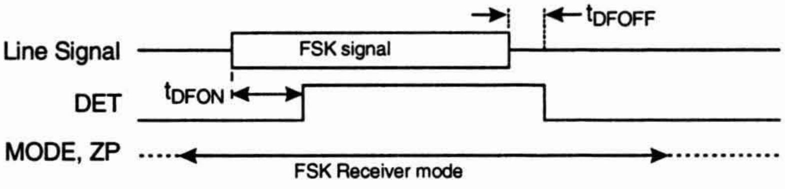
4.4 Level Detector

The Level Detector block operates by measuring the level of the signal at the output of the Bandpass Filter. It then compares it against a threshold, which depends on whether FSK Receive or Tone Alert Detect mode has been selected.

In Tone Alert Detect mode the output of the Level Detector block provides an input to the Tone Alert Signal Detector.

In FSK Receive mode the CMX602A DET output will be set high when the level has exceeded the threshold for a sufficient duration. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: In FSK Receive mode, this circuit may also respond to non-FSK signals such as speech.



See Section 6.1 for definitions of t_{DFON} and t_{DFOFF}

Figure 6: FSK Level Detector Operation

4.5 FSK Demodulator

The FSK Demodulator block converts the 1200 baud FSK input signal to a digital data stream which is output via the RXD pin as long as the Data Retiming function is not enabled (Holding RXCLK continuously high). The RXD output does not depend on the state of the FSK Level Detector output.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

4.6 FSK Data Retiming

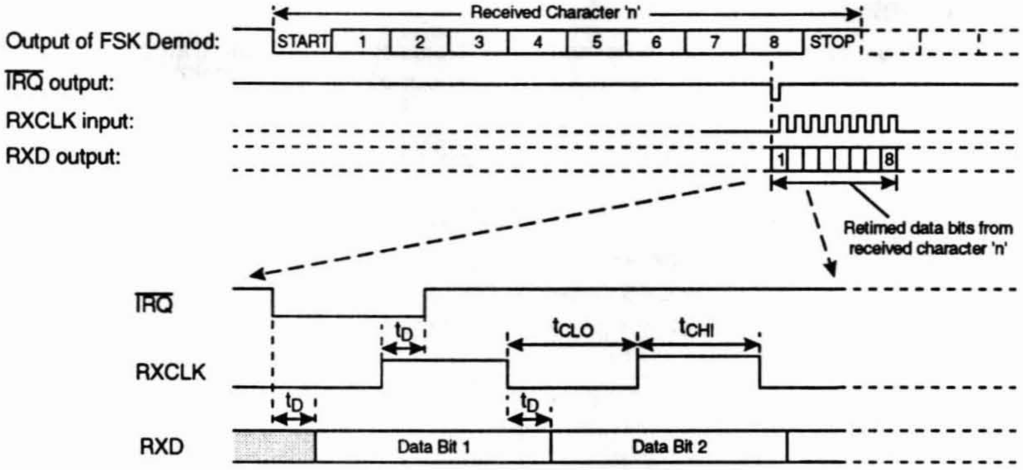
The Data Retiming block extracts the 8 data bits of each character from the received asynchronous data stream and presents them to the µC under the control of strobe pulses applied to the RXCLK input. The timing of these pulses is not critical, and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The block operates on a character by character basis by first looking for the mark to space transition which signals the beginning of the start bit. Using this transition as a timing reference, the block samples the output of the FSK Demodulator in the middle of each of the following 8 received data bits and stores the results in an internal 8-bit shift register.

When the eighth data bit has been clocked into the internal shift register, the CMX602A examines the RXCLK input. If RXCLK input is low, then the $\overline{\text{IRQ}}$ output will be pulled low, thereby sending the first of the stored data bits to the RXD output pin. Upon detecting that the $\overline{\text{IRQ}}$ output has gone low, the µC should pulse the RXCLK pin high 8 times. The high to low transition at the end of the first 7 of these pulses will be used by the CMX602A to shift the next data bit from the shift register onto the RXD output. At the end of the eighth pulse, the FSK Demodulator output will be reconnected to the RXD output pin. The $\overline{\text{IRQ}}$ output will be cleared the first time the RXCLK input goes high.

Thus to use the Data Retiming function, the RXCLK input should be kept low until the $\overline{\text{IRQ}}$ output goes low; if the Data Retiming function is not required the RXCLK input should continuously be kept high.

The only restrictions on the timing of the RXCLK waveform are those shown in Figure 7 and the need to complete the transfer of all eight bits into the µC within 8.3ms (to empty the buffer before the next character is received and put into the buffer).


Received Character 'n'
Output of FSK Demod:
START
1
2
3
4
5
6
7
8
STOP
IRQ output:
RXCLK input:
RXD output:
1
8
Retimed data bits from received character 'n'
IRQ
RXCLK
RXD
tD
tCLO
tCHI
tD
tD
Data Bit 1
Data Bit 2

t_D = Internal CMX602A delay (max 1µS); t_{CLO} = RXCLK low time (min 1µS); t_{CHI} = RXCLK high time (min 1µS)

Figure 7: FSK Operation with Data Retiming

Note: If enabled, the Data Retiming block will interpret the FSK Channel Seizure signal (a sequence of alternating mark and space bits) as valid received characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters.

4.7 FSK Data Without Retiming

If the Data Retiming facility is not required, the RXCLK input to the CMX602A should continuously be kept high. The asynchronous data from the FSK Demodulator is then connected directly to the RXD output pin and the $\overline{\text{IRQ}}$ output will not be activated by the FSK signal. This case is illustrated in Figure 8.

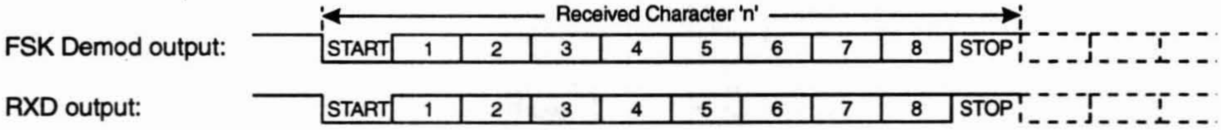

Received Character 'n'
FSK Demod output:
START
1
2
3
4
5
6
7
8
STOP
RXD output:
START
1
2
3
4
5
6
7
8
STOP

Figure 8: FSK Operation without Data Retiming (RXCLK always high)

4.8 Tone Alert Detector

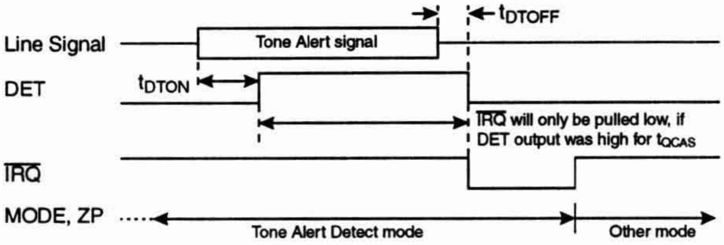
The Tone Alert Detector block is enabled when the CMX602A is set to Tone Alert Detector operating mode. It then monitors the received signal for the presence of simultaneous 2130Hz and 2750Hz tones of sufficient level and duration.

Two digital bandpass filters, centered around 2130Hz and 2750Hz, are used within the block to provide additional rejection of interfering signals.

The CMX602A DET output will be set high while Tone Alert signal is detected.

When DET goes low at the end of the Tone Alert signal, the $\overline{\text{IRQ}}$ output will be pulled low, only if DET was high for a period of time falling within the CAS qualifying time (t_{QCAS}) limits (See Section 6.1). $\overline{\text{IRQ}}$ will remain low until the CMX602A is switched out of Tone Detect mode. This $\overline{\text{IRQ}}$ falling transition indicates a valid CAS dual-tone has occurred.

Note: The t_{QCAS} timing has been optimized for the detection of 75 to 85ms CPE Alert Signals (CAS) used in off-hook applications. The longer (88ms to 110ms) Tone Alert signal employed by British Telecom for on-hook applications will not necessarily cause $\overline{\text{IRQ}}$ to go low.


t_{DTOFF}
Line Signal
Tone Alert signal
DET
t_{DTON}
$\overline{\text{IRQ}}$ will only be pulled low, if DET output was high for t_{QCAS}
$\overline{\text{IRQ}}$
MODE, ZP
Tone Alert Detect mode
Other mode

See Section 6.1 for definitions of t_{DTON}, t_{DTOFF} and t_{QCAS}

Figure 9: Tone Alert Detector Operation

4.9 Ring or Line Polarity Reversal Detector

These circuits are used to detect the Line Polarity Reversal and Ringing signals associated with the Calling Line Identification protocol. Figure 10 illustrates their use in a typical application.

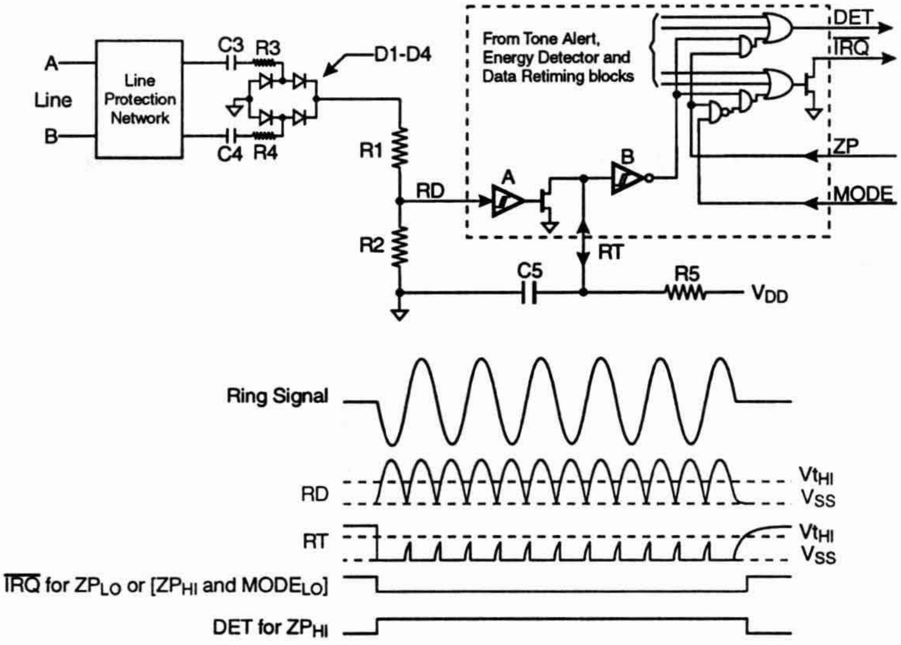

A
Line
B
Line Protection Network
C3 R3
C4 R4
D1-D4
R1
RD
R2
From Tone Alert, Energy Detector and Data Retiming blocks
DET
$\overline{\text{IRQ}}$
ZP
MODE
A
B
RT
C5
R5
V_{DD}
Ring Signal
RD
Vt_{HI}
V_{SS}
RT
Vt_{HI}
V_{SS}
$\overline{\text{IRQ}}$ for ZP_{LO} or [ZP_{HI} and $MODE_{LO}$]
DET for ZP_{HI}

Figure 10: Ring or Line Polarity Reversal Operation

When no signal is present on the telephone line, RD will be at V_{SS} and RT pulled to V_{DD} by R5 so the output of the Schmitt trigger 'B' will be low.

The ring signal is usually applied at the subscriber's exchange as an ac voltage. The ring signal is inserted in series with one of the telephone wires and will pass through either C3 and R3 or C4 and R4 to appear at the top end of R1 in a rectified and attenuated form.

The signal prior to R1 will be further attenuated by the potential divider formed by R1 and R2 before being applied to the CMX602A input RD. If the amplitude of the signal appearing at RD is greater than the input threshold (Vt_{HI}) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C5. The output of the Schmitt trigger 'B' will then go high, activating the DET and/or $\overline{IRQ}$ outputs depending on the states of the MODE and ZP inputs.

The minimum amplitude ringing signal that is certain to be detected is:

$$\left(0.7 + Vt_{HI}\frac{(R1+R2+R3)}{R2}\right)(0.707V_{RMS})$$

Where Vt_{HI} is the high-going threshold voltage of the Schmitt trigger A (see Section 6.1).

With R1, R3 and R4 all 470kΩ as indicated in Figure 2, then setting R2 to 68kΩ will guarantee detection of ringing signals of $40V_{RMS}$ and above for $V_{DD} = 2.7$ to 5.5V.

A line polarity reversal may be detected using the same circuit but there will be only one pulse at RD. The British Telecom specification SIN242 indicates that the circuit must detect a +15V to -15V reversal between the two lines slewing in 30ms. For a linearly changing voltage at the input to C3 (or C4), then the voltage appearing at the RD pin will be

$$\frac{dV}{dt}C3\left(1-e^{-\frac{t}{T}}\right)R2$$

where $T = C3(R1+R2+R3)$ and $\frac{dV}{dt}$ is the input slew rate.

For dV/dt = 500V/sec (15V in 30ms), R1, R3 and R4 all 470kΩ and C3, C4 both 0.1µF as indicated in Figure 2, then setting R2 to 390kΩ will guarantee detection at $V_{DD} = 5.5V$.

If the time constant of R5 and C5 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger keeping the DET and/or $\overline{IRQ}$ outputs active for the duration of a ring cycle

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD}\left(1-e^{-\frac{t}{R5C5}}\right)$$

As the Schmitt trigger high-going input threshold voltage (Vt_{HI}) has a minimum value of 0.56 x V_{DD}, then the Schmitt trigger 'B' output will remain high for a time of at least 0.821 x R5 x C5 following a pulse at RD.

Using the values provided in Figure 2 (470kΩ and 0.33µF) gives a minimum time of 100ms (independent of V_{DD}), which is adequate for ring frequencies of 10Hz or above.

If necessary, the µC can distinguish between a ring and a reversal by timing the length of the $\overline{IRQ}$ or DET output.

4.10 Xtal Osc and Clock Dividers

A 3.579545MHz clock present at the XTAL pin determines frequency and timing accuracy of the CMX602A. This may be generated by the on-chip oscillator inverter using the external components C1, C2, and X1 of Figure 2, or may be supplied from an external source to the XTAL input, in which case C1, C2, and X1 should not be fitted.

The oscillator is turned off in the 'Zero-Power' modes.

If the clock is provided by an external source which is not always running, then the ZP input must be set high when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by CMX602A as well as generating undefined states of the RXD, DET, and $\overline{\text{IRQ}}$ outputs.

5. Application

5.1 Calling Identity Delivery on Call Waiting (CIDCW) Application

The CMX602A supports Calling Line ID subscriber line protocols based on either the Bell 202 or CCITT V23 1200 baud FSK signaling for on hook (Type 1) and off-hook (Type 2) data transmission.

Within the Bell 202 and V.23 protocols the most difficult aspect of designing CIDCW equipment is that of correctly detecting the CAS CPE Alerting Signal in the presence of speech signals, as required within the Bellcore specifications.

This application provides guidance, suggestions, and an example circuit design to incorporate the CMX602A within the telephone unit.

5.1.1 Glossary of terms

Terms	Description
CAS	Dual-tone CPE Alerting Signal as defined in SR-TSV-002476.
CID	Calling Identity Delivery System (Bellcore).
CIDCW	Calling Identity Delivery on Call Waiting, see Bellcore Documents GR-30-CORE, and SR-TSV-002476.
CLIP	Calling Line Delivery Presentation (British Telecom)
CPE	Customer Premise Equipment i.e. the telephone set.
dBm	Signal level measurement, as used here 0dBm = 775mV$_{RMS}$
Hook Switch	The switch in a telephone which is operated when the handset is placed in the cradle.
On-Hook	The condition when the CPE is not being used i.e. the telephone handset is placed on the cradle, operating the hook switch.
Off-Hook	The condition when the CPE is in use i.e. the telephone handset is removed from the cradle, releasing the hook switch.

5.1.2 Requirements

Bellcore Special Report SR-TSV-002476 includes a test plan for CPE Alerting Signal Detectors, which defines three categories of test:

1. Signal Recognition Test without speech present.
2. Talkdown Test – missed signals in the presence of speech,
3. Talkoff Test - false detection's caused by speech.

The CMX602A will meet the requirements of the Signal Recognition Test without any problem. However, it will not meet the requirements of the Talkdown Test and the Talkoff Test if connected directly across the tip and ring of the 2-wire telephone line. This is because of the relatively high level of locally generated (near end) speech. (SR-TSV-002476 states that the average level of near end speech is 9dB higher than the average level of far end speech when both are measured at the tip and ring of the CPE).

These high near end speech levels can be too great to allow successful detection of the CAS Signals, and are more likely to give rise to false detection's.

A 2 to 4-wire hybrid is required to reduce the level of near end speech appearing at the CMX602A's input when it is in CAS detect mode. This should ideally provide about 16dB rejection of the near end speech although significant performance gains can be achieved with as little as 7dB.

5.1.3 Hardware

Any Feature Phone design will include circuitry to perform the normal telephone functions for dialing, AC and DC line termination, microphone signal amplification, and (most importantly for CIDCW applications) a 2 to 4-wire hybrid that can be used to drive the CMX602A. See Figure 11.

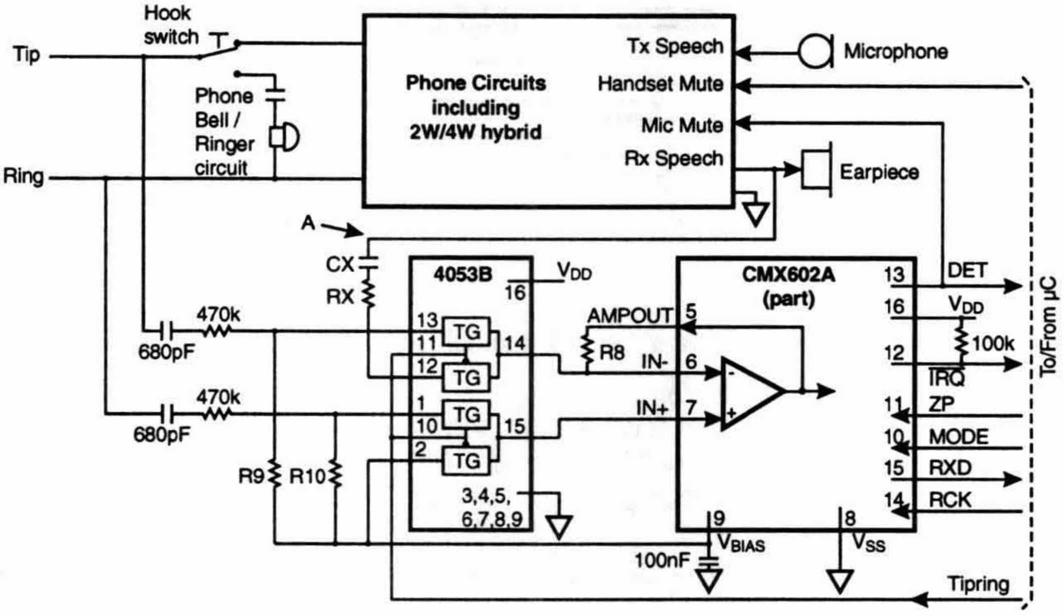

Hook switch
Tip
Ring
Phone Bell / Ringer circuit
Phone Circuits including 2W/4W hybrid
Tx Speech
Handset Mute
Mic Mute
Rx Speech
Microphone
Earpiece
A
CX
RX
4053B
VDD
16
13
11
12
14
1
10
2
15
TG
3,4,5, 6,7,8,9
470k
680pF
470k
680pF
R9
R10
CMX602A (part)
AMPOUT 5
R8
IN- 6
IN+ 7
13
DET
16
VDD
100k
12
IRQ
11
ZP
10
MODE
15
RXD
14
RCK
9
VBIAS
100nF
8
VSS
Tipring
To/From µC

Figure 11: Application in Feature Phone

Note: For values of CX and RX see Section 5.1.3. For values of R8 and R10 see Section 3.

This circuit uses two-third's of 4053B CMOS triple 2-channel analog multiplexer to switch the CMX602A analog input to the tip and ring lines or to be the receive (earpiece) output of the phone circuits. The control line 'Tipring" should be low when the CMX602A is being used to look for a CAS signal in off-hook mode. It should be high at all other times i.e. when receiving on-hook or off-hook FSK signals and when looking for the tone alert signal in a British Telecom on-hook CLID application.

The values of RX and CX depend on the characteristics of the phone circuits used and can be calculated on the following basis:

G is the received signal voltage at point A (See Figure 11) for a $1V_{RMS}$ signal applied between tip and ring. If Rx is made equal to G x 470k, then this will ensure that the CMX602A has the same sensitivity for signals coming via the Phone circuits as for those taken directly from the tip and ring lines. However, the CAS detection performance in 0ff-hook applications can be improved slightly by reducing the CMX602A's sensitivity to 6dB, thereby changing the 'will detect' level from –41dBm to –35dBm per tone.

The Optimum values for RX and CX are:

$$RX = 2 \times G \times 470k\Omega$$

$$CX = 680 \times \frac{470K}{Rx} \text{pF (the value is not critical)}$$

Note that the Microphone Mute Input of the phone circuits is driven by the CMX602A's DET as required by the 'off-hook' control algorithm provided in Section 5.3. If the particular circuits used do not have a Microphone Mute input, then this function should be implemented by using the spare switch found in the 4053B.

5.1.4 Software

In Figure 12 a successful CIDCW transaction is shown using the circuit shown in Figure 11 and the 'off-hook' control algorithm described in Section 5.3.

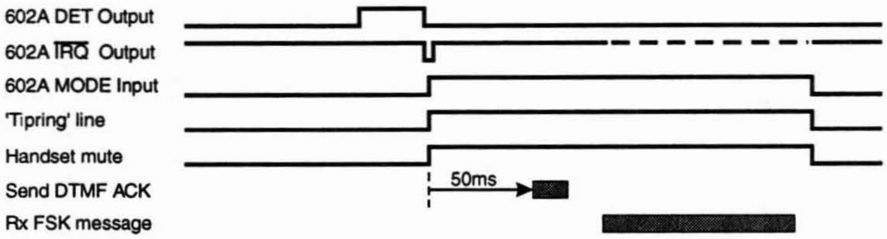


Figure 12: Successful CIDCW Transaction using the Circuit found in Figure 11

While looking for a CAS signal, the CMX602A is running in Tone Detect Mode (MODE Input low), with its input connected to the RX Speech. In this states the CMX602A's DET output directly controls the Microphone Mute line as required by the Data Sheet Algorithm. The DET output serves no other purpose at this stage.

CAS signal detection is indicated by the CMX602A's $\overline{\text{IRQ}}$ output going low. When this happens the µC should:

1. Set the CMX602A to FSK Mode by taking the MODE pin high (this will also clear the $\overline{\text{IRQ}}$ output).
2. Completely mute the local handset and keypad.
3. Set the Tipring line high, so that the CMX602A is connected directly across tip and ring (as the Rx Speech output of the phone circuits will now be muted).
4. Start a 50ms timer.

In the 50ms period between setting the CMX602A into the FSK mode and sending the ACK signal, the CMX602A's DET output should be monitored and the transaction terminated if the line goes high during this time, as described in Section 5.3.

At the end of the 50ms period, a DTMF ACK should be sent, after which the FSK message containing the waiting caller's ID will be received by the CMX602A. At the end of the message, the µC should set the CMX602A back into the 'looking for CAS' mode by taking the MODE and Tipring lines low and removing the local handset and keypad mute.

5.1.5 Printed Circuit Layout

The CMX602 is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} decoupling and V_{BIAS} decoupling are very important.

It is recommended that decoupling capacitors be placed so that connections between them and the device pins are as short as practicable and via a printed circuit ground plane, which can also be laid out to shield the receive path from interfering signals.

5.1.6 High Frequency interfering Signals

The CMX602A input filter uses switched capacitor technology running at 57.7kHz and is therefore sensitive to input signals at multiples of this frequency.

A linear anti-alias filter is included on chip between the output of the Input Signal Amplifier and the input to the switched capacitor filter. This should provide adequate attenuation of out of band signals for most applications. Additional attenuation may be added if necessary. This can be accomplished by adding a 22pF capacitor in parallel with the input amplifier feedback resister R8.

5.1.7 If the Ring Detect Circuit is not Used

The RD pin should be connected to V_{SS} and RT to V_{DD}.

5.1.8 Common Mode Interface

The interface circuits between the telephone line and the CMX602A as shown in figure XXX have been designed to reduce the effects of common mode noise voltages appearing between the line and the CMX602A's ground connection (VSS pin). However, excessive levels of common mode noise can cause the problems with the detection of the ringing signal or the line polarity reversal, with reception of CAS, the Tone Alert signal used in British Telecom's CLIP system, and FSK data signals.

The extent of the problem depends mainly on the power supply used for the CMX602A and the connection (if any) between this power supply and the tip and ring lines.

5.2 'On-Hook' Operation

The systems described in this section operate when the telephone set is not in use (on-hook) to display the number of a calling party before the call is answered. System specific descriptions are provided as well as a flowchart for on-hook applications (Figure 15).

5.2.1 Bellcore System

Figure 13 illustrates the line signaling and CMX602A input and output signals for the Bellcore 'On-Hook' Caller ID system as defined in Bellcore documents GR-30-CORE and SR-TSV-002476 and also in ETS 300 659-1 Section 6.1.1.

As for the British Telecom system, the 'Chan Seize' signal is a '1010...' FSK bit sequence. The Bellcore specifications do not require AC or DC line terminations while the FSK data is being received, however ETS 300 659-1 allows for the possibility of an AC termination begin applied.

Note: For simplicity of presentation, the Data Retiming function is not used in Figure 13 (RXCLK is kept high).

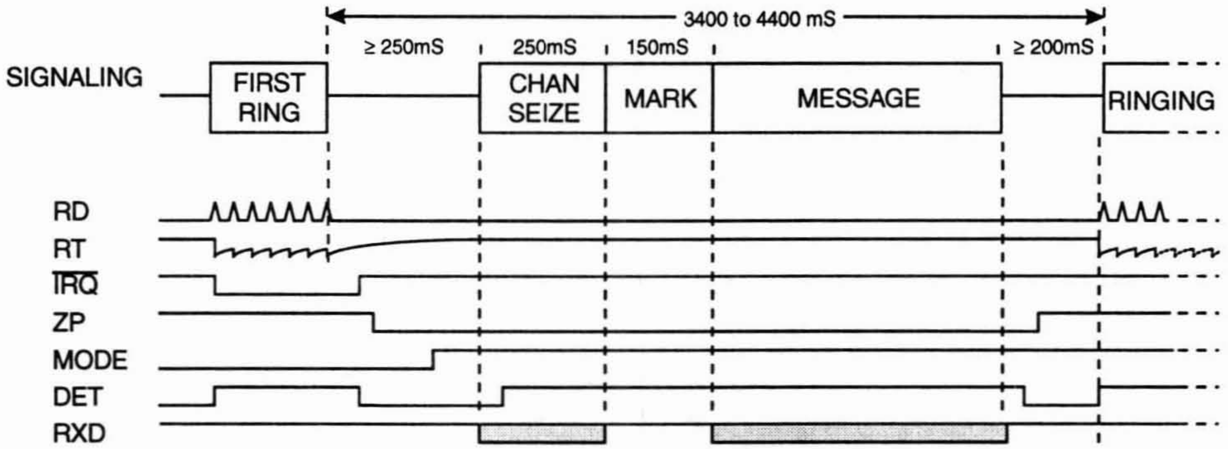


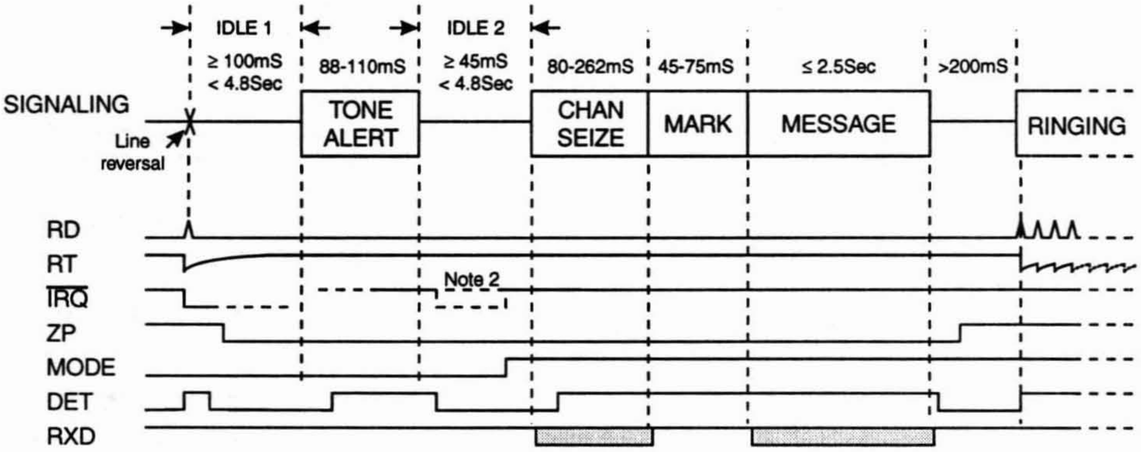
Figure 13: Bellcore System Signals

5.2.2 British Telecom System

Figure 12 illustrates the line signaling and CMX602A input and output signals for the British Telecom 'On-Hook' Caller ID system as defined in the British Telecom specifications SIN227 and SIN242 part 1. A similar system is described in ETSI 300 659-1 Section 6.1.2c.

The Tone Alert signal consists of simultaneous 2130Hz and 2750Hz tones. The 'Chan Seize' signal consists of a '1010..' FSK bit sequence. Not shown are the requirements for AC and DC loads, including a short initial Current Wetting Pulse, to be applied to the line 20ms after the end of the Tone Alert signal and to be maintained during reception of the FSK signal.

Note: For simplicity of presentation, the Data Retiming function is not used in Figure 14 (RXCLK is kept high).



Notes:
1. IDLE 1 + IDLE 2 ≤ 5 sec
2. IRQ may go low at end of DET high period but this is not gauranteed.

Figure 14: British Telecom System Signals

5.2.3 Other 'On-Hook' Systems

ETS 300 659-1 also allows for systems where the FSK transmission is preceded by a Dual Tone Alert signal similar to that used by British Telecom but without line reversal (ETS 300 659-1 Section 6.1.2a) or by a Ringing Pulse alerting Signal (ETS 300 659-1 Section 6.1.2b).

The U.K. CCA (Cable Communications Association) specification TW/P&E/312 precedes the FSK signals by a 200 to 450ms ring burst. AC and DC line terminations during FSK reception are optional.

Mercury Communications Ltd. Specification MNR 19 allows for either the British Telecom system or that specified by CCA.

As these are all slight variants on the Bellcore and British Telecom systems, they can also be supported by the CMX602A.

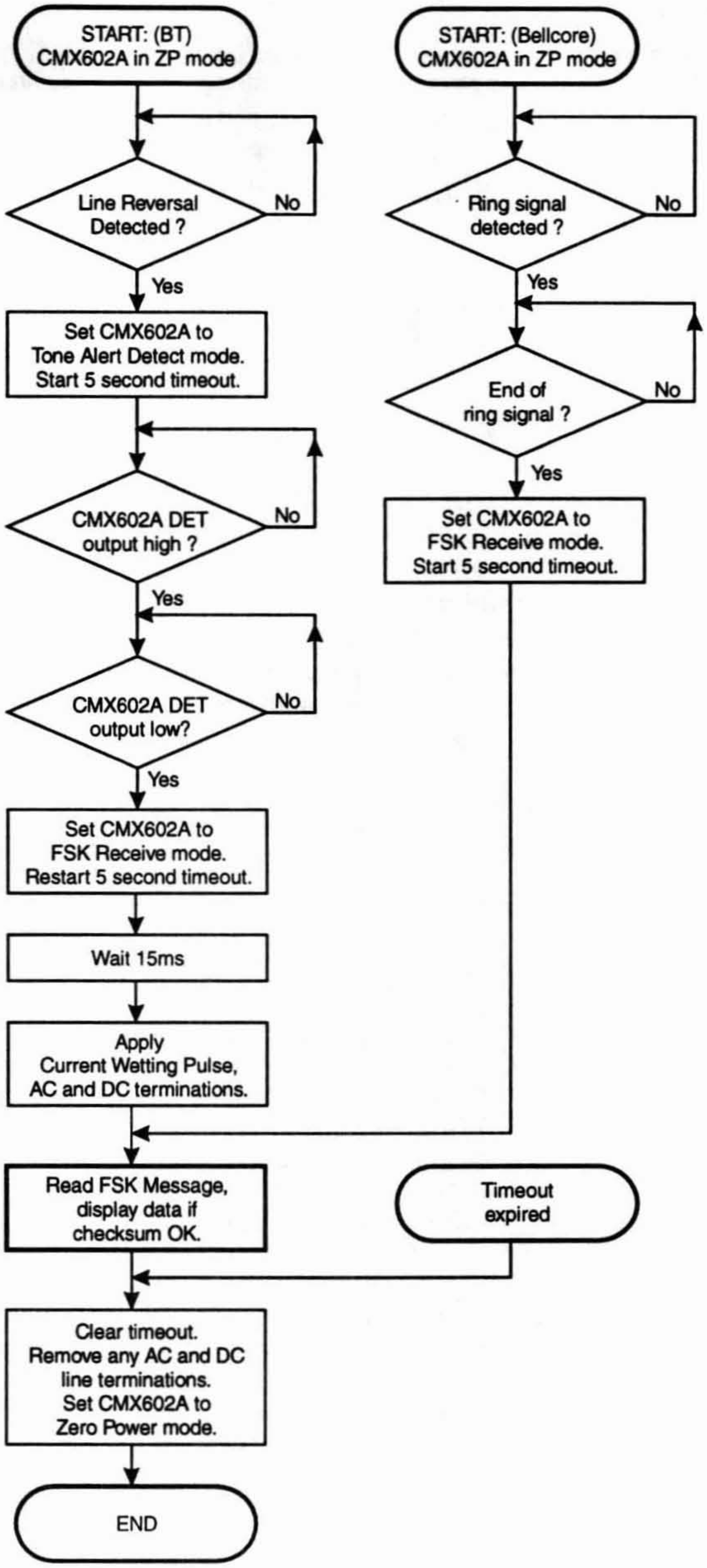
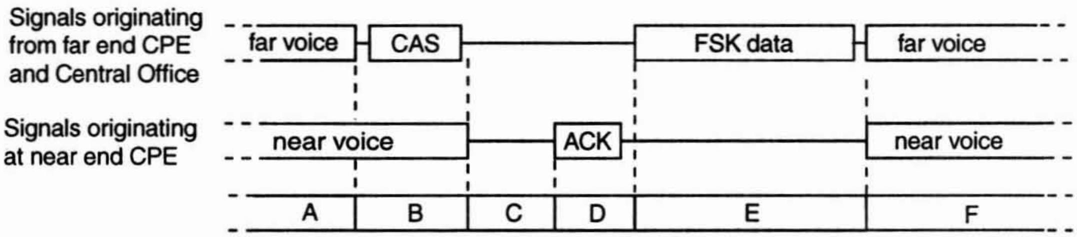

START: (BT)
CMX602A in ZP mode
Line Reversal
Detected ?
No
Yes
Set CMX602A to
Tone Alert Detect mode.
Start 5 second timeout.
CMX602A DET
output high ?
No
Yes
CMX602A DET
output low?
No
Yes
Set CMX602A to
FSK Receive mode.
Restart 5 second timeout.
Wait 15ms
Apply
Current Wetting Pulse,
AC and DC terminations.
Read FSK Message,
display data if
checksum OK.
Clear timeout.
Remove any AC and DC
line terminations.
Set CMX602A to
Zero Power mode.
END
START: (Bellcore)
CMX602A in ZP mode
Ring signal
detected ?
No
Yes
End of
ring signal ?
No
Yes
Set CMX602A to
FSK Receive mode.
Start 5 second timeout.
Timeout
expired

Figure 15: Flow Chart for 'On-Hook' Operation of CMX602A

5.3 'Off-Hook' Operation

The CIDCW (Calling Identity on Call Waiting) system, as described in this section, operates when the telephone set is in use (off-hook) to display the number of a waiting caller without interrupting the current call.

Bellcore documents GR-30-CORE and SR-TSV-002476, British Telecom specifications SIN227 and SIN242 part 2 and ETS 300-659-2 all describe similar systems in which a successful CIDCW transaction consists of a sequence of actions between the near end CPE (Customer Premises Equipment - e.g. a telephone) and the Central Office as indicated in Figure 16.


Signals originating from far end CPE and Central Office
far voice
CAS
FSK data
far voice
Signals originating at near end CPE
near voice
ACK
near voice
A
B
C
D
E
F

A. Normal conversation with both near and far voice present.
B. Central Office mutes far end voice, emits CAS, and becomes silent.
C. CPE recognizes CIDCW initiation and mutes near end voice and keypad.
D. CPE emits DTMF ACK to Central Office to signal its readiness to receive Caller ID data stream.
E. Central Office recognizes ACK and emits FSK Data stream of Caller ID data which is received and decoded by CPE.
F. CIDCW transaction is complete. CPE unmutes near end voice and Central Office unmutes far end voice returning to normal conversation with both near and far voice present.

Figure 16 CIDCW Transaction From Near End CPE Perspective

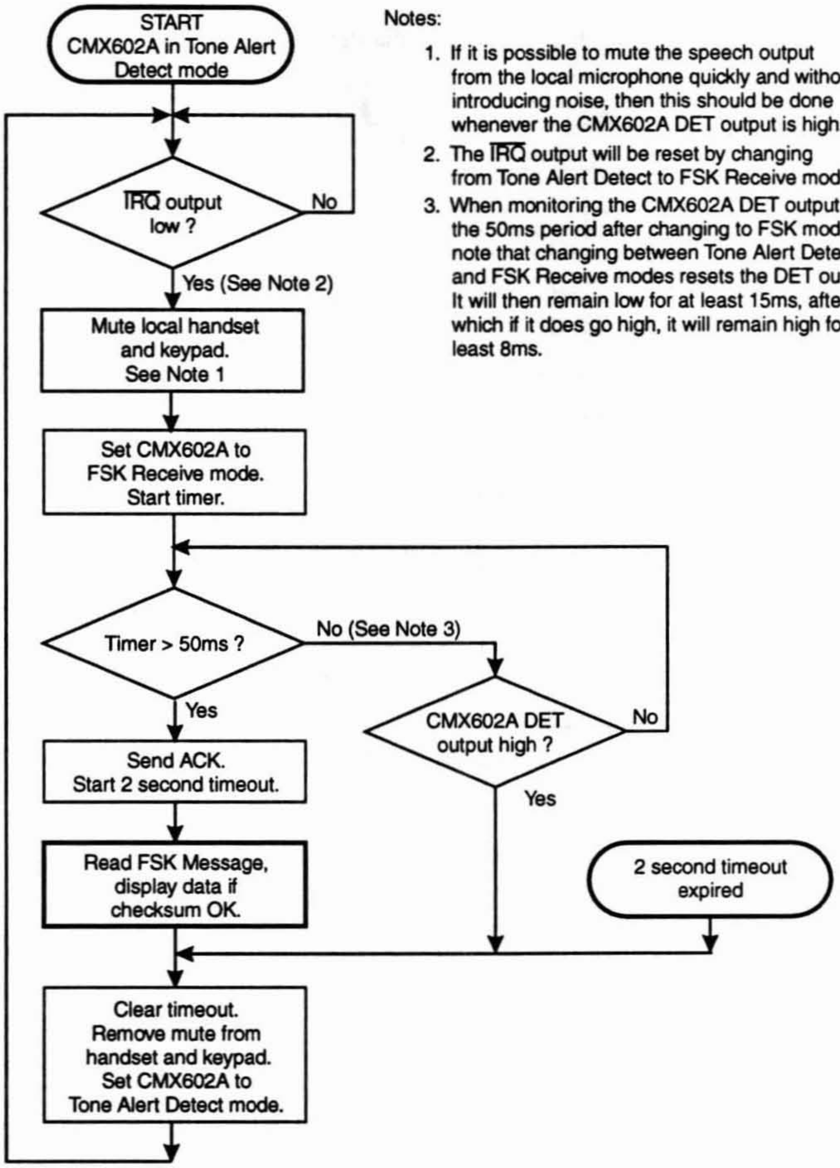
The CAS signal is transmitted by the Central Office to initiate a CIDCW transaction and consists of an 80ms burst of simultaneous 2130Hz and 2750Hz tones.

CAS detection is very important because a 'missed' signal causes Caller ID information to be lost and a false signal detection produces a disruptive tone which is heard by the far end caller. Because the CAS signals must be detected in the presence of conversations, which both mask and masquerade as the tone signals, this function is difficult to accomplish correctly.

Because the number of false responses (Talk-offs) and missed signals (Talk-downs) are related to the speech levels at the CMX602A input, the level of near end speech from the local handset is normally greater than that of far end speech coming from the Central Office. A further improvement in overall performance can be obtained by taking the CMX602A's audio input from the receive side of the telephone set hybrid where this is possible.

The internal algorithms used by the CMX602A to drive the DET and $\overline{IRQ}$ outputs in Tone Alert Detect mode have been optimized for the detection of off-hook CAS signals in the presence of speech when used according to the following principles:

1. If it is possible to mute the local speech from the microphone rapidly (within 0.5ms) without introducing noise (i.e. where the CIDCW equipment is built into the telephone set), then this muting should be done whenever the CMX602A is in Tone Alert Detect mode and the DET output is high. Doing this will markedly reduce the number of false responses generated by local (near end) speech. Note that the DET output is not used for any other purpose in an off-hook application when the CMX602A is set to Tone Alert Detect mode.
2. When the $\overline{IRQ}$ output goes low in Tone Alert Detect mode, this indicates that a CAS has been detected. The local handset and keypad should then be muted as required by the Bellcore specification and the CMX602A switched to FSK Receive mode to be ready to receive the FSK data. Doing this will also clear the $\overline{IRQ}$ output.
3. The CMX602A's DET output should be monitored for a period of 50ms after changing to FSK Receive mode and before sending the ACK signal. The transaction should be abandoned if the DET output goes high during this time, which would be the case if a false CAS detect had been caused by far end speech.


START
CMX602A in Tone Alert Detect mode
$\overline{\text{IRQ}}$ output low ?
No
Yes (See Note 2)
Mute local handset and keypad. See Note 1
Set CMX602A to FSK Receive mode. Start timer.
Timer > 50ms ?
No (See Note 3)
Yes
CMX602A DET output high ?
No
Yes
Send ACK. Start 2 second timeout.
Read FSK Message, display data if checksum OK.
2 second timeout expired
Clear timeout. Remove mute from handset and keypad. Set CMX602A to Tone Alert Detect mode.

Notes:

1. If it is possible to mute the speech output from the local microphone quickly and without introducing noise, then this should be done whenever the CMX602A DET output is high.
2. The $\overline{\text{IRQ}}$ output will be reset by changing from Tone Alert Detect to FSK Receive mode.
3. When monitoring the CMX602A DET output for the 50ms period after changing to FSK mode note that changing between Tone Alert Detect and FSK Receive modes resets the DET output. It will then remain low for at least 15ms, after which if it does go high, it will remain high for at least 8ms.

Figure 17, Flow Chart for 'Off-Hook' Operation of CMX602A

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	30	mA
Current into or out of any other pin	-20	20	mA
D4 / P3 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	1	2.7	5.5	V
Operating Temperature	1	-40	85	°C
Xtal frequency	2	3.575965	3.583125	MHz

Operating Limits Notes:

1. Operating temperature range –10°C to 60°C at V_{DD} < 3.0V.
2. A Xtal frequency of 3.579545MHz ±0.1% is required for correct Tone Alert and FSK detection.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 2.7V at T_{AMB} = 10°C to 60°C and V_{DD} = 3.0V to 5.0V at T_{AMB} = -40°C to 85°C

Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to $1.0V_{RMS}$

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ZP input high) at V_{DD} = 5.0V	1,2		0.02	1.0	µA
I_{DD} (ZP input low) at V_{DD} = 3.0V	1		0.5	1.0	mA
I_{DD} (ZP input low) at V_{DD} = 5.0V	1		1.0	2.0	mA
Logic 1 input level (RXCLK and XTAL inputs)		70%			V_{DD}
Logic 0 input level (RXCLK and XTAL inputs)				30%	V_{DD}
Logic input leakage current (V_{IN} = 0 to V_{DD}) excluding XTAL input		-1.0		1.0	µA
Output logic 1 level (I_{OH} = 360µA)		V_{DD} - 0.4			V
Output logic 0 level (I_{OL} = 360µA)				0.4	V
$\overline{IRQ}$ output 'off' state current (V_{OUT} = V_{DD})				1.0	µA
Schmitt Trigger input thresholds (Figure 18)					
High going (Vt_{HI})		$(0.56)(V_{DD})$		$(0.56)(V_{DD}) + 0.6$	V
Low going (Vt_{LO})		$(0.44)(V_{DD}) - 0.6$		$(0.44)(V_{DD})$	V
Tone Alert Detector					
'Low' tone nominal frequency			2130		Hz
'High' tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (t_{DTON} Figure 9)			55.0		ms
End of Tone Alert signal to DET and $\overline{IRQ}$ low time (t_{DTOFF} Figure 9)		0.5		10.0	ms
DET high time to ensure $\overline{IRQ}$ goes low (t_{QCAS} see Figure 9)		8.0		45.0	ms
To ensure detection:	3				
'Low' tone frequency deviation from nominal				±20	Hz
'High' tone frequency deviation from nominal				±30	Hz
Tone level of each simultaneously applied tone	4	-40.0		-2.2	dBV
2750Hz tone level with respect to 2130Hz tone level		-7.0		7.0	dB
Signal to Noise ratio	5	20.0			dB
Dual Tone Burst Duration for DET output		75			ms
Dual Tone Burst Duration to ensure $\overline{IRQ}$ goes low		75		85	ms

	Notes	Min.	Typ.	Max.	Units
To ensure non-detection:	6				
'Low' tone frequency deviation from nominal		±75			Hz
'High' tone frequency deviation from nominal		±95			Hz
Level (total)	4			-46.0	dBV
Dual Tone Burst Duration				45.0	ms
FSK Receiver					
Transmission rate		1188	1200	1212	Baud
V23 Mark (logic 1) frequency		1280	1300	1320	Hz
V23 Space (logic 0) frequency		2068	2100	2132	Hz
Bell202 Mark (logic 1) frequency		1188	1200	1212	Hz
Bell202 Space (logic 0) frequency		2178	2200	2222	Hz
Valid input level range	4	-40.0		-8.0	dBV
Acceptable twist (mark level with respect to space level)					
V23		-7.0		7.0	dB
Bell202		-10.0		10.0	dB
Acceptable Signal to Noise ratio					
V23	5	20.0			dB
Bell202	5	30.0			dB
Level Detector 'on' threshold level	4			-40.0	dBV
Level Detector 'off' to 'on' time (t_{DFON} Figure 6)				25.0	ms
Level Detector 'on' to 'off' time (t_{DFOFF} Figure 6)		8.0			ms
Input Signal Amplifier					
Input impedance	7	10.0			MΩ
Voltage gain			500		V/V
XTAL Input					
'High' pulse width	8	100			ns
'Low' pulse width	8	100			ns

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the CMX602A pins by external circuitry other than X1, C1, and C2.
2. RD, MODE, RXCLK inputs at V_{SS}, ZP input at V_{DD}. See Figure 19.
3. All conditions must be met to ensure detection.
4. For V_{DD} = 5.0V with equal level tones and with the input signal amplifier external components as shown in Section 3. The internal threshold levels are proportional to V_{DD}. For other supply voltages or different signal level ranges the voltage gain of the input signal amplifier should be adjusted by selecting the appropriate external components as described in Section 4.2
5. Flat Noise in the 300Hz-3400Hz band for V23 and 200Hz-3200Hz for Bell202.
6. Meeting any of these conditions will ensure non-detection.
7. Open loop, small signal, low frequency measurements.
8. Timing for an external input to the XTAL pin.

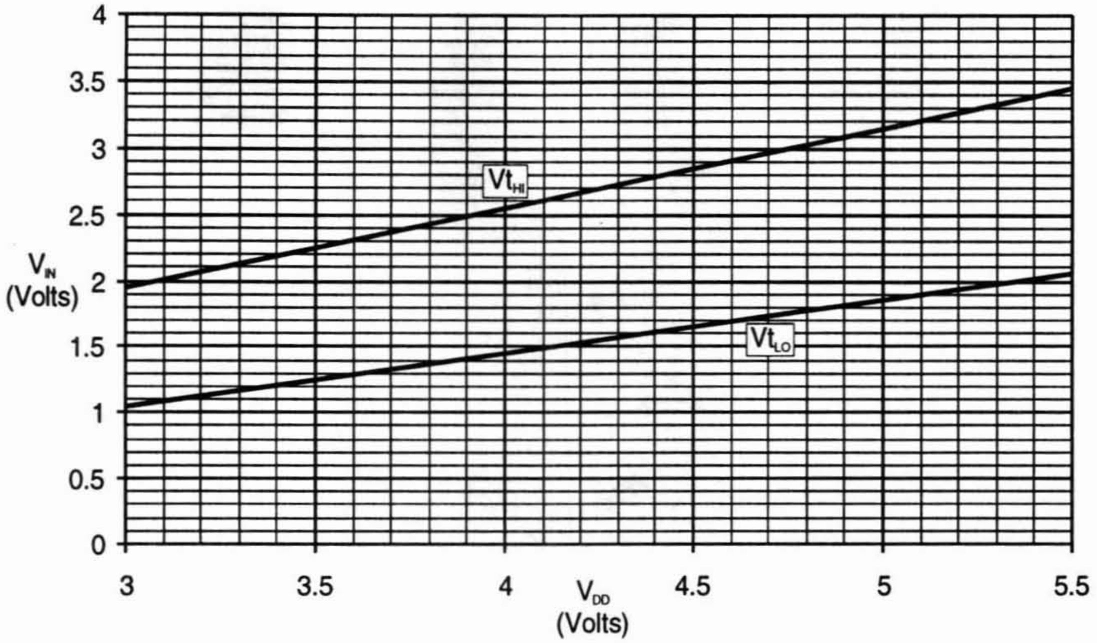


Figure 18: Schmitt Trigger typical input voltage thresholds vs. V_{DD}

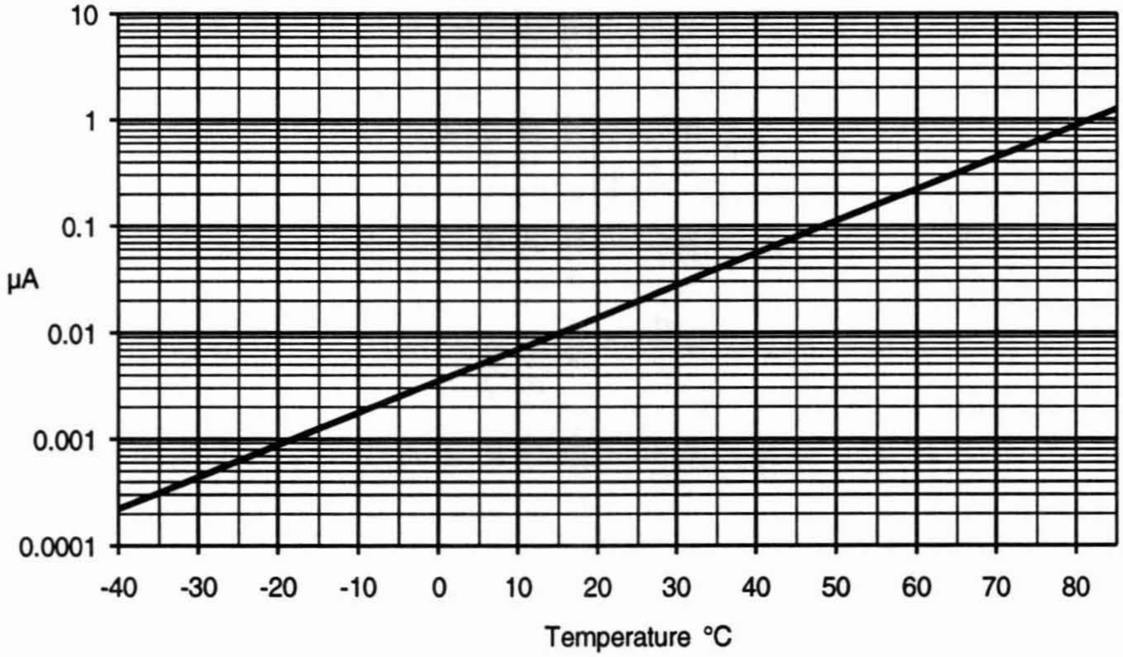


Figure 19: Typical 'Zero-Power' I_{DD} vs. Temperature (V_{DD} = 5.0V)

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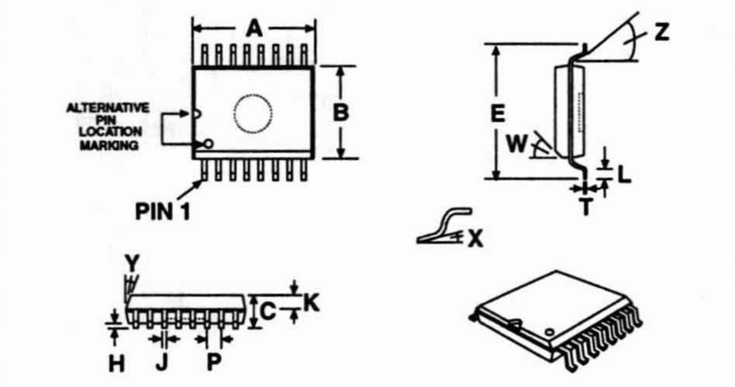
6.2 Packaging

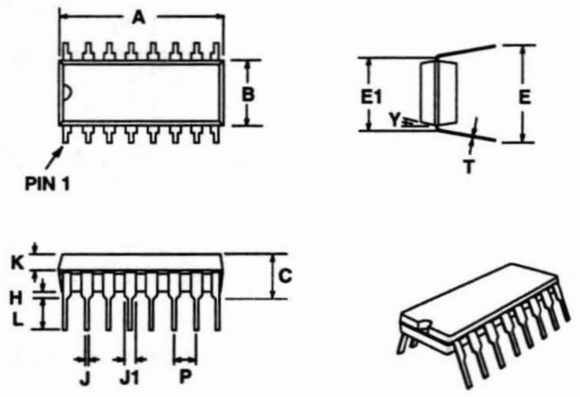


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 20 : 16-pin SOIC Mechanical Outline: *Order as part no. CMX602AD4*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 21 : 16-pin PDIP Mechanical Outline: *Order as part no. CMX602AP3*

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX605

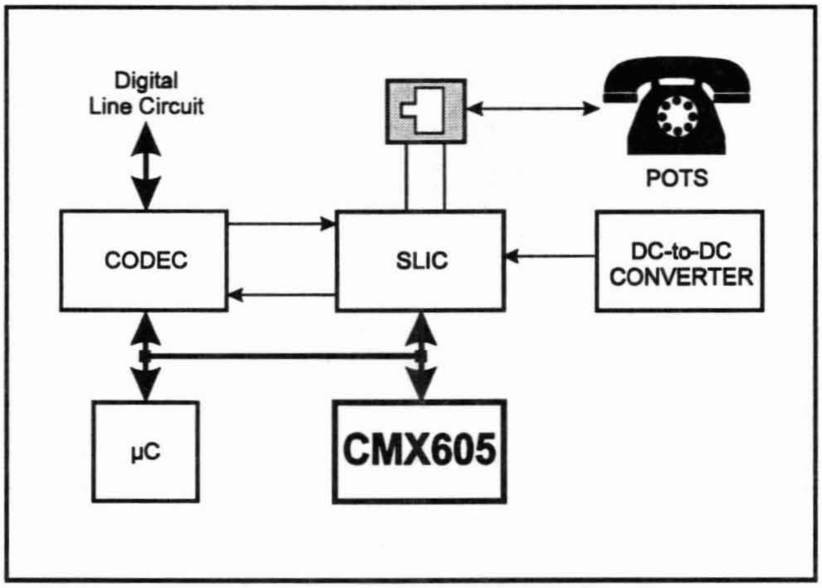
Digital Line to POTS Interface

Features

- **Pre-Programmed Tone Generators**
- **Fully Integrated DTMF Decoder/Encoder**
- **SPM Generator**
- **Simple Serial Control Interface**
- **'Zero-Power' (1µA) Standby Mode**
- **3.58MHz Xtal/Clock**
- **Low Power Operation (2.7V)**
- **V23/Bell 202 FSK Generator**
- **Digital Ringing Voltage Generator**

Applications

- **Digital Line to POTS Interface**
- **Subscriber Terminal Adapters**
- **Wireless Local Loop**
- **Computer Telephony Integration**
- **Telephone/Radio Patch Systems**
- **Pair Gain Systems**
- **Billing/SPM Systems**



The CMX605 is an integrated telecom tone generator and DTMF encoder/decoder, designed for ISDN interfaces, Wireless Local Loop and Analog to Digital Phone Conversion systems. The tone generator covers an extensive range of pre-programmed tones used in analog Phone systems (POTS). Three outputs are provided: 'Ringing signals', 'In-band tones or FSK data', and '12kHz/16kHz Metering pulses'. Simple software control facilitates the interface to a wide range of commonly used µCs and SLICs, enabling a comprehensive analog telephone line presentation.

The DTMF encoder/decoder presents the digital line interface with DTMF dialing information received from the telephone user and generates the appropriate DTMF tones for the POTS interface. DTMF tone pairs can be encoded along with each tone singly or with other dual tone signals, such as those used in CIDCW systems and 'On Hook' signaling systems.

Other tone standards supported are FAX and Modem 'answer' and 'originate', ITU (CCITT) 'R1', and 'R2' signals, a melody generator and special national tone sets (yet to be defined). Communication to and from the host µC is performed by a 'C-BUS' serial interface, which is similar to the SPI interface.

The CMX605 may be used with a 2.7V to 5.5V power supply and is available in a 16-pin SOIC (CMX605D4) package.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX624 Bell 202 and V.23 Modem with Call Progress and DTMF

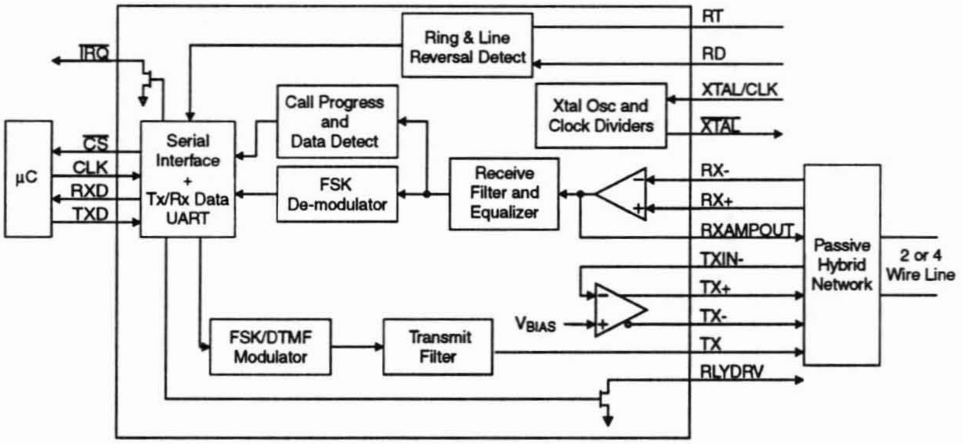
ADVANCE INFORMATION - Shipping September 98

Features

- Bell 202 and V.23 Compatible Modem
- 1200bps Full duplex Operation (2 or 4 Wire)
- Software Adjustable Tx and Rx Levels
- Programmable Group Delay Equalizer
- Answer/Originate Tone Generator/Detector
- Call Progress Tone Detection
- Integrated DTMF Encoder
- Line Reversal and Ring Detector
- Simple Serial Control Interface
- Hook Switch Relay Driver
- Zero-Power Standby Mode
- 3.0 to 5.0V Operation

Applications

- Telephone Telemetry Systems
- Remote Utility Meter Reading
- Security Systems
- Payphones
- Cable-TV Set Top Boxes
- Industrial Control Systems
- Electronic Cash Terminals
- Vending Machines



IRQ
µC
CS
CLK
RXD
TXD
Serial Interface + Tx/Rx Data UART
Call Progress and Data Detect
FSK De-modulator
Ring & Line Reversal Detect
Xtal Osc and Clock Dividers
Receive Filter and Equalizer
FSK/DTMF Modulator
Transmit Filter
V_{BIAS}
RT
RD
XTAL/CLK
XTAL
RX-
RX+
RXAMPOUT
TXIN-
TX+
TX-
TX
RLYDRV
Passive Hybrid Network
2 or 4 Wire Line

The CMX624 Bell 202 and V.23 modem provides full duplex 1200bps data signaling suitable for telephone based information and telemetry systems where low power operation is desired. Bell 202 and V.23 signaling delivers fast call set up times and robust, error resistant, transmission in 2 or 4 wire line circuits. A rich set of important additional functions enhances end product value while reducing size. These include: integrated DTMF encoder for dial out functions, single tone encoder for 'melody' generation, answer tone generator/detector, line reversal and ring detector for 'waking' up a sleeping µC, adjustable Tx and Rx gain, and a low impedance pull down output for hook relay control. The addition of the answer tone generator/detector and call progress tone detector makes the set-up of a telephone call much easier for the host µC to accomplish.

Very low power telemetry and data collection applications are supported by the CMX624's 'Zero Power' standby mode in which the device will detect telephone line ringing voltage or line voltage reversal events.

Pin compatible with the CMX644 Bell212A / V.22 modem, the CMX624 is available in the following packages: 24-pin SSOP (CMX624D5), 24-pin SOIC (CMX624D2), and 24-pin PDIP (CMX624P4).

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1 Block Diagram

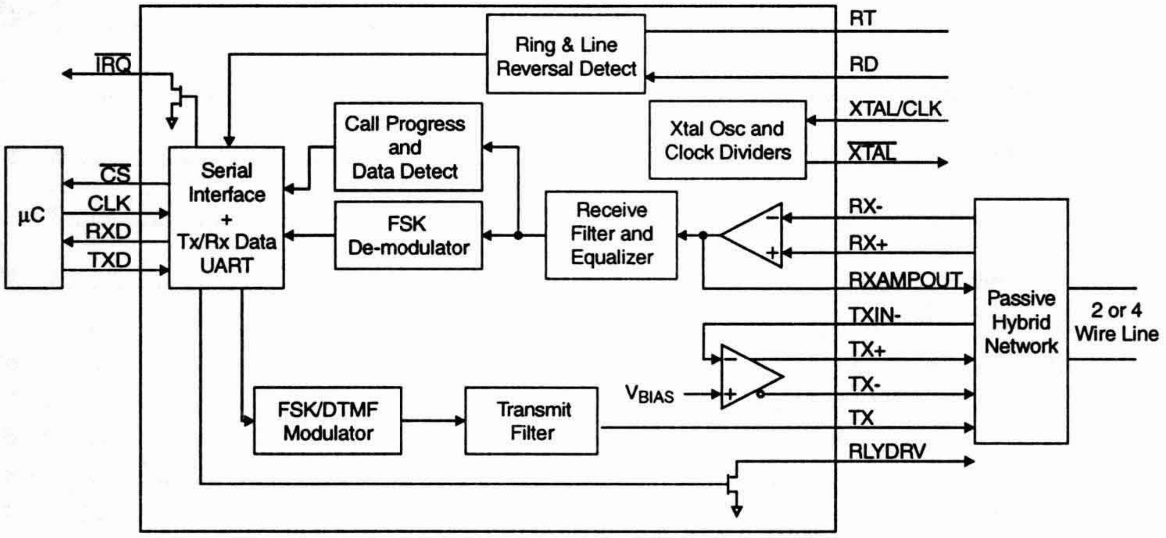

RT
RD
XTAL/CLK
XTAL
IRQ
CS
CLK
RXD
TXD
µC
Ring & Line Reversal Detect
Call Progress and Data Detect
Xtal Osc and Clock Dividers
Serial Interface + Tx/Rx Data UART
FSK De-modulator
Receive Filter and Equalizer
RX-
RX+
RXAMPOUT
TXIN-
TX+
TX-
TX
RLYDRV
Passive Hybrid Network
2 or 4 Wire Line
VBIAS
FSK/DTMF Modulator
Transmit Filter

Figure 1: Block Diagram

2 Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	input	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	SERIAL CLOCK	input	The serial interface clock input from the µC. See Section 4.1.
4	COMMAND DATA	input	The serial interface data input from the µC.
5	REPLY DATA	tri-state	A 3-state serial interface data output to the µC. This output is high impedance when not sending data to the µC.
6	$\overline{\text{CS}}$	input	The serial interface transfer control input provided by the µC.
7	$\overline{\text{IRQ}}$	output	A 'wire-ORable' output for connection to a µC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pullup resistor is required.
8	TX	output	The Tx analog signal output.
9	TX+	output	The output of the line driving amplifier.
10	TXIN-	input	The inverting input to the line driver amplifier.
11	TX-	output	The inverted output of the line driving amplifier.
12	V_{SS}	Power	The negative supply rail (ground).
13	V_{BIAS}	output	Internally generated bias voltage of $V_{DD}/2$, except when the device is in 'Zero Power' mode when V_{BIAS} will discharge to V_{SS}. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
14	RLYDRV	output	Relay drive open drain output. This output is pulled down to V_{SS} when active and is high impedance when inactive.
15	RX+	input	The non-inverting input to the Rx input amplifier.
16	RX-	input	The inverting input to the Rx input amplifier.
17	RXAMPOUT	output	The output of the Rx input amplifier.
18	RT	bidirectional	This pin is Bi-directional. An open drain output and Schmitt trigger input forming part of the Ring Signal detector.
19	RD	input	Schmitt trigger input to the Ring Signal Detector.
24	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
20, 21 22, 23		NC	No connection should be made to this pin.

Note: This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} should be bypassed. It is very important to protect the receive path from extraneous in-band signals. It is recommended that the printed circuit board be laid out with a ground plane in the CMX624 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} bypass capacitors.

3 External Components

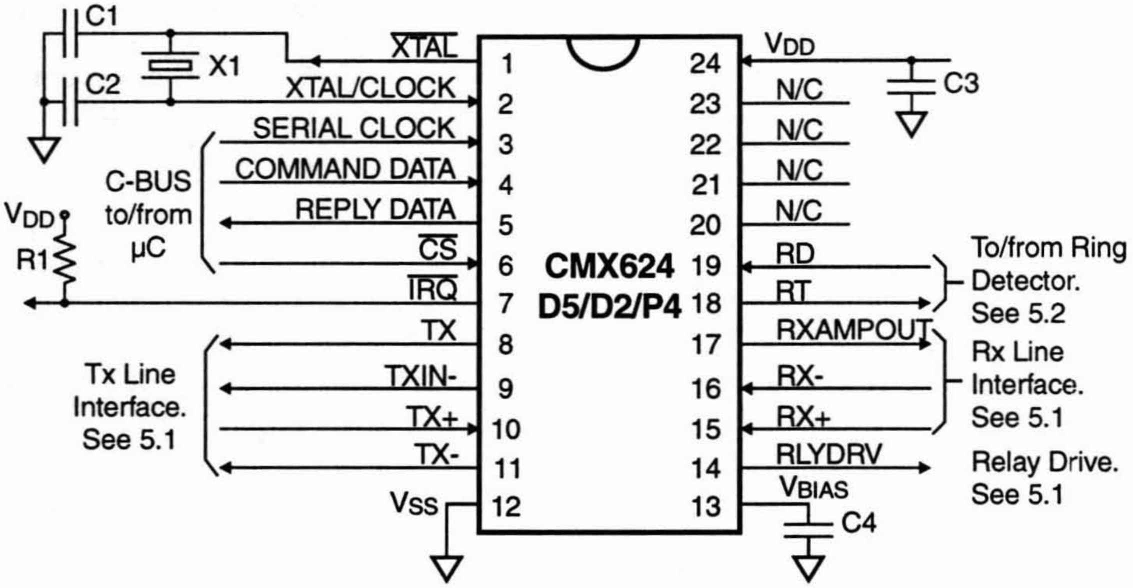

C1
C2
X1
XTAL
XTAL/CLOCK
SERIAL CLOCK
COMMAND DATA
REPLY DATA
CS
IRQ
C-BUS
to/from
µC
VDD
R1
TX
TXIN-
TX+
TX-
Tx Line
Interface.
See 5.1
VSS
CMX624
D5/D2/P4
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
N/C
N/C
N/C
N/C
RD
RT
RXAMPOUT
RX-
RX+
RLYDRV
VBIAS
C3
C4
To/from Ring
Detector.
See 5.2
Rx Line
Interface.
See 5.1
Relay Drive.
See 5.1

Figure 2: Recommended External Components

R1		100kΩ	±5%,
C1, C2		18pF	±10%
C3, C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Tolerances for Resistors and Capacitors are as indicated unless otherwise stated.

Table 1: Recommended External Components

Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult you crystal manufacturer.

4 General Description

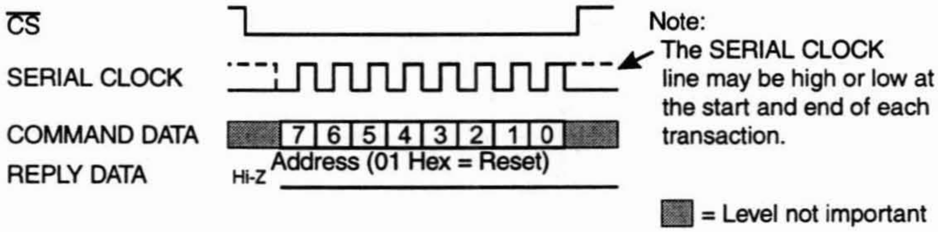
The CMX624 contains a Bell 202 and V.23 compatible FSK modem. This device is capable of duplex operation at 1200/75bps or 1200/150bps over a 2-wire line interface. It is also capable of 1200/1200bps over a 4-wire line interface. This device also contains a flexible FSK data UART, a receive FSK or Call Progress Tone energy detector, a 2100Hz detector, a DTMF generator, a Tx line driving buffer amplifier, a telephone line Ringing Signal or Line Voltage Reversal detector and a 3.579545MHz Xtal oscillator. These functions are controlled via a serial interface to the µC, which also carries the transmit and receive FSK modem data.

4.1 Serial Bus Interface

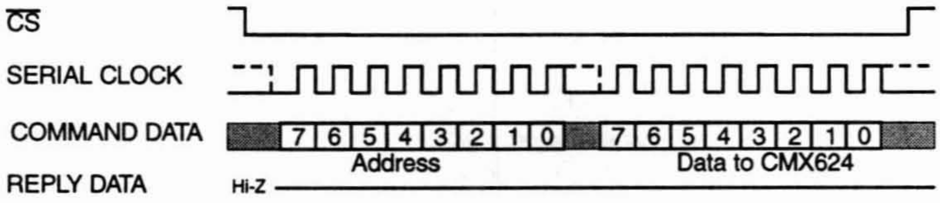
This block provides for the transfer of data and control or status information between the CMX624's internal registers and the µC over the serial interface bus. Each transaction, see Figure 3, consists of a single Register Address byte sent from the µC which may be followed by a single data byte sent from the µC to be written into one of the CMX624's Write Only Registers, or a single byte of data read out from one of the CMX624's Read Only Registers, as illustrated in Figure 3.

Data sent from the µC on the Command Data line is clocked into the CMX624 on the rising edge of the Serial Clock input. Reply Data sent from the CMX624 to the µC is valid when the Serial Clock is high. The interface is compatible with the most common µC serial interfaces such as SCI, SPI and Microwire, and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. See Figure 14 for detailed Serial Bus timing requirements.

a) Single byte from µC


CS
SERIAL CLOCK
COMMAND DATA
REPLY DATA
7 6 5 4 3 2 1 0
Address (01 Hex = Reset)
Hi-Z
Note:
The SERIAL CLOCK line may be high or low at the start and end of each transaction.
▨ = Level not important

b) One Address and one Data byte from µC


CS
SERIAL CLOCK
COMMAND DATA
REPLY DATA
7 6 5 4 3 2 1 0
Address
7 6 5 4 3 2 1 0
Data to CMX624
Hi-Z

c) One Address byte from µC and one Reply byte from CMX624

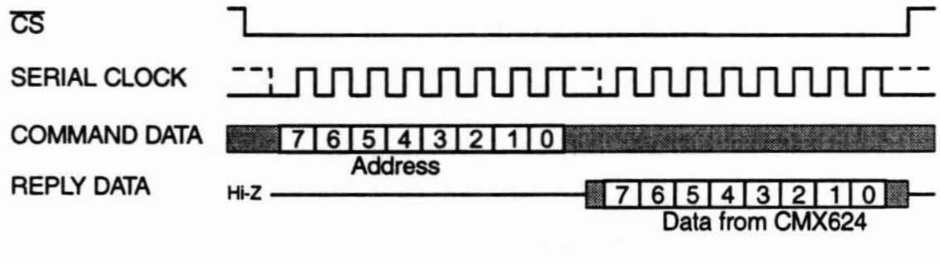

CS
SERIAL CLOCK
COMMAND DATA
REPLY DATA
7 6 5 4 3 2 1 0
Address
Hi-Z
7 6 5 4 3 2 1 0
Data from CMX624

Figure 3: Serial Bus Transactions

4.2 Software Description

4.2.1 Write Only Serial Bus Register

		Command Data Byte Bits							
Addr	Reg.	7	6	5	4	3	2	1	0
$01	RESET	SINGLE BYTE COMMAND							
$E0	SETUP	FSK mode: 0 = V.23 1 = Bell 202	TX- output: 0 = Off 1 = On	Relay Drive: 0 = o/c 1 = Pull low	0 = Zero Power 1 = Normal	Stop bits: 0 = 1 bit 1 = 2 bits	Parity: 0 = None 1 = Parity	Parity: 0 = Odd 1 = Even	Data bits: 0 = 8 bits 1 = 7 bits
$E1	TX TONES	Tx Mode: 0 = FSK. 1 = Tones.	Tone output: 0 = Off. 1 = On.	Reserved, set to 0	0 = DTMF 1 = Single tone	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Set Detect: 0 = FSK/CP 1 = 2100Hz
$E3	TX DATA	D7	D6	D5	D4	D3	D2	D1	D0
$E7	FSK MODE	0 = Rx Sync 1 = Async	Rx Equal: 0 = Off 1 = On	0 = Rx Call Progress 1 = Rx FSK	0 = Rx 75 / 150bps 1 = RX1200	0 = Tx Sync 1 = Async	Tx output level: 0 = Normal 1 = +3dB	FSK output: 0 = Off 1 = On	0 = Tx 75 / 150bps 1 = 1200
$EE	IRQ MASK	Reserved, Set to 0	Reserved, Set to 0	RT Change	Reserved, Set to 0	Rx Data overflow	Rx Data ready	Tx Data underflow	Tx Data ready

4.2.2 Read Only Serial Bus Registers

		Reply Data Byte Bits							
Addr	Reg.	7	6	5	4	3	2	1	0
$EA	RX DATA	D7	D6	D5	D4	D3	D2	D1	D0
$EF	FLAGS	Bad Rx Parity	Ring Detect	RT Change **	Rx Energy detect.	Rx Data overflow **	Rx Data ready **	Tx Data underflow **	Tx Data ready **

** See note 2 and 3

Notes:

1. Accessing the RESET Register over the Serial Bus clears all of the bits in the SETUP, TX TONES, TX DATA, FSK MODE and IRQ MASK registers, and Bits 0-3, 5 and 7 of the FLAGS Register to '0'. This will set the device into Zero Power mode.
2. This is a single-byte Serial Bus transaction consisting solely of the address byte value $01.
3. If any of Bits 0, 1, 2, 3 or 5 of the FLAGS Register is '1' and the corresponding bit of the IRQ MASK Register is also '1' then the $\overline{\text{IRQ}}$ output of the CMX624 will be pulled low.
4. Bit 5 (RT change) of the FLAGS Register is set on every '0' to '1' or '1' to '0' change of Bit 6 (Ring Detect).
5. Clearing Bit 4 of the SETUP Register puts the CMX624 into the Zero Power mode by turning off all blocks except for the Serial Bus interface and Ring Detector circuit.
6. Reading the FLAGS Register clears the $\overline{\text{IRQ}}$ output and also clears Bits 0, 1, 2, 3 and 5 of the FLAGS Register.

4.3 Xtal Oscillator

The frequency and timing accuracy of the CMX624 is determined by a 3.579545MHz clock signal input to the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 or may be supplied from an external source to the XTAL/CLOCK input. See Figure 2. If the clock is supplied from an external source, components C1, C2, and X1 should not be fitted.

The on-chip oscillator is disabled in the 'Zero-Power' mode.

If the clock is provided by an external source, which may not always be running, then the 'Zero-Power' mode must be enabled when the clock is not available. Failure to observe this rule may cause an increase in the supply current consumption by the CMX624.

4.4 Rx Input Amplifier

The Rx Input Amplifier, with suitable external components, is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits and may also form part of a 2-wire or 4-wire hybrid circuit. See Section 5.1.

4.5 Receive Filter

This block includes a bandpass filter whose characteristics are set by Bits 4 and 5 of the FSK MODE Register according to the receive operating mode (Call Progress, 75/150bps FSK or 1200bps FSK). It is used to attenuate out of band noise and interfering signals, especially the locally generated transmit FSK signal which could otherwise interfere with the received FSK signal when the modem is operating in 2-wire duplex mode. The FSK Demodulator block is enabled when Bit 5 of the FSK MODE Register is set to '1'. It converts the 75bps, 150bps or 1200bps FSK input signal to a binary received data signal which is sent to the Rx UART block.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

FSK mode Register $E7		TX Tone Register $E1	
Bit 5	Bit 4	Bit 0	RX MODE
1	1	0	RX FSK data at 1200 baud
1	0	0	Rx FSK data at 75/150 baud
0	X	0	RX Call progress Tones Detect
1	1	1	RX 2100Hz tone detect

Note: Other states are not defined and may result in unpredictable behavior

Table 2: Receive Mode

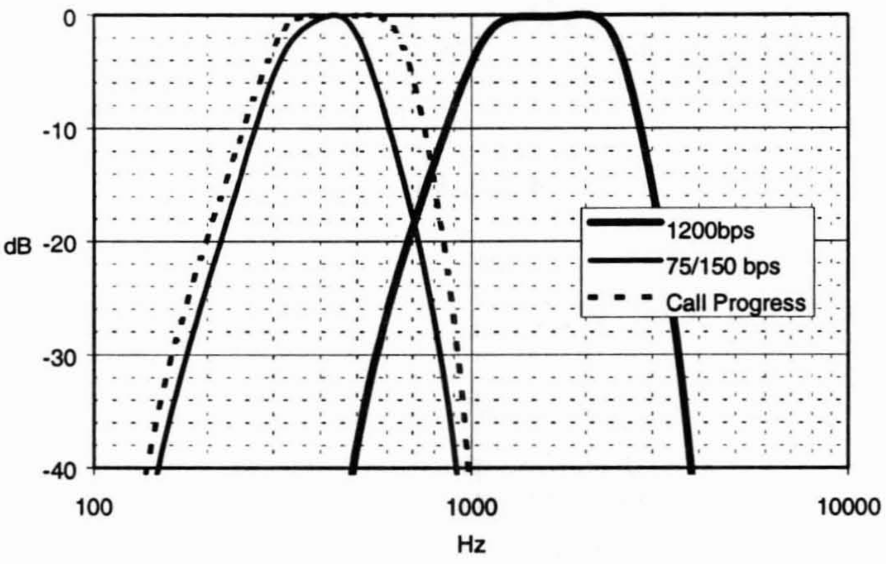


Figure 4 Rx Frequency Responses with Line Interface

The Rx Energy and 2100Hz Detector functional blocks are controlled by Bit 4 and Bit 5 of the FSK MODE Register and Bit 0 of the TX TONES Register.

This block will measure the frequency and amplitude of the incoming signal when Bit 0 of the TX TONES Register and Bit 4 and Bit 5 of the FSK MODE Register are set to '1'. When a signal of 2100Hz is present and of sufficient amplitude and time, Bit 4 of the FLAGS Register is set high. See Section 6.1 for amplitude, time and frequency limits.

When Bit 0 of the TX TONES Register is set to '0', this block compares the signal level at the output of the Receive Filter against an internal threshold. This may be used as a FSK level detector or a simple Call

Progress Signal detector, according to the settings of Bit 4 and Bit 5 of the FSK MODE Register, which affect the Receive Filter pass band as described in section 4.5.

Bit 4 of the FLAGS Register is set high by the output of this block when the received level has exceeded the threshold for sufficient time. Amplitude and time hysteresis, are used to reduce chattering in marginal conditions. See Section 6.1.

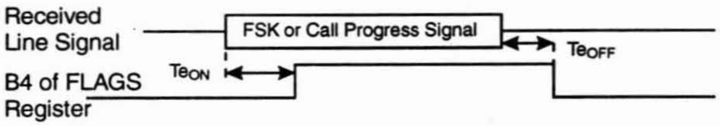


Figure 5: **Rx Energy Detector Timing**

4.6 Equalizer

When receiving 1200bps FSK data an optional equalizer section can be enabled by setting Bit 6 of the FSK MODE Register, compensates for one-half of the ETS Test Line 1 characteristics shown in Figure 6.

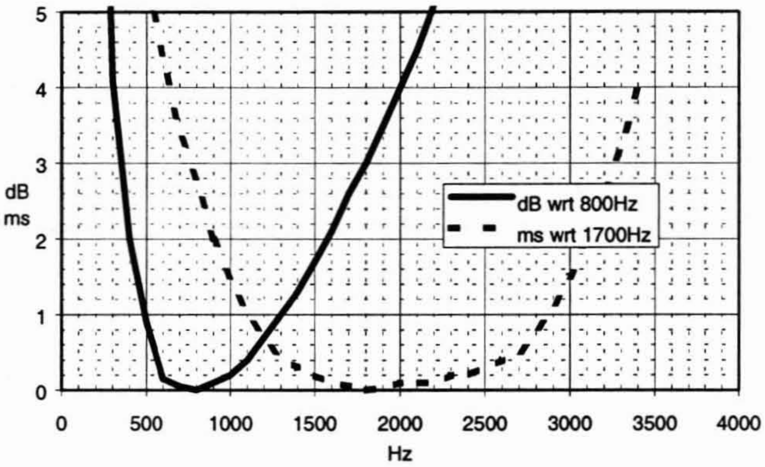


Figure 6: **ETS 300 114 Test Line 1 Characteristics (Normalized)**

4.7 FSK / DTMF Modulator

When Bit 7 of the TX TONES Register is set to '0' then the FSK/DTMF Modulator generates FSK signals as determined by Bit 0 and Bit 1 of the FSK MODE Register and the Tx data bits from the UART block as shown in Table 3 and Table 4.

4.7.1 V.23 mode (Bit 7 of SETUP register = '0'):

FSK MODE Reg		FSK / DTMF Modulator block output	FSK Signal Frequency	
Bit 1	Bit 0	(Bit 7 of TX TONES = '0')	'0' (Space)	'1' (Mark)
0	x	Disabled (output held at $V_{DD}/2$)		
1	0	75bps FSK	450Hz	390Hz
1	1	1200bps FSK	2100Hz	1300Hz

Table 3: **V.23 mode (Bit 7 of SETUP register = '0')**

4.7.2 Bell 202 mode (Bit 7 of SETUP register = ‘1’):

FSK MODE Reg		FSK / DTMF Modulator block output (Bit 7 of TX TONES = ‘0’)	FSK Signal Frequency	
Bit 1	**Bit 0**		**‘0’ (Space)**	**‘1’ (Mark)**
0	x	Disabled (output held at $V_{DD}/2$)		
1	0	150bps FSK	487Hz	387Hz
1	1	1200bps FSK	2200Hz	1200Hz

Table 4: Bell 202 mode (Bit 7 of SETUP register = ‘1’)

When Bit 7 of the TX TONES Register is set to ‘1’, the block generates DTMF tone parts or single tones from the DTMF range as shown in Table 5. Bit 6 of the TX TONES Register is then used to enable or disable the block’s output to the Tx filter.

TX DATA Register				TX TONES Register			
Bits 0 - 3				**DTMF Tone Pairs (Bit 4 = ‘1’)**			**Single Tone (Bit 4 = ‘0’)**
D3	**D2**	**D1**	**D0**	**Lower Frequency (Hz)**	**Upper Frequency (Hz)**	**Keypad Legend**	**Single Tone Frequency (Hz)**
0	0	0	0	941	1633	D	1633
0	0	0	1	697	1209	1	1209
0	0	1	0	697	1336	2	1336
0	0	1	1	697	1477	3	1477
0	1	0	0	770	1209	4	1209
0	1	0	1	770	1336	5	1336
0	1	1	0	770	1477	6	1477
0	1	1	1	852	1209	7	1209
1	0	0	0	852	1336	8	852
1	0	0	1	852	1477	9	852
1	0	1	0	941	1336	0	941
1	0	1	1	941	1209	*	941
1	1	0	0	941	1477	#	941
1	1	0	1	697	1633	A	697
1	1	1	0	770	1633	B	770
1	1	1	1	852	1633	C	852

Table 5: DTMF Transmitting settings

4.8 Transmit Filter

This stage attenuates out of band signals present at the output of the FSK/DTMF modulator and also includes a programmable 3dB level switch, selected by Bit 2 of the FSK MODE Register.

The nominal output levels at the TX pin when V_{DD} = 5.0V are as shown below.

FSK MODE Register Bit 2	FSK Signal	DTMF Tone (Low group)	DTMF Tone (High group)
0 (low level)	-6dB	-5dB	-3dB
1 (high level)	-3dB	-2dB	0dB

0dB = 775mV$_{RMS}$

Table 6: Transmit Filter

These levels are proportional to V_{DD}, and the actual transmit signal levels present on the 2- or 4-wire line will depend on the external circuitry as described in section 5.1. Using the external components recommended in section 5.1 for a nominal FSK transmit level of -9dBm, DTMF tone levels of -8dBm and -6dBm, then the out of band energy sent to the line will be within the limits shown in Figure 7 for both FSK and DTMF signals.

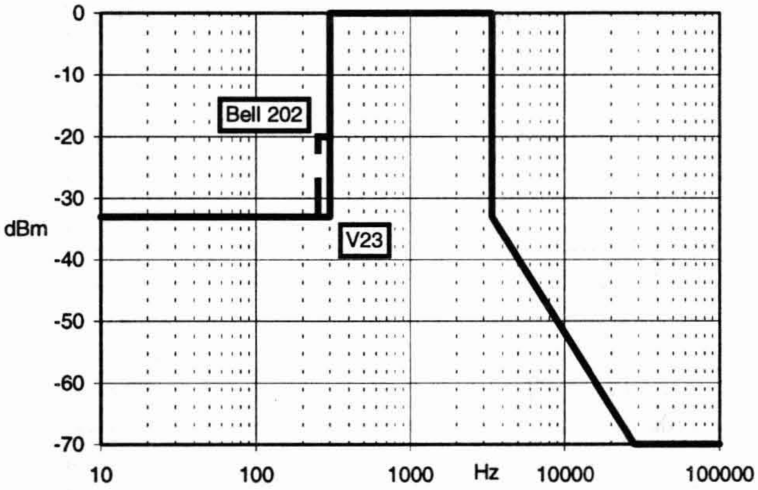


Figure 7: Maximum Out of Band Tx Line Energy Limits

4.9 Transmit Output Buffer

This buffer amplifier, connected to the TXIN-, TX+ and TX- pins, is intended for use as a Tx line driver as shown in section 5.1. Two symmetrical outputs are provided for use with a balanced load to give sufficient Tx line signal levels even at low V_{DD}. If this is not required the TX- output can be disabled.

If the buffer is used as a balanced line driver, then Bit 6 of the SETUP Register should be set to '1' (TX- output enabled). Setting Bit 6 to '0' disables the TX- output and the buffer draws less current from the supply. When Bit 6 is set to '0' the TX- pin should be left open circuit. N.B. The TX+ output is unaffected by this Bit.

4.10 Ring Signal Detector

This block, which functions even in Zero Power mode, can be used to detect a telephone line Ring Signal or Line Voltage Reversal and then generate a Interrupt Request signal to wake up the µC at the start of a call. Suitable interface circuits are shown in section 5.2.

The output of this block is the 'Ring Detect' line shown in Figure 1 which directly drives Bit 6 of the FLAGS Register. Any '0' to '1' or '1' to '0' change on this line will also set the 'RT Change' Bit (5) of the FLAGS Register.

If this block is not used, then the RD and RT pins should be connected to V_{SS} and the 'RT Change' Bit (5) of the IRQ MASK Register set to '0'.

4.11 Tx/Rx UART

This block connects the µC, via the Serial Bus interface, to the received data from the FSK Demodulator and to the transmit data input to the FSK Modulator.

As part of this function, the block can be programmed to convert data to be transmitted from 7 or 8-Bit bytes to asynchronous data characters, adding Start and Stop bits and - optionally - a parity bit to the data before passing it to the FSK Modulator. Similarly, in the receive direction it can extract data bits from asynchronous characters coming from the FSK Demodulator, stripping off the Start and Stop bits and performing an optional Parity check on the received data before passing the result over the Serial Bus to the µC. Bits 0-3 of the SETUP Register control the number of Stop and Data bits and the Parity options for both receive and transmit directions.

Data to be transmitted should be loaded by the µC into the TX DATA Register when the Tx Data Ready bit (Bit 0) of the FLAGS Register goes high. It will then be treated by the Tx UART block in one of two ways, depending on the setting of Bit 3 of the FSK MODE Register:

1. If the bit is '0' ('Tx Sync' mode) then the 8 bits from the TX DATA Register will be transmitted sequentially at 75bps, 150bps, or 1200bps, lsb (D0) first.
2. If Bit 3 of the FSK MODE Register is '1' ('Tx Async') then bits will be transmitted as asynchronous data characters at 75bps, 150bps, or 1200bps according to the following format:
    A. One Start bit (Space).
    B. 7 or 8 Data bits from the TX DATA Register (D0-D6 or D0-D7) as determined by Bit 0 of the SETUP Register. LSB (D0) transmitted first.
    C. Optional Parity bit (even or odd parity) as determined by Bits 1 and 2 of the SETUP Register.
    D. One or Two Stop bits (Mark) as determined by Bit 3 of the SETUP Register.

In both cases data will only be transmitted if Bit 1 of the FSK MODE Register is set to '1'.

Failure to load the TX DATA Register with a new value when required will result in Bit 1 (Tx Data Underflow) of the FLAGS Register being set to '1' and if the 'Tx Async' mode of operation had been selected then a continuous Mark ('1') signal will then be transmitted until a new value is loaded into TX DATA, whereas in 'Tx Sync' mode the byte already in the TX DATA Register will be re-transmitted.

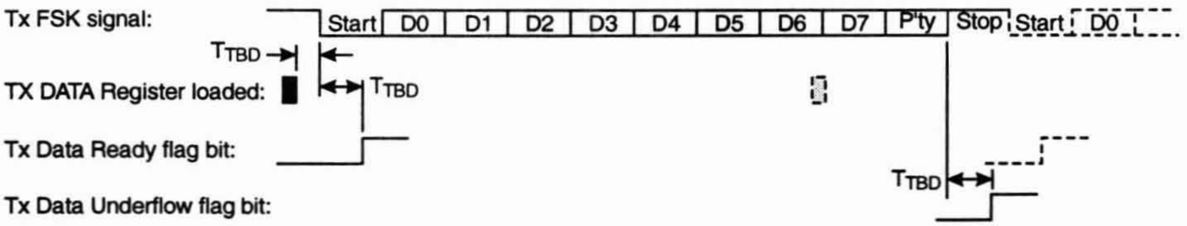


Figure 8: Transmit UART Function (Async)

Received data from the FSK Demodulator goes into the receive part of the UART block, where it is handled in one of two ways depending on the setting of Bit 7 of the FSK MODE Register:

1. If the bit is '0' ('Rx Sync' mode) then the receive part of the UART block will simply take 8 consecutive bits from the Demodulator and transfer them to the RX DATA Register (the first bit going into the D0 position).

    Note: This mode is intended for detection of simple data patterns such as '1010...' or continuous Mark or Space signals, the CMX624's receive data clock extraction circuits are not adequate to support a true synchronous receive data mode of operation.
2. If Bit 7 of the FSK MODE Register is '1' (' Rx Async') then the received data output of the FSK Demodulator is treated as 75, 150 or 1200bps asynchronous characters each comprising:
    A. A Start bit (Space).
    B. 7 or 8 Data bits as determined by Bit 0 of the SETUP Register. These bits will be placed into the RX DATA Register with the first bit received going into the D0 position.
    C. An optional Parity bit as determined by Bits 1 and 2 of the SETUP Register. If Parity is enabled (Bit 2 of the SETUP Register = '1') then Bit 7 of the FLAGS Register will be set to '1' if the received parity is incorrect.
    D. At least one Stop bit (Mark).

Bit 2 (Rx Data Ready) of the FLAGS Register will be set to '1' every time a new received value is loaded into the RX DATA Register. If the previous contents of the RX DATA Register had not been read out over the Serial Bus before the new value is loaded from the UART then Bit 3 (Rx Data Overflow) of the FLAGS Register will also be set to '1'.

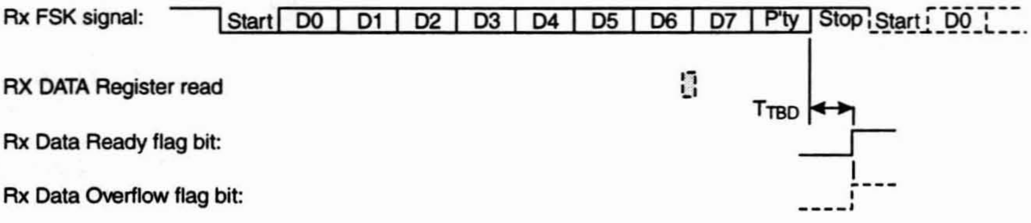

Rx FSK signal:
Start
D0
D1
D2
D3
D4
D5
D6
D7
P'ty
Stop
Start
D0
RX DATA Register read
T_{TBD}
Rx Data Ready flag bit:
Rx Data Overflow flag bit:

Figure 9: Receive UART Function (Async)

5 Application Notes

5.1 Line Interface

A line interface circuit is needed to provide DC isolation between the modem and the line, to perform line impedance termination, and to set the correct transmit and receive signal levels.

5.1.1 4-Wire Line Interface

Figure 10 shows an interface circuit for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R15, while R11 and R13 should be selected to give the desired transmit and receive levels.

5.1.1.1 Receive Gain

When $V_{DD} = 5.0V$, the gain of the receive input amplifier (R12 / R11) should just compensate for the loss of the input transformer, so that the signal level at pin RXAMPOUT is the same as that on the 4-wire receive line. At other values of V_{DD} the amplifier gain should be multiplied by the ratio $V_{DD} / 5$. Thus for R12 = 100kΩ

$$R11 = \frac{100k\Omega \times \frac{V_{DD}}{5.0}}{(\text{Input transformer loss})}$$

where the 'Input transformer loss' = (Rx level on 4-wire line) / (level at point A of Figure 10).

Assuming a transformer loss of about 1dB, R11 should be 91kΩ at $V_{DD} = 5.0V$, rising to 130kΩ at 3.3V

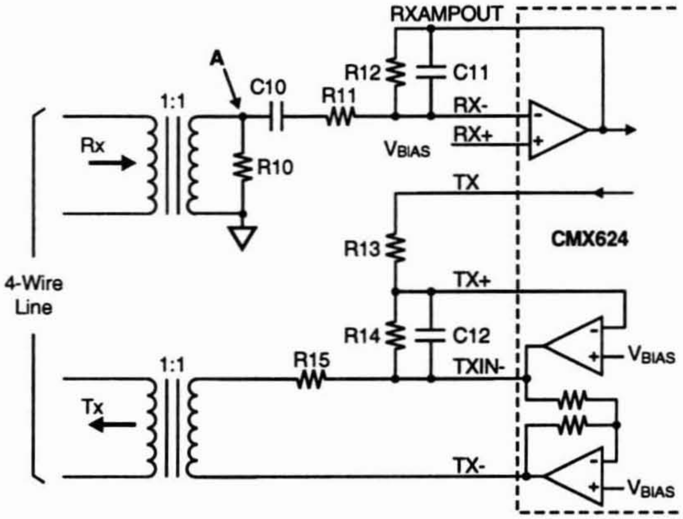


Figure 10: 4-Wire Line Interface Circuit

R10	Note 1	600Ω	±1%
R11	Note 1	See text	±1%
R12	Note 1	100kΩ	±1%
R13	Note 1	See text	±1%
R14	Note 1	100kΩ	±1%

R15	Note 1	600Ω	±1%
C10	Note 1	TBD	±20%
C11	Note 1	330pF	±20%
C12	Note 1	330pF	±20%

Tolerances for Resistors and Capacitors are as indicated unless otherwise stated.

Table 7: 4-Wire Line Interface Circuit components

Note:

1. The relay circuit, AC and DC loads and line protection are not shown for clarity

5.1.1.2 Transmit Gain

In the transmit direction, the level on the 4-wire line is determined by the level at the TX pin, the gain of the Output Buffer Amplifier, a loss of nominally 6dB due to the line termination resistor R15, and the loss in the transformer.

The TX pin signal level is proportional to V_{DD} and is also affected by the setting of the Tx output level control Bit (Bit 2) of the FSK Mode Register.

Assuming that the Tx output level control bit is set to '1' (giving a FSK signal level of -3dB with respect to $775mV_{RMS}$ at the TX pin when V_{DD} = 5.0V) and that there is 1dB loss in the transformer, then:

$$\text{Tx FSK 4 - wirel line level} = -\left(3+6+1\right) + 20 \times \text{LOG}_{10}\left(\frac{2 \times R14}{R13}\right) + 20 \times \text{LOG}_{10}\left(\frac{V_{DD}}{5.0}\right) \text{dBm}$$

For example, to generate a nominal Tx FSK line level of -9dBm, R13 should be 180kΩ when V_{DD} = 5.0V, falling to 120kΩ at 3.3V.

5.1.2 2-Wire Line Interface

Figure 11 shows an interface circuit suitable for connection to a 600Ω 2-wire line. The circuit also shows how a relay may be driven from the RLYDRV pin.

Note: When the CMX624 is powered from less than 5.0V, buffer circuitry may be required to drive a 5V relay.

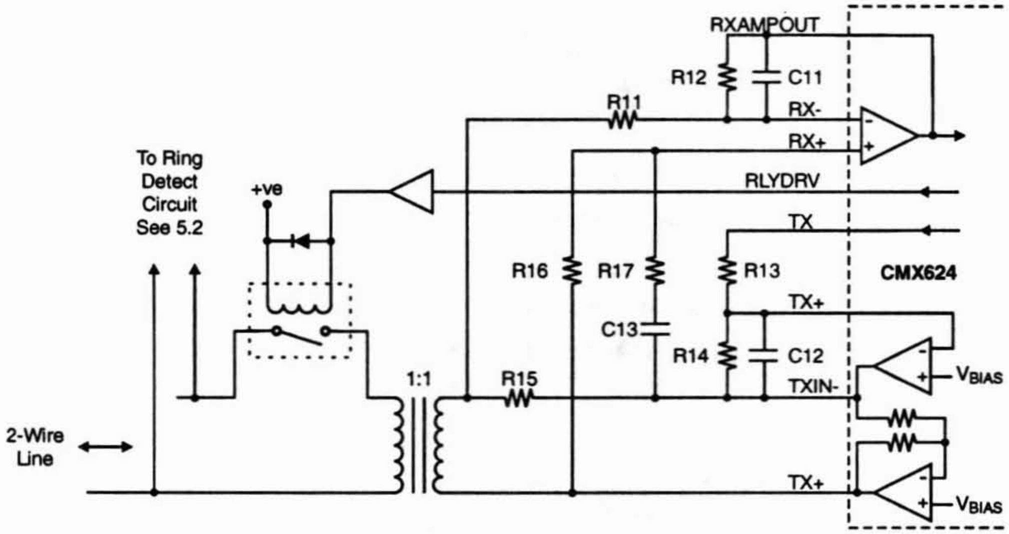

RXAMPOUT
R12
C11
R11
RX-
RX+
To Ring Detect Circuit See 5.2
+ve
RLYDRV
TX
R16
R17
R13
CMX624
TX+
C13
R14
C12
1:1
R15
TXIN-
VBIAS
2-Wire Line
TX+
VBIAS

Figure 11: 2-Wire Line Interface Circuit

R11		See text	±1%
R12		100kΩ	±1%
R13		See text	±1%
R14		100kΩ	±1%
R15		600Ω	±1%

R16		120kΩ	±1%
R17		100kΩ	±1%
C11		330pF	±20%
C12		330pF	±20%
C13		10nF	±20%

Tolerances for Resistors and Capacitors are as indicated unless otherwise stated.

Table 8: 2-Wire Line Interface Circuit components

Note:

1. The relay circuit, AC and DC loads and line protection are not shown for clarity

This circuit includes a 2-wire to 4-wire hybrid circuit, formed by R11, R15, R16, R17, C13 and the impedance of the line itself, which ensures that the modem receive input and transmit output paths are both coupled efficiently to the line, while minimizing coupling from the modem's transmit signal into the receive input.

The values of R11 and R13 should be calculated in the same way as for the 4-wire interface circuit of Figure 10.

5.2 Ring Detector Interface

Figure 12 shows how the CMX624 may be used to detect large amplitude Ringing signals received at the start of an incoming telephone call.

The ring signal is applied at the subscriber's exchange as an AC voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 in a rectified and attenuated form. See point X in Figure 12.

The signal at point X is further attenuated by the R22 and R23 divider before being applied to the RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vt_{HI}) of Schmitt trigger 'A' then the transistor (Q1) connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 6 (Ring Detect) of the FLAGS register.

The minimum amplitude ringing signal that is certain to be detected is found by the following calculation:

$$\left(\frac{0.7 + Vt_{HI} \times [R20 + R22 + R23]}{R23}\right) \times 0.707 V_{RMS} = \text{Min. Ring Signal } V_{RMS}$$

where Vt_{HI} is the high-going threshold voltage of the Schmitt trigger A. See Figure 13 and Section 6.1.3.

With R20-22 at 470kΩ as shown Figure 12, then setting R23 to 68kΩ will guarantee detection of ringing signals of $40V_{RMS}$ and above for V_{DD} over the range 3.0 to 5.5V.

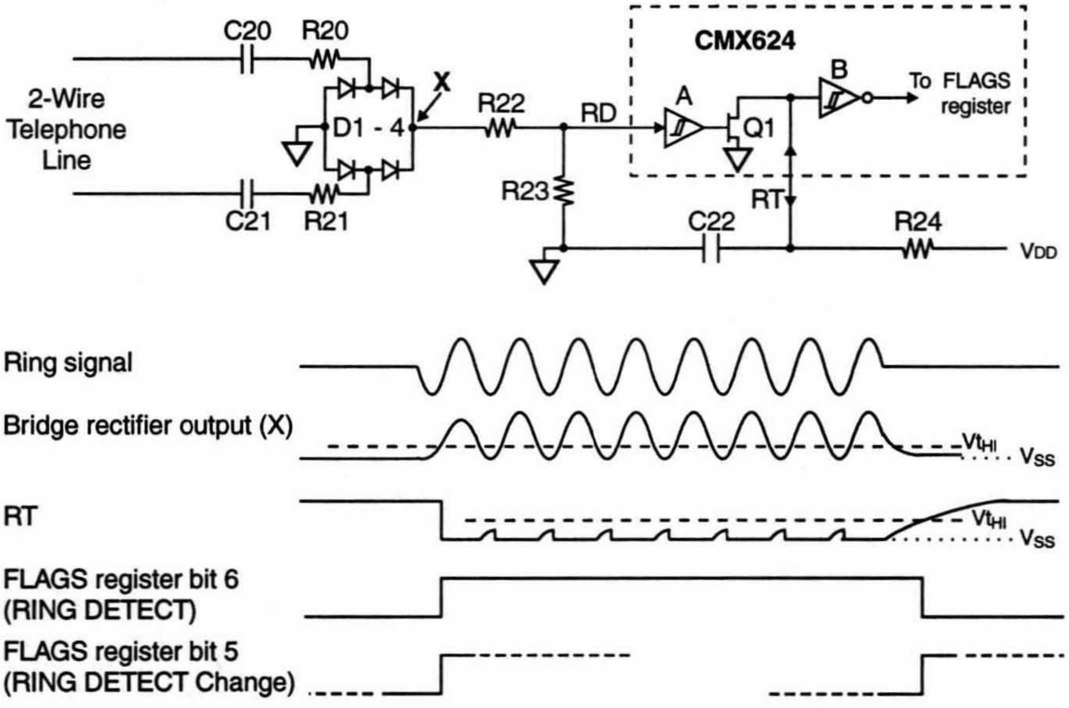

C20
R20
2-Wire
Telephone
Line
D1 - 4
X
R22
RD
CMX624
A
Q1
B
To FLAGS
register
R23
C21
R21
C22
RT
R24
VDD
Ring signal
Bridge rectifier output (X)
Vt_HI
Vss
RT
Vt_HI
Vss
FLAGS register bit 6
(RING DETECT)
FLAGS register bit 5
(RING DETECT Change)

Figure 12: Ring Signal Detector Interface Circuit

R20,21,22		470kΩ	±1%
R23		See text	±1%
R24	Note 1	470kΩ	±1%

C20,21		0.1μF	±20%
C22	Note 1	0.33μF	±20%
D1-4		1N4004	±20%

Tolerances for Resistors and Capacitors are as indicated unless otherwise stated.

Table 9: Ring Signal Detector Interface Circuit components

Note:

1. If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

   The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula:

   $$V_{RT} = V_{DD}\left[1 - e^{\frac{-t}{RC}}\right] \qquad t = -RC\left[\ln\left(1 - \frac{V_{RT}}{V_{DD}}\right)\right]$$

   As the Schmitt trigger high-going input threshold voltage (Vt_{HI}) has a minimum value of 0.56 x V_{DD}, then the Schmitt trigger B output will remain high for a time of at least 0.821 x R24 x C22 following a pulse at RD.

   The values of R24 and C22 given in Figure 12 (470kΩ and 0.33µF) give a minimum RT charge time of 100ms, which is adequate for ring frequencies of 10Hz or above.

Note: The circuit will also respond to a telephone line voltage reversal. If necessary the µC can distinguish between a Ring signal and a line voltage reversal by measuring the time that bit 6 of the FLAGS register (Ring Detect) is high.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-50	50	mA
V_{SS}	-50	50	mA
Any other pin	-20	20	mA
RLYDRV pin		50	mA
D2 / P4 Package	Min.	Max.	Unit
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
D5 Package	Min.	Max.	Unit
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Notes: A Xtal frequency of 3.579545MHz ±0.1% is required for correct operation.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 2.7V at T_{AMB} = 25°C and V_{DD} = 3.0V to 5.5V at T_{AMB} = -40 to 85°C,
Xtal Frequency = 3.579545MHz ± 0.1%, 0dBm corresponds to 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Unit
DC Parameters					
I_{DD} (Zero Power mode)	1, 2		1.0		μA
(Running, TX- output Off, V_{DD}= 5.0V)	1		2.6	TBD	mA
(Running, TX- output Off, V_{DD}= 3.3V)	1		1.7	TBD	mA
(Running, TX- output On, V_{DD}= 5.0V)	1		3.0	TBD	mA
(Running, TX- output On, V_{DD}= 3.3V)	1		2.0	TBD	mA
Logic '1' Input Level	3	70%			V_{DD}
Logic '0' Input Level	3			30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0		1.0	μA
Output Logic '1' Level (I_{OH} = 360μA)		V_{DD}-0.4			V
Output Logic '0' Level (I_{OL} = 360μA)				0.4	V
$\overline{IRQ}$ OUTPUT 'Off' State Current (V_{OUT} = V_{DD})				1.0	μA
Schmitt trigger input high-going threshold (Vt_{HI}) (see Figure 13)		(0.56)V_{DD}		(0.56)V_{DD} + 0.6V	V
Schmitt trigger input low-going threshold (Vt_{LO}) (see Figure 13)		(0.44)V_{DD} - 0.6V		(0.44)V_{DD}	V
RLYDRV 'ON' resistance to V_{SS} (V_{DD}= 5.0V)				TBD	Ω
FSK Modulator and Tx UART					
Level at TX pin.	4	-4.0	-3.0	-2.0	dBm
Twist (Mark level WRT Space level)		-2.0	0	2.0	dB
Tx 1200bps (V.23 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1297	1300	1303	Hz
Space (Logical 0) Frequency		2097	2100	2103	Hz
Tx 75bps (V.23 mode)					
Baud Rate (set by UART and Xtal frequency)		74	75	76	Baud
Mark (Logical 1) Frequency		388	390	392	Hz
Space (Logical 0) Frequency		448	450	452	Hz
Tx 1200bps (Bell 202 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1197	1200	1203	Hz
Space (Logical 0) Frequency		2197	2200	2203	Hz
Tx 150bps (Bell 202 mode)					
Baud Rate (set by UART and Xtal frequency)		149	150	151	Baud
Mark (Logical 1) Frequency		385	387	389	Hz
Space (Logical 0) Frequency		485	487	489	Hz

	Notes	Min.	Typ.	Max.	Unit
DTMF Transmitter					
Level at TX pin; tones in High Group	4	-1.0	0.0	1.0	dBm
Twist (level of High Group tones with respect to level of Low Group tones)			2.0		dB
Tone frequency accuracy (worst case)		-0.5		0.5	%
Tx Filter and Output Buffer					
Change in level at TX pin caused by changing Bit 2 of FSK MODE Register		2.5	3.0	3.5	dB
Buffer output signal swing; Load ≥ 500Ω.	5	2.2			V_{P-P}
FSK Demodulator and Rx UART					
Valid Input Level Range	6	-43.0		-9.0	dBm
Acceptable Twist (Mark level with respect to Space level)		-7.0		7.0	dB
Acceptable Signal to Noise Ratio	7	20.0		-	dB
Rx 1200bps (V.23 mode)					
Acceptable Rx Data Rate	8	1188	1200	1212	Baud
Mark (Logical 1) Frequency		1280	1300	1320	Hz
Space (Logical 0) Frequency		2068	2100	2132	Hz
Rx 75bps (V.23 mode)					
Acceptable Rx Data Rate	8	TBD	75	TBD	Baud
Mark (Logical 1) Frequency		TBD	390	TBD	Hz
Space (Logical 0) Frequency		TBD	450	TBD	Hz
Rx 1200bps (Bell 202 mode)					
Acceptable Rx Data Rate	8	1188	1200	1212	Baud
Mark (Logical 1) Frequency		1180	1200	1220	Hz
Space (Logical 0) Frequency		2168	2200	2232	Hz
Rx 150bps (Bell 202 mode)					
Acceptable Rx Data Rate	8	TBD	150	TBD	Baud
Mark (Logical 1) Frequency		TBD	387	TBD	Hz
Space (Logical 0) Frequency		TBD	487	TBD	Hz
2100Hz Detector					
'Will Decode' Frequency Range		2040		2235	Hz
'Will Not Decode' Frequency Range		<2010		>2265	Hz
'Off' to 'On' time	9			25	ms
'On' to 'Off' time	9	4.0			ms
Rx Energy Detector					
'Off' to 'On' Threshold Level	6, 10	-48.0		-43.0	dBm
Hysteresis	6, 10	2.0			dB
'Off' to 'On' Time (Figure 5 Te_{ON}):	6, 10				
1200bps Rx mode				25	ms
75/150bps Rx mode				48	ms
Call Progress Detect mode				48	ms
'On' to 'Off' Time (Figure 5 Te_{OFF}):	6, 10				
1200bps Rx mode		8.0			ms
75/150bps Rx mode		20			ms
Call Progress Detect mode		20			ms

	Notes	Min.	Typ.	Max.	Unit
XTAL/CLOCK Input					
'High' Pulse Width	11	100			ns
'Low' Pulse Width	11	100			ns

Notes:

1. At 25°C, not including any current drawn from the CMX624 pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for RT and $\overline{CS}$ inputs, which are at V_{DD}.
3. Excluding RD, RT and XTAL/CLOCK pins.
4. At V_{DD} = 5.0V, Tx output level control bit set to 'High'; load resistance greater than 40kΩ.
5. For each of the TX- (if enabled) and TX+ pins, load between pin and $V_{DD}/2$.
6. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for V_{DD} = 5.0V.
   The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1.
7. Flat noise in 300-3400 Hz band for V.23, 200-3400 Hz for Bell 202.
8. Set by Rx UART and Xtal frequency.
9. 2100Hz detection requires a signal within the amplitude range given in section 4.5.
10. Measured with 1300Hz signal in 1200bps mode, 390Hz for 75bps or 150bps and Call Progress mode, signal level -33dBm for time delay measurements.
11. Timing for an external input to the XTAL/CLOCK pin.

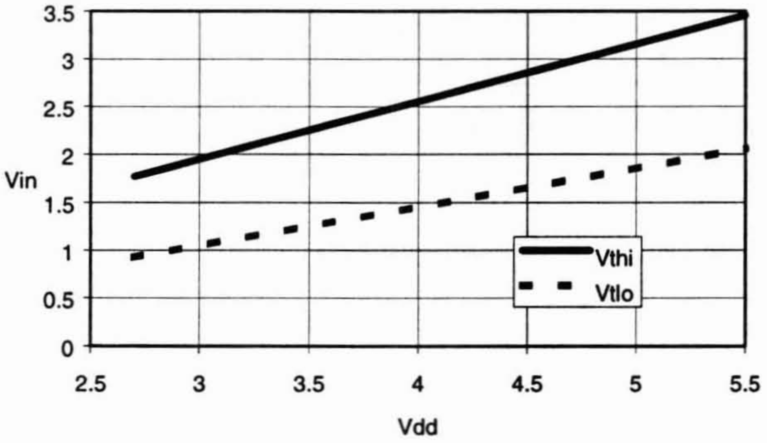


Figure 13: Typical Schmitt Trigger Input Voltage Thresholds vs. V_{DD}

6.1.4 Timing

Serial Bus Timings	Description	Notes	Min.	Typ.	Max.	Unit
t_{CSE}	$\overline{CS}$ -Enable to Clock-High time		100			ns
t_{CSH}	Last Clock-High to $\overline{CS}$-High time		100			ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0			ns
t_{HIZ}	$\overline{CS}$-High to Reply Output 3-state time				1.0	µs
t_{CSOFF}	$\overline{CS}$-High Time between transactions		1.0			µs
t_{NXT}	Inter-Byte Time		200			ns
t_{CK}	Clock-Cycle time		200			ns
t_{CH}	Serial Clock-High time		100			ns
t_{CL}	Serial Clock-Low time		100			ns
t_{CDS}	Command Data Set-Up time		75			ns
t_{CDH}	Command Data Hold time		25			ns
t_{RDS}	Reply Data Set-Up time		75			ns
t_{RDH}	Reply Data Hold time		0			ns

Note: These timings are for the latest version of the Serial Bus as embodied in the CMX624, and allow faster transfers than the original Serial Bus.

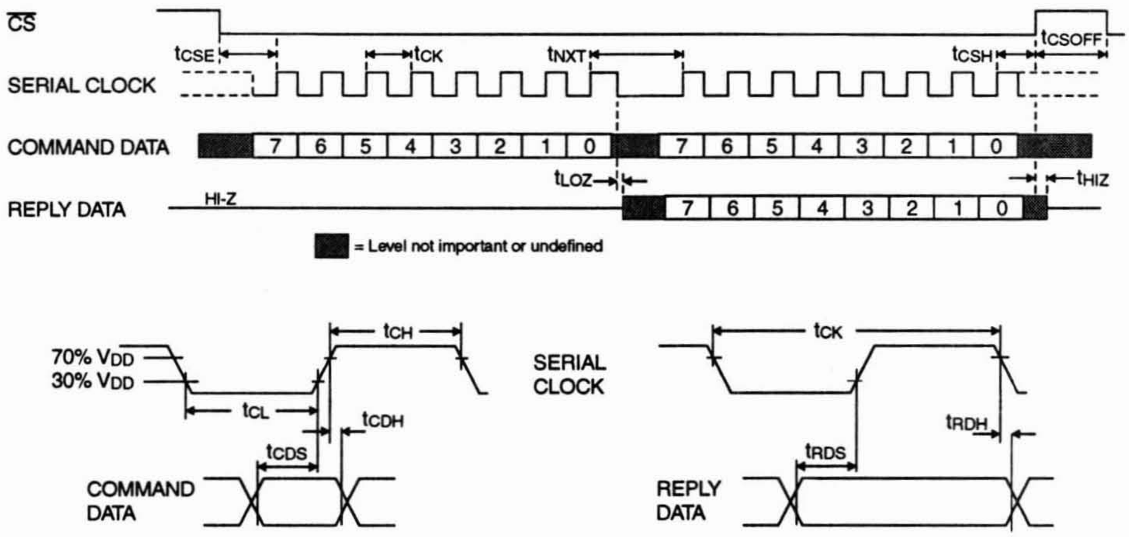
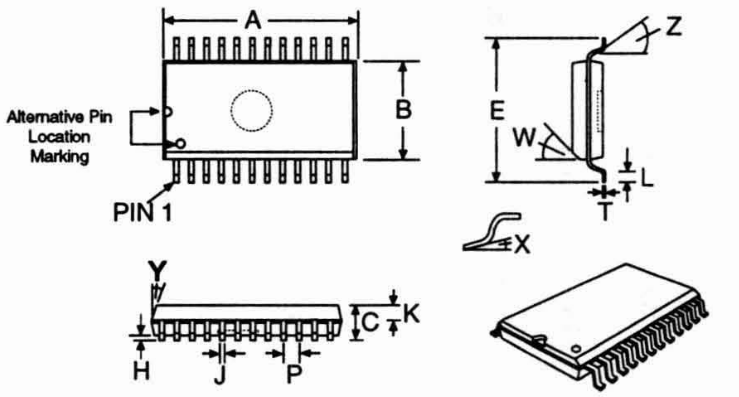

$\overline{CS}$
tCSE
tCK
tNXT
tCSH
tCSOFF
SERIAL CLOCK
COMMAND DATA
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0
tLOZ
tHIZ
REPLY DATA
HI-Z
7 6 5 4 3 2 1 0
= Level not important or undefined
70% VDD
30% VDD
tCH
tCL
tCDH
tCDS
COMMAND DATA
SERIAL CLOCK
tCK
tRDH
tRDS
REPLY DATA

Figure 14: Serial Bus Timing

6.2 Packaging

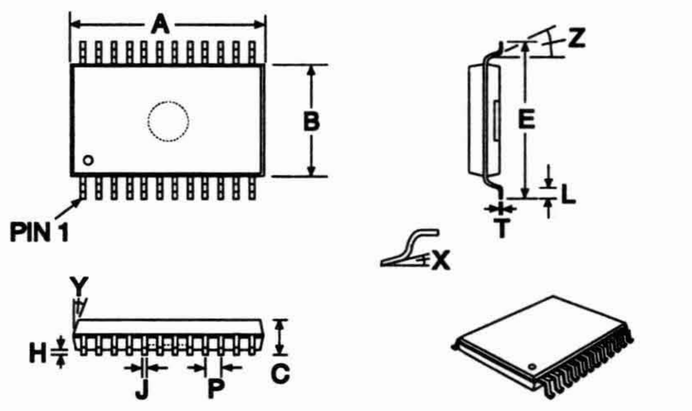


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin SOIC (D2) Mechanical Outline: *Order as part no. CMX624D2*

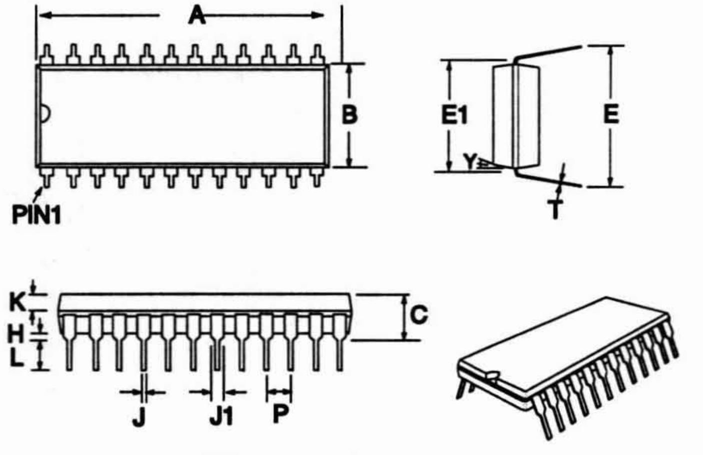


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin SSOP (D5) Mechanical Outline: *Order as part no. CMX624D5*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin PDIP (P4) Mechanical Outline: ***Order as part no. CMX624P4***

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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX631A

Low Voltage SPM Detector

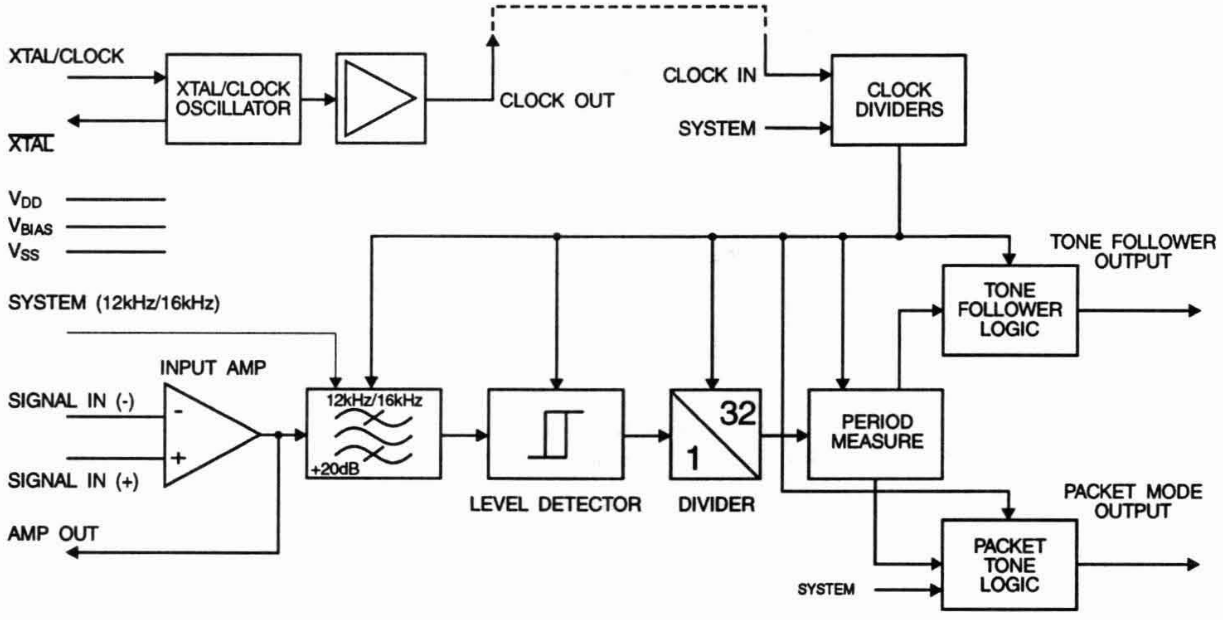
PRELIMINARY INFORMATION

Features

- **Detects 12kHz or 16kHz SPM Frequencies**
- **Tone Follower and Packet Mode Outputs**
- **High Speech-Band Rejection Properties**
- **Low Power Operation (3.0V < 0.8mA)**

Applications

- **Call Charge Applications on PABX Line Cards**
- **Complex and/or Simple telephone Systems**
- **Remote Telephone/Payphones**


XTAL/CLOCK
XTAL/CLOCK OSCILLATOR
$\overline{\text{XTAL}}$
CLOCK OUT
CLOCK IN
SYSTEM
CLOCK DIVIDERS
V_{DD}
V_{BIAS}
V_{SS}
SYSTEM (12kHz/16kHz)
INPUT AMP
SIGNAL IN (-)
SIGNAL IN (+)
AMP OUT
12kHz/16kHz
+20dB
LEVEL DETECTOR
32
1
DIVIDER
PERIOD MEASURE
TONE FOLLOWER OUTPUT
TONE FOLLOWER LOGIC
PACKET MODE OUTPUT
PACKET TONE LOGIC
SYSTEM

The CMX631A is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector that indicates the presence of both 12kHz or 16kHz telephone call-charge frequencies on a telephone line.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier. The 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The CMX631A demonstrates exceptional 12kHz and 16kHz performance in the presence of both voice and noise. This device may operate from a single or differential analog signal input, from which two individual logic outputs will be produced; a Tone Follower Output or a Packet Mode Output.

This system (12kHz/16kHz) selectable integrated circuit, requires a 2.7V to 5.5V power supply, which may be line-powered, is available in the following packages: 24-pin SSOP (CMX631AD5), 16-pin SOIC (CMX631AD4), and 16-pin PDIP (CMX631AP3). Additional package styles may be available to meet specific design requirements.

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

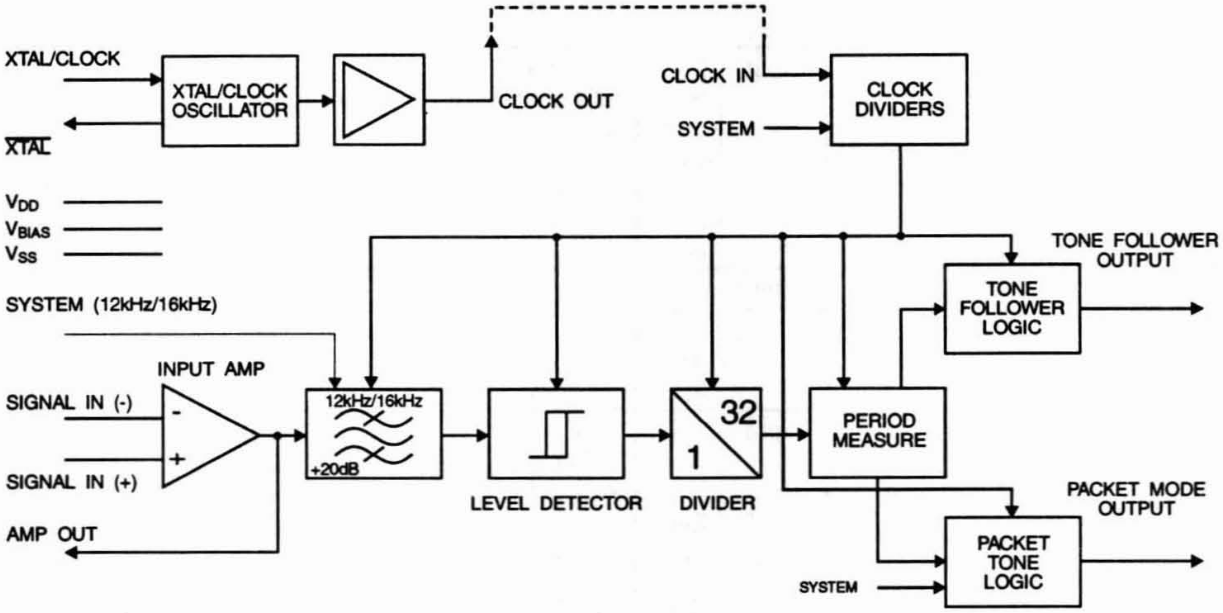

XTAL/CLOCK
XTAL/CLOCK OSCILLATOR
$\overline{XTAL}$
CLOCK OUT
CLOCK IN
SYSTEM
CLOCK DIVIDERS
V_{DD}
V_{BIAS}
V_{SS}
SYSTEM (12kHz/16kHz)
TONE FOLLOWER OUTPUT
TONE FOLLOWER LOGIC
INPUT AMP
SIGNAL IN (-)
SIGNAL IN (+)
12kHz/16kHz
+20dB
32
1
PERIOD MEASURE
LEVEL DETECTOR
DIVIDER
AMP OUT
PACKET MODE OUTPUT
PACKET TONE LOGIC
SYSTEM

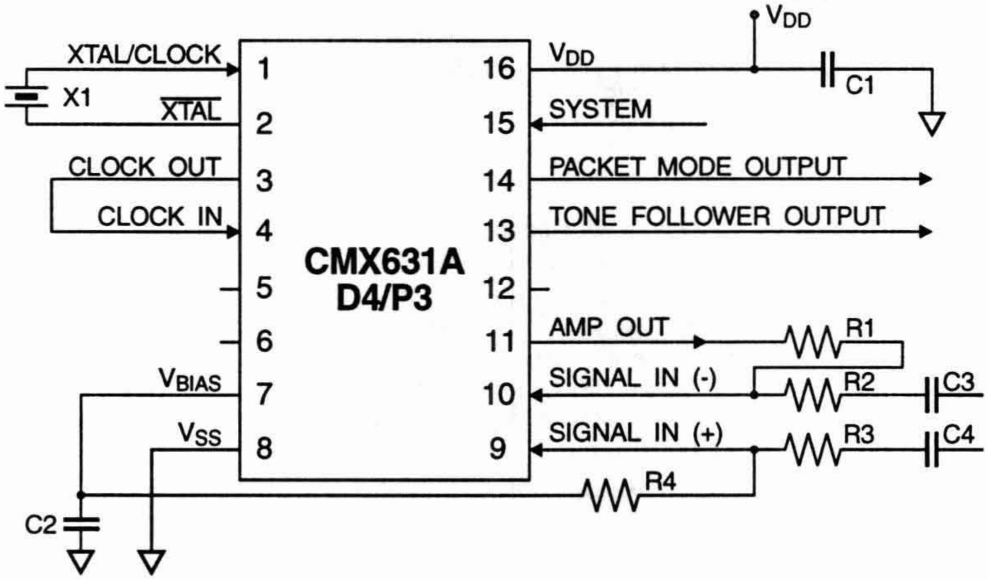
Figure 1: Block Diagram

2 Signal List

Packages		Signal		Description
D5	D4/P3	Name	Type	
1	1	Xtal/Clock	input	The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is used at the Clock In pin, this (Xtal/Clock) pin must be connected directly to V_{DD} See Figure 2 and Section 3.
4	2	$\overline{XTAL}$	output	The output of the on-chip clock oscillator inverter.
5	3	Clock Out	output	The buffered output of the on-chip-clock oscillator inverter. If a Xtal input is used, this output should be connected directly to the Clock In pin.
6	4	Clock In	input	The 3.579545MHz clock pulse input to the internal clock dividers. If an externally generated clock pulse is used, the Xtal/Clock input pin should be connected to V_{DD}. Reference Section 3.
8	7	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be bypassed to V_{SS}. See Figure 2.
12	8	V_{SS}	power	Negative supply (GND).
13	9	Signal In +	input	The positive input to the input gain adjusting signal amplifier. Reference Section 4.3 and 4.4.
17	10	Signal In -	input	The negative input to the input gain adjusting signal amplifier. Reference Section 4.3 and 4.4.
18	11	Amp Out	input	The output of the input gain adjusting signal amplifier. Reference Section 4.3 and 4.4.
19	13	Tone Follower Mode	output	This output provides a logic 0 for the period of a detected tone and a logic 1 for a NOTONE detection. See Section 4.1 and Figure 3.
20	14	Packet Mode	output	This output provides a logic 0 for a detected tone and a logic 1 for NOTONE detection and will ignore a small fluctuation or fade during the tone signal. See Section 4.2 and Figure 3.
21	15	System	input	This logic input selects the device operation to either 12kHz (logic 1) or 16kHz (logic 0) SPM systems. This input has an internal 1MΩ pull-up resistor (12kHz).
24	16	V_{DD}	power	Positive supply. A single, stable power supply is required. Critical levels and voltages within the CMX631A are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the pin. Note: If this device is line powered, the resulting power supply must be stable. See Section 5.1.1.
2, 3, 7, 9, 10, 11, 14, 15, 16, 22, 23	5,6,12	N/C		No internal connection; leave open circuit.

Table 1: Signal List

3 External Components



VDD
XTAL/CLOCK
X1
XTAL
CLOCK OUT
CLOCK IN
VBIAS
VSS
C2
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CMX631A
D4/P3
VDD
C1
SYSTEM
PACKET MODE OUTPUT
TONE FOLLOWER OUTPUT
AMP OUT
R1
SIGNAL IN (-)
R2
C3
SIGNAL IN (+)
R3
C4
R4

Figure 2: Recommended External Components

R1	Note 1	$R_{FEEDBACK}$	
R2	Note 1	$R_{IN(-)}$	
R3	Note 1	$R_{IN(+)}$	
R4	Note 1	R_{BIAS}	

C1		1.0µF	±20%
C2		1.0µF	±20%
C3		$C_{IN(-)}$	
C4		$C_{IN(+)}$	
X1	Note 2, 3, 4	3.579545MHz	

Table 2: Recommended External Components

Recommended External Component Notes:

1. When calculating input gain components, for correct operation R1 and R4 should always be ≥ 33kΩ.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The on-chip crystal circuitry includes a feedback resistor (nominally 2MΩ) between pins 1 and 2 and load capacitors on pins 1 and 2 (nominally 10pF each, excluding package and board parasitics).
4. When using an external clock input, X1 should be removed, Pin 1 (Xtal/Clock) should be tied to V_{DD}, the Clock In and Clock Out jumper should be removed, and the external clock signal applied to Clock In.

4 General Description

4.1 Tone Follower Mode

The Tone Follower Output Mode will respond and/or de-respond when a signal is detected or a NOTONE, by providing a Logic level output. When a signal has been detected, a Logic 0 is provided at the output for the duration of the valid signal. When a NOTONE or invalid decode is detected a Logic 1 is provided at the output until a valid signal is available. See Figure 3.

4.2 Packet Mode

The Packet (Cumulative Tone) Mode Output will respond and/or de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period by providing a Logic level output. See Figure 3.

This process does ignore the small fluctuations or fades of a valid frequency input. During a 40ms toneburst, no tone interruption (small fluctuation or fade) is allowed during this period for the signal to be considered valid. If a 45ms toneburst occurs, then a 2ms interruption is allowed, and the signal is still considered valid. For NOTONE, there must be 40ms of continuous no tone or for a 45ms period, there may be 2ms of tone and the NOTONE still be valid. For a valid detect of tone the output provides a Logic 0. For the valid detect of NOTONE, the output provides a Logic 1.

This output is available for µProcessor 'Wake-Up', Minimum Tone detection, NOTONE indication, or transient avoidance.

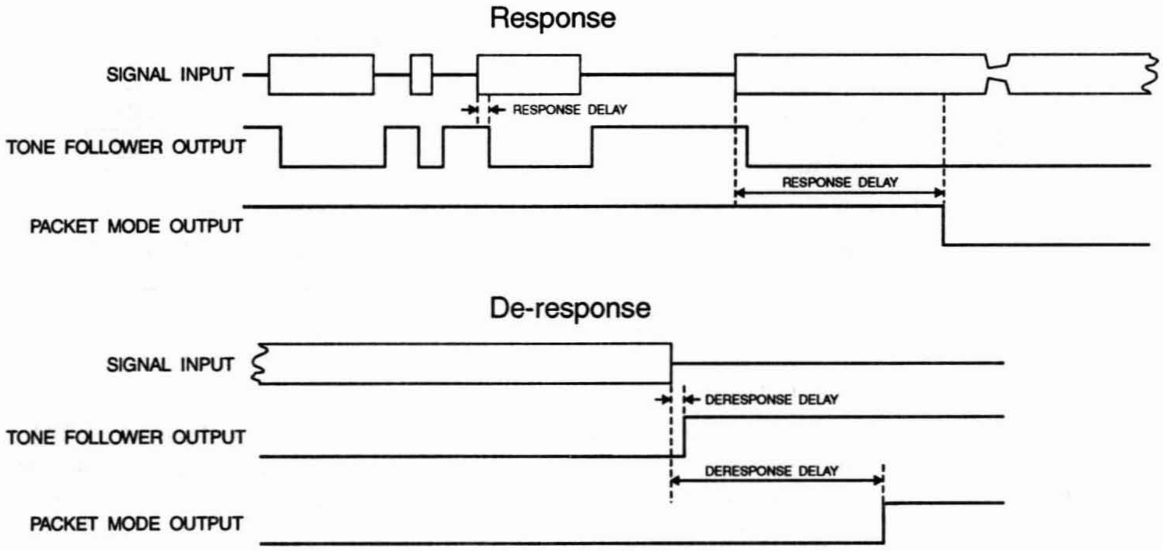


Figure 3: Tone Follower and Packet Mode Outputs

4.3 Sensitivity Setting

The CMX631A input sensitivity can be accurately adjusted and set to support many national 12kHz and 16kHz SPM specifications.

4.3.1 Input Gain Calculation

The input amplifier, with external circuitry, is used to set the sensitivity of the CMX631A to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graphs in Figure 4 and Figure 5, the following steps will assist in the determination of the required gain/attenuation.

1. Draw two horizontal lines from the Y-axis [Signal Level (dB)] in Figure 4 and Figure 5. The upper line represents the required 'Must' decode level. The lower line represents the required 'Must-Not' decode level

2. Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis [Amplifier Gain (dB)]. The point where the vertical line meets the X-axis indicates the minimum Input Amp gain required for reliable decoding of valid signals.
3. Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis. The point where the vertical line meets the X-axis will indicate the maximum allowable Input Amp gain. Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

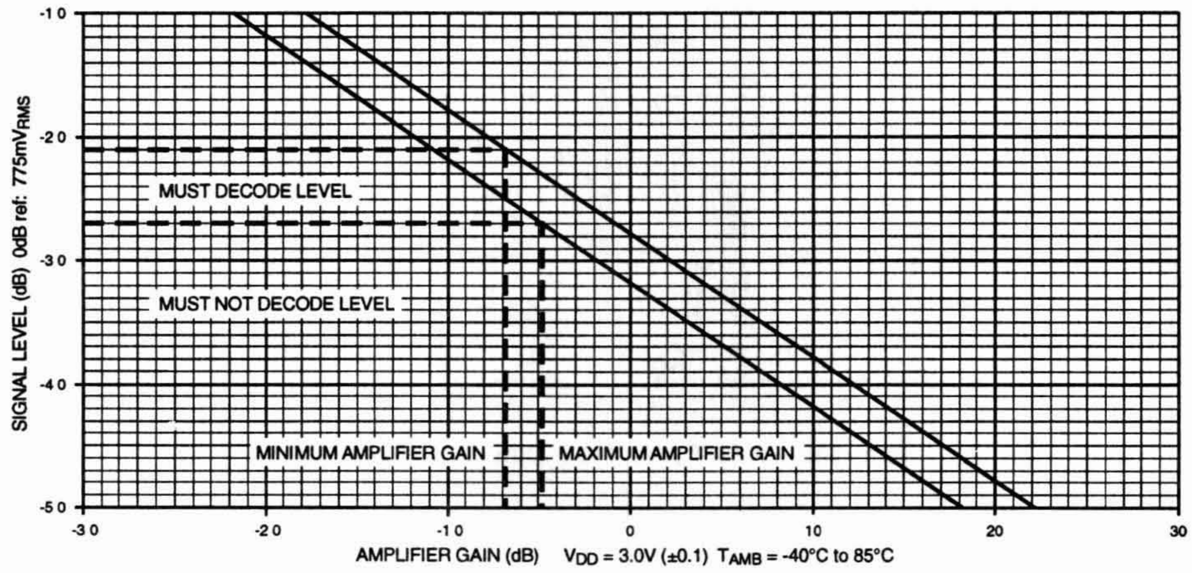


Figure 4: Input Gain Calculation Graph for V_{DD} = 3.0V

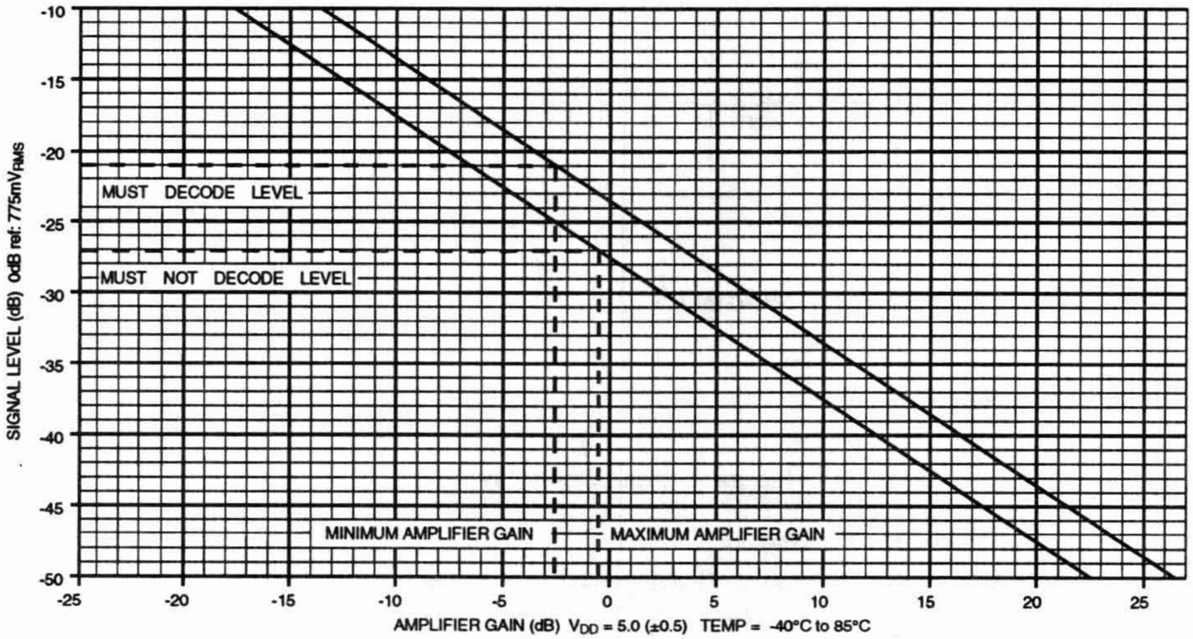


Figure 5: Input Gain Calculation Graph for V_{DD} = 5.0V

4.3.2 Input Gain Components

Reference the gain components found in Table 2 and Figure 2. The user should calculate and select external components (R1/R3/C3 and R2/R4/C4) to provide amplifier gain within the limits obtained in Section 4.3.1.

Component tolerances should not move the gain-figure outside these limits. The graphs in Figure 4 and Figure 5 are for the calculation of input gain components for a CMX631A using a V_{DD} of 3.0 (±0.1) or V_{DD} of 5.0 (±0.5).

4.4 'WILL'/'WILL-NOT' Detect Frequencies

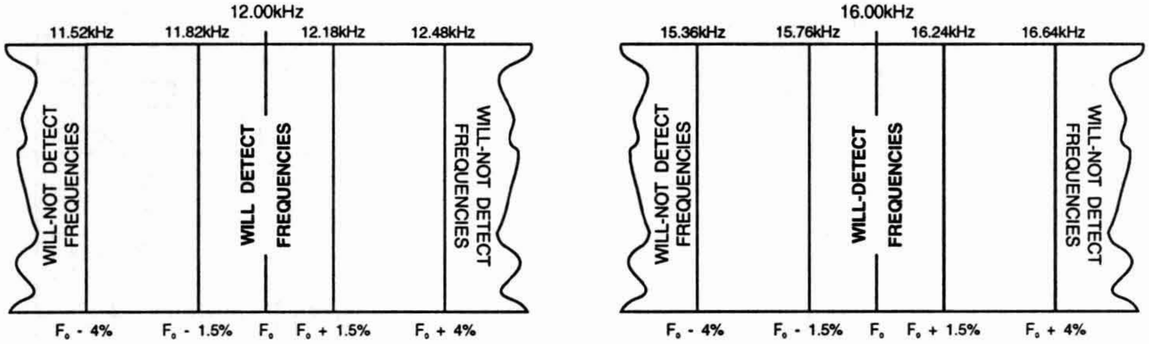

12.00kHz
11.52kHz
11.82kHz
12.18kHz
12.48kHz
WILL-NOT DETECT FREQUENCIES
WILL DETECT FREQUENCIES
WILL-NOT DETECT FREQUENCIES
F₀ - 4%
F₀ - 1.5%
F₀
F₀ + 1.5%
F₀ + 4%
16.00kHz
15.36kHz
15.76kHz
16.24kHz
16.64kHz
WILL-NOT DETECT FREQUENCIES
WILL-DETECT FREQUENCIES
WILL-NOT DETECT FREQUENCIES
F₀ - 4%
F₀ - 1.5%
F₀
F₀ + 1.5%
F₀ + 4%

Figure 6: 'WILL'/'WILL-NOT' Detect Frequencies

5 Applications

5.1 Input Configurations

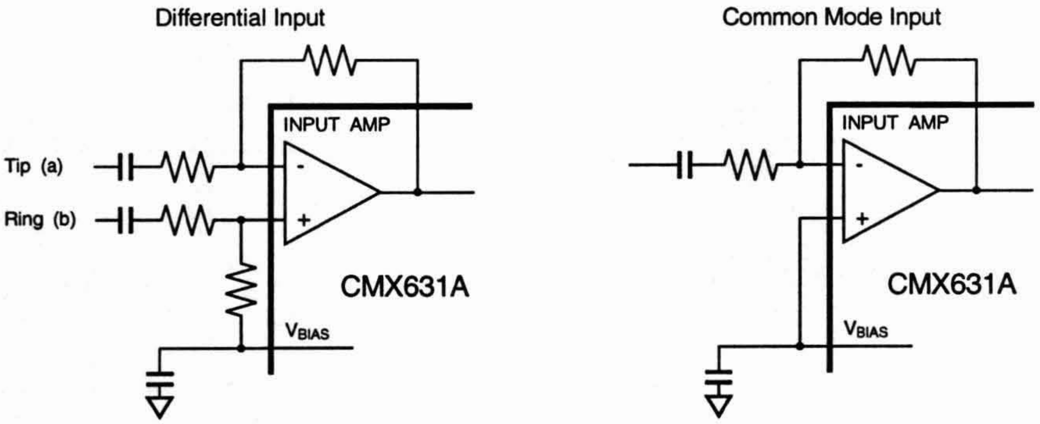

Differential Input
Tip (a)
Ring (b)
INPUT AMP
-
+
CMX631A
VBIAS
Common Mode Input
INPUT AMP
-
+
CMX631A
VBIAS

Figure 7: Input Configurations

5.1.1 Protection Against High Voltages

Telephone systems may have high DC and AC voltages present on the line. If the CMX631A is a part of host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the CMX631A will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the DC voltages plus all expected signal peaks.

5.1.2 Aliasing

Due to the sampling nature of switched-capacitor filters used in the CMX631A, high frequency noise or unwanted signals can alias into the passband, disrupting detection. External components must be chosen carefully to avoid alias effects.

Possible Alias Frequencies:

12kHz Mode = 52kHz
16kHz Mode = 69kHz

If other filtering in the system has not attenuated these alias frequencies, capacitors should be employed across resistors R1 and R4 to provide anti-alias filtering.

The low-pass cutoff frequency should be chosen to be approximately 20kHz to 25kHz for a 12kHz system, or 25kHz to 30kHz for a 16kHz system.

$$\text{i.e.}\quad C = \frac{1}{2\times\ \ \times f_0 \times (R1\ \text{or}\ R4)}$$

When anti-alias capacitors are used, an allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

6 Performance Specification

6.1 Electrical Specifications

6.1.1 Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}-V_{SS})	-0.3		7.0	V
Voltage on any pin to V_{SS}	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
D4 / P3 Packages				
Total allowable device dissipation at T_{AMB} 25°C			800	mW
Derating above T_{AMB} 25°C			13	mW/°C above T_{AMB} 25°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C
D5 Package				
Total allowable device dissipation at T_{AMB} 25°C			550	mW
Derating above T_{AMB} 25°C			9	mW/°C above T_{AMB} 25°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})	2.7	3.0/5.0	5.5	V
Operating Temperature	-40		85	
Xtal/Clock Frequency	3.558918		3.589368	MHz

6.1.3 Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.0V to 5.0V @ T_{AMB} = -40°C to 85°C
Audio Level 0dB (ref.) = 775mV_{RMS}, Noise Bandwidth = 50kHz
Xtal/Clock Frequency = 3.579545MHz, System Setting = 12kHz or 16kHz

	Notes	Min.	Typ.	Max.	Units
Supply Current					
V_{DD} = 3.0V				0.8	mA
V_{DD} = 5.0V				2.2	mA
Logic Inputs/Outputs					
Input Logic '1'		70			%V_{DD}
Input Logic '0'				30	%V_{DD}
Output Logic '1'		90			%V_{DD}
Output Logic '0'				10	%V_{DD}
Xtal/Clock or Clock In Frequency		3.558918		3.589368	MHz
External Clock Pulse Width					
High		100			ns
Low		100			ns
Input Amplifier					
D. C. Gain		60.0			dB
Bandwidth (-3dB)			100		Hz
Input Impedance			1.0		MΩ
Logic Impedances					
Input					
System		0.7		3.8	MΩ
Clock In		10.0			MΩ
Output			14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	1	11.820		12.180	kHz
12kHz Not-detect Frequencies (below 12kHz)	1			11.520	kHz
12kHz Not-detect Frequencies (above 12kHz)	1	12.480			kHz
16kHz Detect Bandwidth	1	15.760		16.240	kHz
16kHz Not-detect Frequencies (below 16kHz)	1			15.360	kHz
16kHz Not-detect Frequencies (above 16kHz)	1	16.640			kHz
Sensitivity					
V_{DD} = 3.0V±0.1V	2	-27.8		-31.8	dBm
V_{DD} = 5.0V±0.5V	2	-23.5		-27.5	dBm

Tone Operating Characteristics					
Signal-to-Noise Requirements (Amp Input)	3, 4, 5, 6	22.0	20.0		dB
Signal-to-Voice Requirements (Amp Input)	3, 4, 5, 7	-36.0	-40.0		dB
Signal-to-Voice Requirements (Amp Output)	5, 6	-25.0		-29.0	dB
Tone Follower Mode	1, 8				
Response and De-Response Time				10.0	ms
Packet Mode	1, 8				
Response and De-Response Time		40.0		48.0	ms

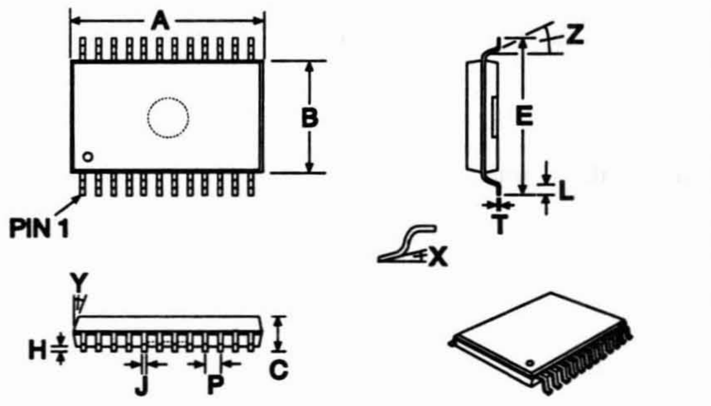
Table 3: Operating Characteristics

Operating Characteristics Notes:

1. With adherence to Signal-to-Voice and Signal-to-Noise specifications.
2. With Input Amplifier gain set to unity gain. Reference Section 4.3 for description of sensitivity setting.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses.
6. With SPM and voice signal amplitudes balanced. To avoid false de-responses due to saturation, the peak to peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz.
8. Response, De-Response, and Power-up Response timing.

6.2 Packages

The CMX631A is available in the following packages. Additional package styles may be available to meet specific design requirements.

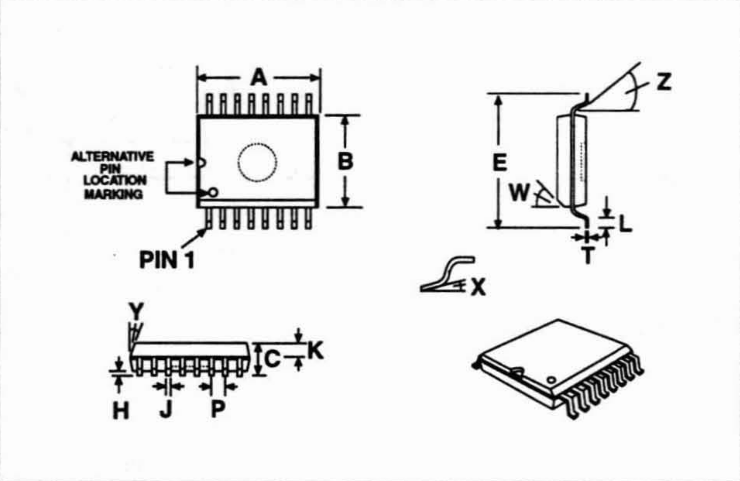


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin SSOP Mechanical Outline: ***order as part no. CMX631AD5***

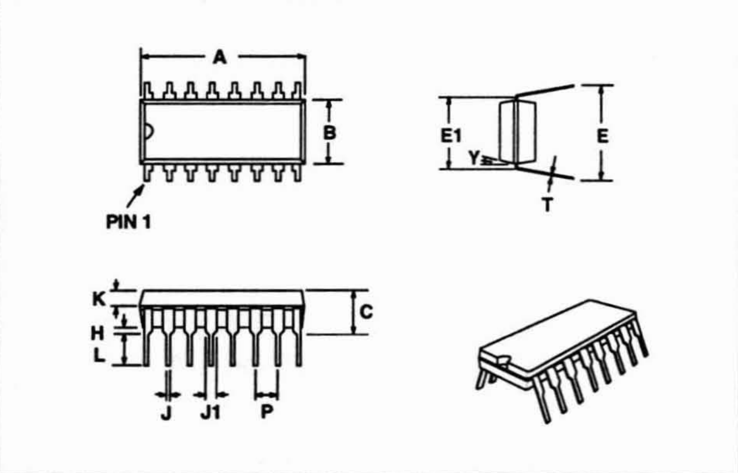


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin SOIC Mechanical Outline: ***order as part no. CMX631AD4***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin PDIP Mechanical Outline: ***order as part no. CMX631AP3***

MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

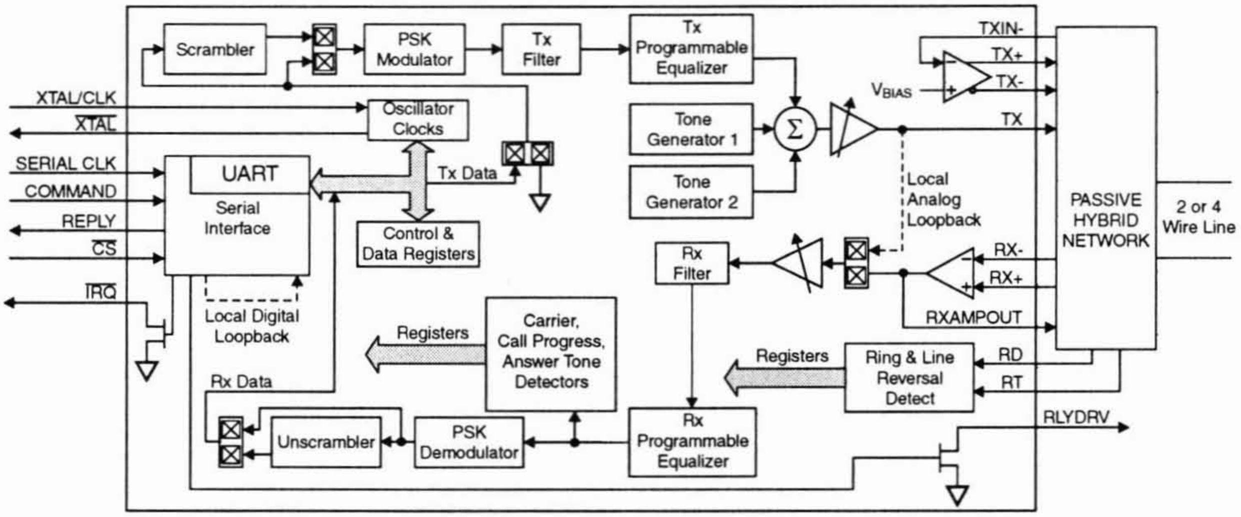
CMX644A Bell 212A and V.22 Modem with Call Progress and DTMF

Features

- **Bell 212A and V.22 Compatible Modem**
- **1200bps Full Duplex Operation (2 or 4 Wire)**
- **UART for Start/Parity/Stop bit processing**
- **Direct Drive (Non-UART) Operating Mode**
- **Software Adjustable Tx and Rx Levels**
- **Programmable Group Delay Equalizer**
- **Answer/Originate Tone Generator/Detector**
- **Call Progress Tone Detection**
- **Integrated DTMF Encoder**
- **Line Reversal and Ring Detector**
- **Hook Switch Relay Driver**
- **Flexible Xtal/Master Clock Selection**
- **Simple Serial Control Interface**
- **Zero-Power Standby Mode**
- **3.0 to 5.0V Operation**

Applications

- **Telephone Telemetry Systems**
- **Remote Utility Meter Reading**
- **Security Systems**
- **Payphones**
- **Cable-TV Set Top Boxes**
- **Industrial Control Systems**
- **Electronic Cash Terminals**
- **Vending Machines**


Scrambler
PSK Modulator
Tx Filter
Tx Programmable Equalizer
TXIN-
TX+
TX-
VBIAS
TX
XTAL/CLK
XTAL
Oscillator Clocks
Tone Generator 1
Σ
Tone Generator 2
SERIAL CLK
COMMAND
REPLY
CS
IRQ
UART
Serial Interface
Tx Data
Control & Data Registers
Local Analog Loopback
PASSIVE HYBRID NETWORK
2 or 4 Wire Line
Rx Filter
RX-
RX+
RXAMPOUT
Local Digital Loopback
Registers
Carrier, Call Progress, Answer Tone Detectors
Registers
Ring & Line Reversal Detect
RD
RT
Rx Data
Unscrambler
PSK Demodulator
Rx Programmable Equalizer
RLYDRV

The CMX644A Bell 212A/V.22 modem provides full duplex 1200bps data signaling suitable for telephone based information and telemetry systems where low power operation is desired. Bell 212A/V.22 signaling delivers fast-call set-up times and robust, error resistant, transmission in 2 or 4 wire line circuits. A rich set of important additional functions enhances end product value while reducing size. These include: integrated DTMF encoder for dial out functions, single tone encoder for 'melody' generation, answer tone generator/detector, line reversal and ring detector for 'waking' up a sleeping µC, adjustable Tx and Rx gain, and a low impedance pull down output for hook relay control. The addition of the answer tone generator/detector and call progress tone detector makes the set-up of a telephone call much easier for the host µC to accomplish.

Very low power telemetry and data collection applications are supported by the CMX644A's 'Zero Power' standby mode in which the device will detect telephone line ringing voltage or line voltage reversal events.

The CMX644A is pin compatible with the CMX624 Bell 202 / V.23 modem and operates with a supply voltage between 3.0V and 5.5V, and is available in the following packages: 24-pin SSOP (CMX644AD5), 24-pin SOIC (CMX644AD2), and 24-pin PDIP (CMX644AP4).

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX654

V.23 TRANSMIT MODULATOR

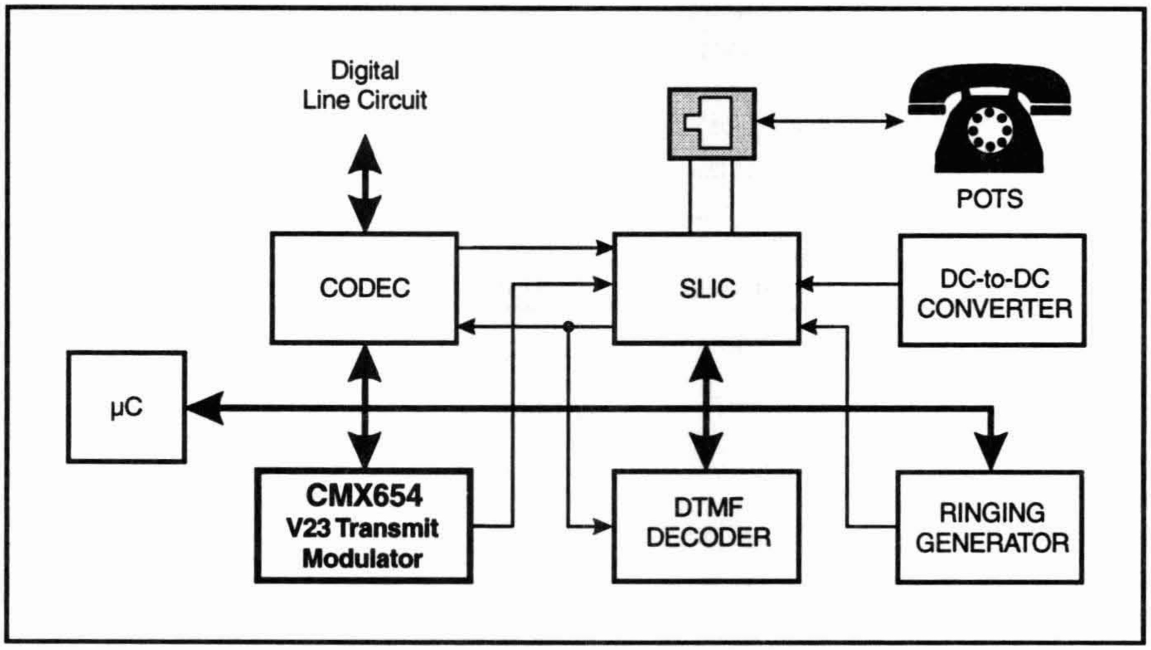
PRELIMINARY INFORMATION

Features

- **1200bits/sec, V.23 Transmit Modulator**
- **3.0V to 5.5V Supply:**
  1mA typical at 3V
- **Zero Power Mode:**
  1µA typical
- **1200bits/sec Tx Data Retiming**
- **3.58MHz Xtal/Clock Rate**
- **Meets ITU and ETSI Specifications**

Applications

- **Caller ID generation for:**
  ISDN Terminal Adapters
  Wireless Local Loop System
  ISDN PABX Applications
  Pair-Gain Systems
  Public Switched Telephone Networks
  Trunk Exchanges



The CMX654 is a low power integrated circuit, designed for the transmission of asynchronous 1200bits/sec data in accordance with ITU, V.23 and ETSI specifications.

The device incorporates an optional Tx data retiming function. This device may be operated so that only the mark or space tone is produced.

The CMX654 may be used in a wide range of telephone telemetry systems. With a low voltage requirement of 3.0V it is suitable for both portable terminal and line powered applications. A very low current 'sleep' mode (1µA typ.) and an operating current of 1mA typ. makes the CMX654 ideal for line powered applications.

This device requires a standard 3.58MHz Xtal/Clock rate and operates from a 3.0 to 5.5V supply. Available packages are: 16-pin SOIC (CMX654D4) and 16-pin PDIP (CMX654P3). Additional package styles may be available to meet specific design requirements.

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1 Block Diagram

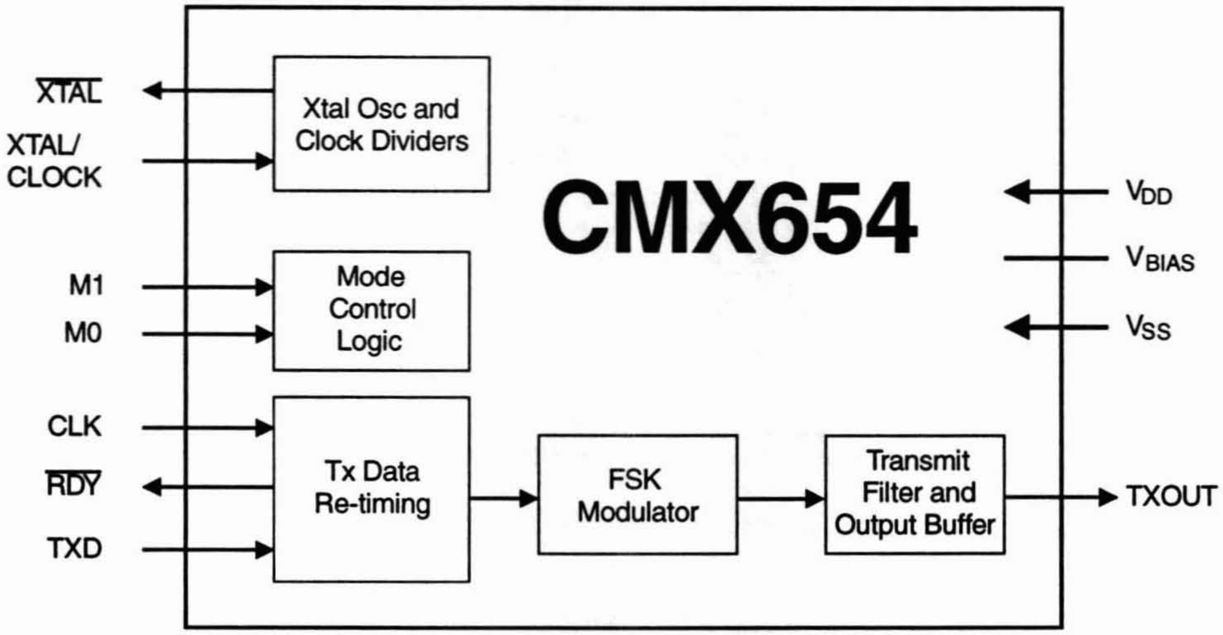

$\overline{\text{XTAL}}$
XTAL/
CLOCK
Xtal Osc and
Clock Dividers
CMX654
V_{DD}
V_{BIAS}
V_{SS}
M1
M0
Mode
Control
Logic
CLK
$\overline{\text{RDY}}$
TXD
Tx Data
Re-timing
FSK
Modulator
Transmit
Filter and
Output Buffer
TXOUT

Figure 1: Block Diagram

2 Signal List

D4/P3	Signal		Description
Pin No.	Name	Type	
1	$\overline{\text{XTAL}}$	input	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	input	The input to the on-chip Xtal oscillator inverter.
3	M0	input	A logic level input for setting the mode of the device. See Section 4.2.
4	M1	input	A logic level input for setting the mode of the device. See Section 4.2.
5			Connect to V_{SS}.
6		N/C	No connection, do not connect to this pin.
7	TXOUT	output	The output of the FSK generator.
8	V_{SS}	Power	The negative supply rail (ground).
9	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	-	-	Connect to V_{DD}.
11	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See Section 4.3.
12	CLK	input	A logic level input which may be used to clock data bits into the Tx FSK Data Retiming block.
13	-	N/C	No connection, do not connect to this pin.
14	-	N/C	No connection, do not connect to this pin.
15	$\overline{\text{RDY}}$	output	"Ready for Tx data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

V_{DD} and V_{BIAS} decoupling is very important. It is recommended that the decoupling capacitors be placed so that connections between them and the device pins are as short as practicable.

Table 1: Signal List

3 External Components

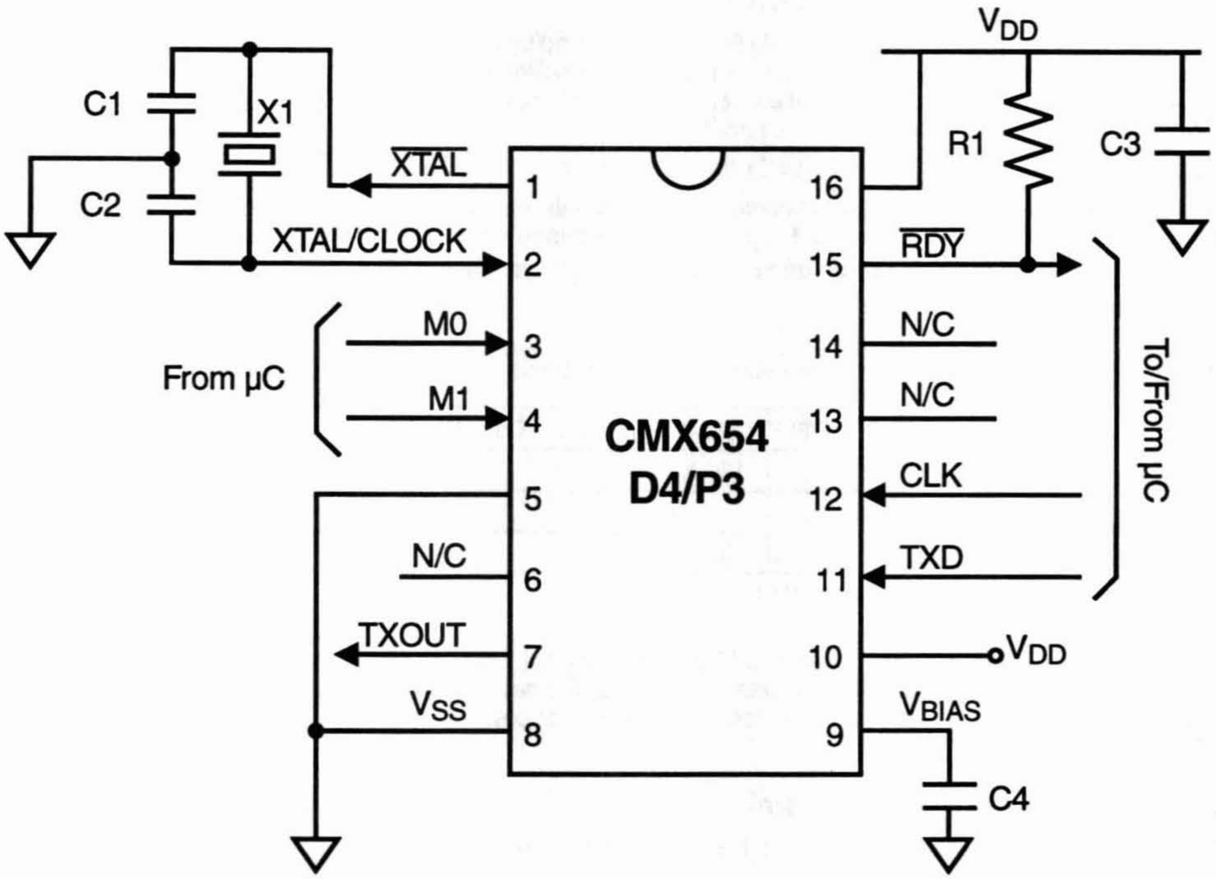

VDD
C1
X1
C2
XTAL
XTAL/CLOCK
1
2
16
15
R1
C3
RDY
From µC
M0
M1
3
4
14
13
N/C
N/C
CMX654
D4/P3
To/From µC
5
12
CLK
N/C
6
11
TXD
TXOUT
7
10
VDD
VSS
8
9
VBIAS
C4

Figure 2: External Components

R1		100kΩ
C1, C2		18pF
C3		0.1µF
C4		0.1µF
X1	Note 1	3.579545MHz

Resistors ±5%, capacitors ±10% unless otherwise stated

Table 2: External Components for Typical Application

External Components Notes:

1. A crystal frequency of 3.579545MHz±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4 General Description

4.1 Xtal Oscillator and Clock Dividers

Frequency and timing accuracy of the CMX654 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source, which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by CMX654 as well as generating undefined states of the $\overline{\text{RDY}}$ output.

4.2 Mode Control Logic

The CMX654's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Tx Mode	Data Retime[1]
0	1	1200bits/sec	Tx
1	0	off	-
1	1	'Zero-Power'	-

[1] If enabled

In the 'Zero-Power' mode, power is removed from all internal circuitry. When leaving 'Zero-Power' mode there must be a delay of 20ms before any Tx data is passed to the device to allow the bias level, filters and oscillator to stabilize. On applying power to the device the mode must be set to 'ZP', i.e. M0=1, M1=1, until V_{DD} has stabilized.

4.3 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = '0'	TXD = '1'
1	1	'Zero Power'	'Zero Power'
1	0	0Hz	0Hz[1]
0	1	2100Hz	1300Hz

[1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see Section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 3 assuming that the signal on the line is at -6dBm or less.

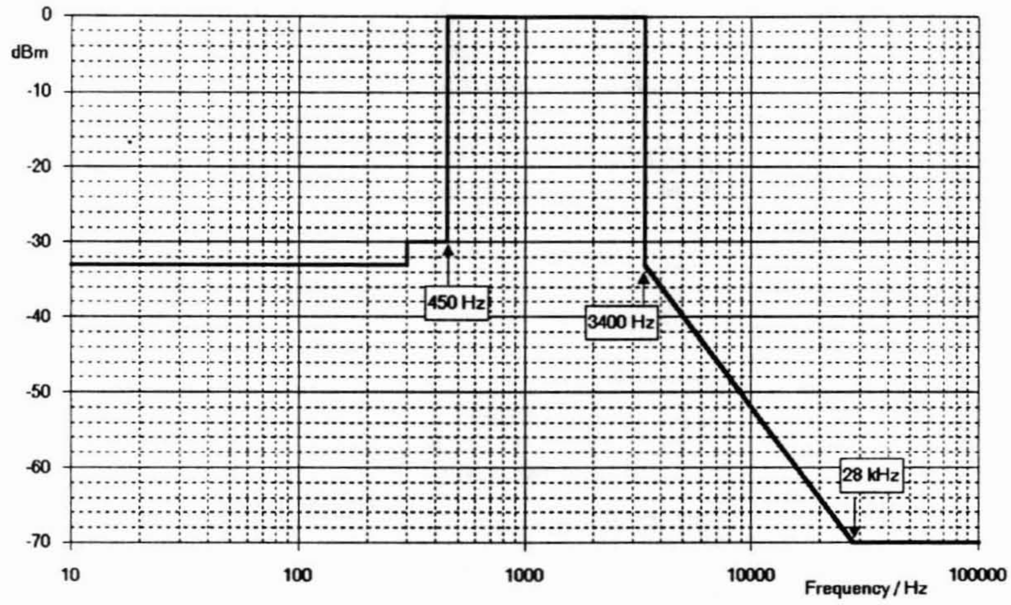


Figure 3: Tx Limits

4.4 Tx Data Retiming

The Data Retiming block, when enabled in 1200bits/sec transmit mode, requires the controlling µC to load 1 bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{\text{RDY}}$ pin is pulled low. The $\overline{\text{RDY}}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the $\overline{\text{RDY}}$ output is pulled low. When the $\overline{\text{RDY}}$ pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 7.

To ensure synchronization between the controlling device and the CMX654 when entering Tx retiming mode, the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, the CLK input to the CMX654 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 4.

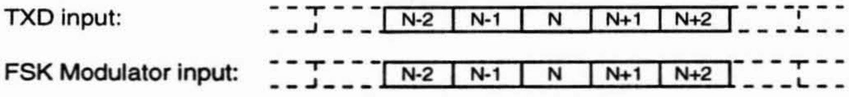


Figure 4: FSK Operation without Tx Data Retiming (CLK always high)

5 Application Notes

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the CMX654. A Line Interface circuit is necessary to:

- Provide high voltage and DC isolation
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals

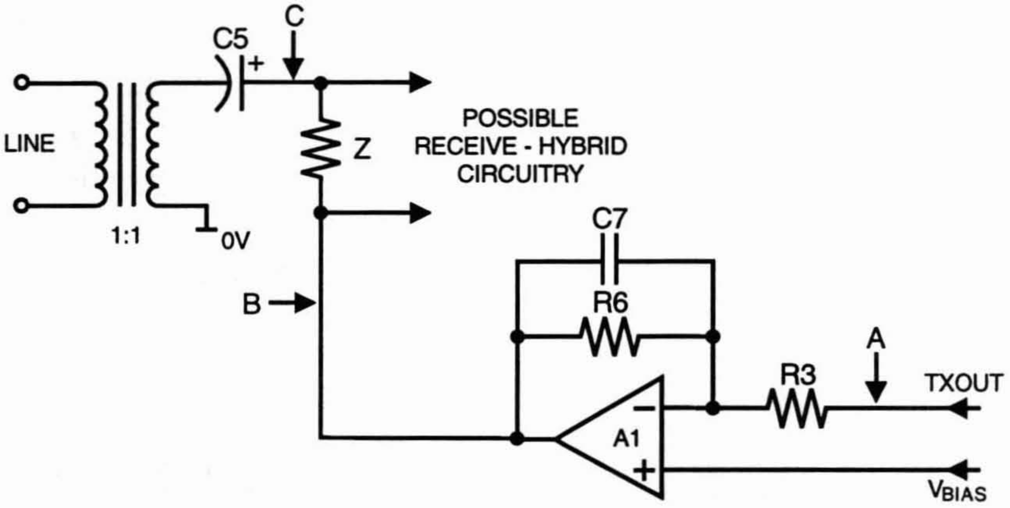


Figure 5: Line Interface Circuit

R3	Note 3	C5	22µF (±20%)
R6	100kΩ	C7	330pF

Resistors ±1%, capacitors ±10% unless otherwise stated.

Notes:

1. The component(s) 'Z' between points B and C should match the line impedance.
2. Device A1 must be able to drive 'Z' and the line.
3. R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

'A' = 20Log(V_{DD}/5)
'B' = 'A' + 20Log(100kΩ/R3)
'C' = 'B' - 6

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of:			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
D4 / P3 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Notes:

1. A Xtal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.0V at T_{AMB} = 25°C and V_{DD} = 3.3V to 5.5V at T_{AMB} = -40 to +85°C,

Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS} ,

0dBm corresponds to 775mV_{RMS} into 600Ω.

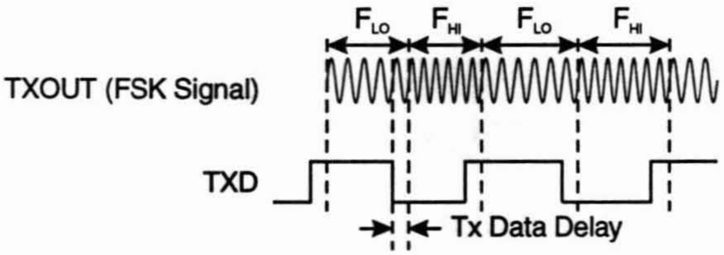
	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0='1', M1='1')	1, 2		1		µA
I_{DD} (M0 or M1='0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1='0') at V_{DD}= 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD}-0.4			V
Output Logic '0' Level (I_{OL} = -360µA)				0.4	V
$\overline{RDY}$ Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Retiming					
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level	3	-1.0	0	1.0	dB
Twist (Mark Level WRT Space Level)		-2.0	0	2.0	dB
Tx 1200bits/sec (M1='0', M0='1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1297		1303	Hz
Space (Logical 0) Frequency		2097		2103	Hz
XTAL/CLOCK Input					
'High' Pulse Width	4	100			ns
'Low' Pulse Width	4	100			ns

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the CMX654 pins by external circuitry other than X1, C1 and C2.
2. TXD and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Relative to 775mV_{RMS} at V_{DD}= 5.0V for load resistance greater than 40kΩ.
4. Timing for an external input to the XTAL/CLOCK pin.

6.2 Timing

Data and Mode Timing	**Min.**	**Typ.**	**Max.**	**Units**
Delay to reliable data at TXOUT after ZP to Tx mode change			20.0	ms
Data Retiming Disabled (reference Figure 6)				
Tx Data Delay (TXD to TXOUT)		0.1		ms
Data Retiming Enabled (reference Figure 7)				
t_D = Internal CMX654 delay			1	µs
tc_{HI} = CLK High time	1			µs
t_R = RDY low to CLK going low			800	µs
t_S = Data Set-up time	1			µs
t_H = Data Hold time	1			µs


F_{LO}
F_{HI}
F_{LO}
F_{HI}
TXOUT (FSK Signal)
TXD
Tx Data Delay

Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 6: TXD to TXOUT Delay time

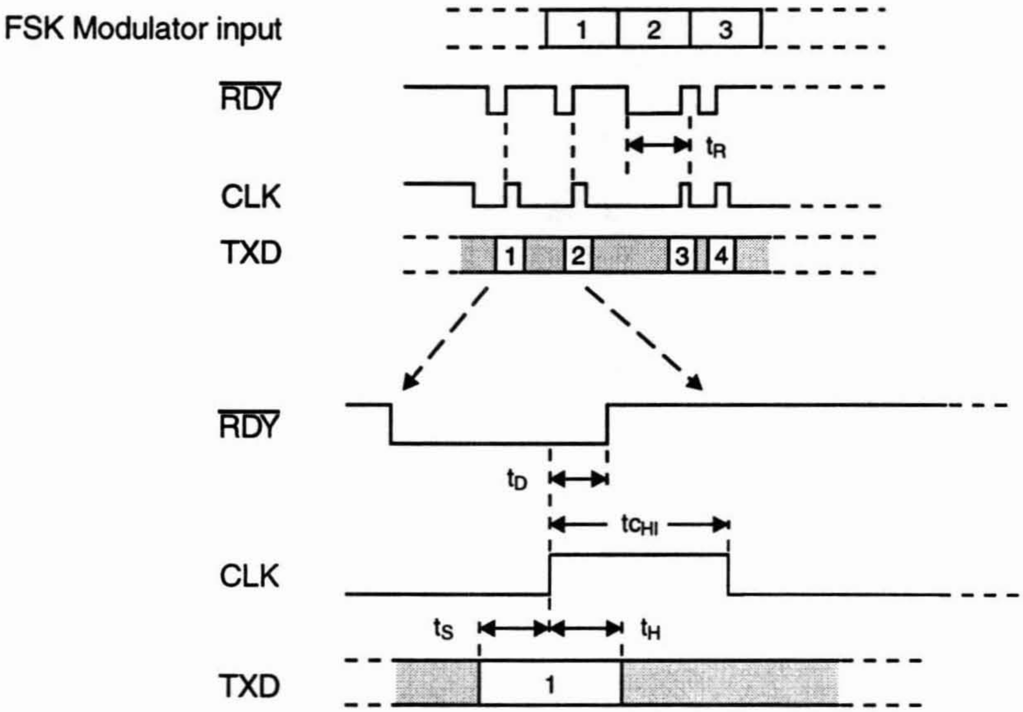
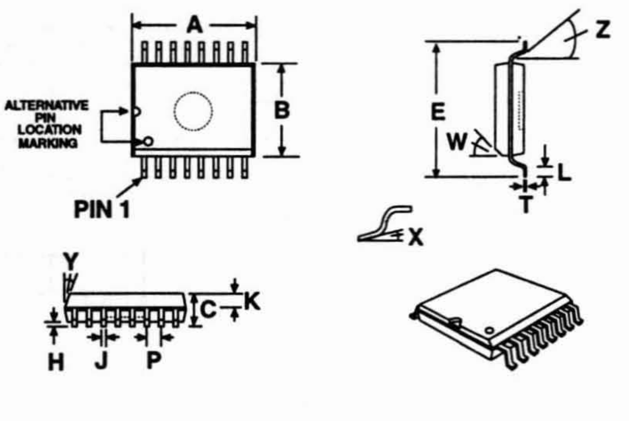

FSK Modulator input
1
2
3
$\overline{RDY}$
t_R
CLK
TXD
1
2
3
4
$\overline{RDY}$
t_D
tc_{HI}
CLK
t_S
t_H
TXD
1

Figure 7: FSK Operation with Tx Data Retiming

6.3 Packaging

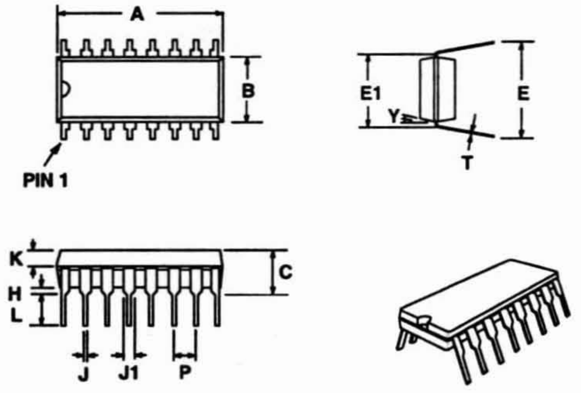


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 16-pin SOIC (D4) Mechanical Outline: ***Order as part no. CMX654D4***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin PDIP (P3) Mechanical Outline: ***Order as part no. CMX654P3***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX673 Call Progress Tone Detector

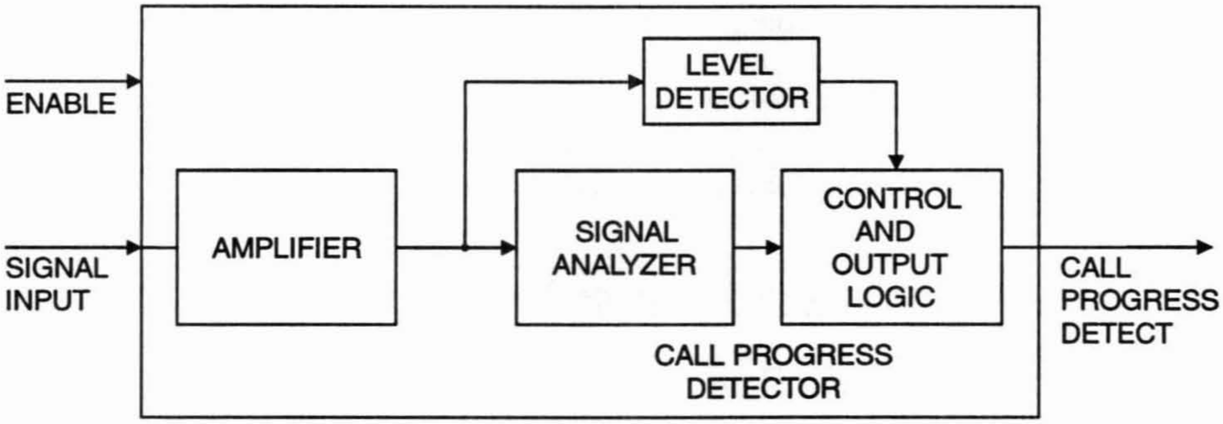
ADVANCE INFORMATION – Shipping September 98

Features

- **Worldwide Tone Compatibility**
- **Fast Response**
  - **Stutter Dial Tone**
  - **Single and Dual Tones**
- **Industry Compatible Pin Out**
- **Wide Dynamic Signal Range**
- **Low Power: 0.5mA at 3.0V**
- **3.0V to 5.0V Operation**
- **3.58MHz Xtal/Clock Oscillator**

Applications

- **Worldwide Payphone Systems**
- **Featurephone active feature confirmation**
- **Telephone Redialing Systems**
- **Dialing Modems**
- **Banking and Billing Systems**
- **Telecom Test Equipment**
- **Telecom Security Systems**



The CMX673 is a low voltage multi-purpose Call Progress Tone detector for use in Public Switched Telephone Network System (PSTN) applications. Call progress detection allows equipment that dials into the PSTN to monitor the progress of the resulting call. Various states such as Ringing, Busy, Not available, and Answer can be determined. Using digital signal processing techniques the CMX673 accurately analyzes tones in the 315Hz to 650Hz frequency band and distinguishes valid call progress tone signals from line noise or voice. This contrasts with other call progress detection devices that are based on simple filtering techniques. When combined with cadence measurement of the CMX673 output, the rapid detect response time of the CMX673 allows it to support a wide range of call progress functions including 'stutter dial tone' detection used in voice messaging systems.

A single, low cost 3.58MHz crystal ensures accurate and repeatable performance. With supply requirements between 2.7V and 5.5V the CMX673 is easily integrated into a wide range of telecom applications.

The convenient CMX673 pin out allows it to be readily incorporated into existing product designs to quickly achieve its benefits. Small geometry CMOS design techniques provide a complete call progress detector that analyzes both frequency and amplitude in a small single package. Available packages are: 8-pin PDIP (CMX673P1) and 16-pin SOIC (CMX673D4). Additional package styles may be available to meet specific design requirements.

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1 Block Diagram

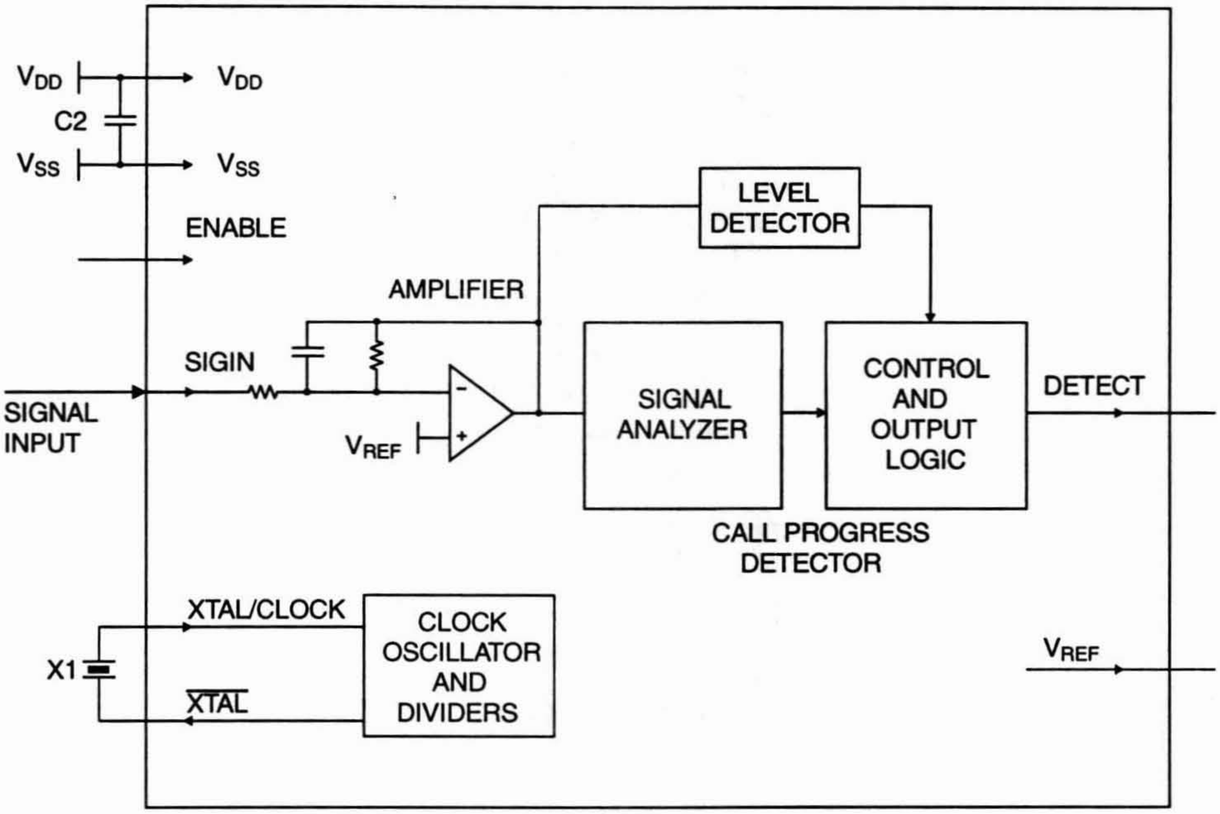

V_DD
V_DD
C2
V_SS
V_SS
ENABLE
AMPLIFIER
LEVEL DETECTOR
SIGIN
SIGNAL INPUT
V_REF
SIGNAL ANALYZER
CONTROL AND OUTPUT LOGIC
DETECT
CALL PROGRESS DETECTOR
XTAL/CLOCK
X1
XTAL
CLOCK OSCILLATOR AND DIVIDERS
V_REF

Figure 1: Block Diagram

2 Signal List

Packages		Signal		Description
D4	P1	Name	Type	
2	1	XTAL/CLOCK	input	The input to the on-chip oscillator and external clock input. Components are on chip.
4	2	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
5	3	ENABLE	input	A logic '1' applied to this input enables the DETECT output. A logic '0' will reset DETECT output to a logic '0'.
7	4	DETECT	output	When a call progress signal is detected, this output goes to a logic '1'.
10	5	SIGIN	input	Signal input. Signals to this pin should be AC coupled. The DC bias of this pin is set internally.
12	6	V_{SS}	Power	The negative supply rail (ground).
14	7	V_{REF}	output	Internally generated reference voltage, held at $V_{DD}/2$
15	8	V_{DD}	Power	The positive supply rail. This pin should be bypassed to V_{SS} by a capacitor.
1, 3 6, 8 9, 11 13, 16		NC		Internal Connection. Do not make any connection to these pins.

Table 1: Signal List

3 External Components

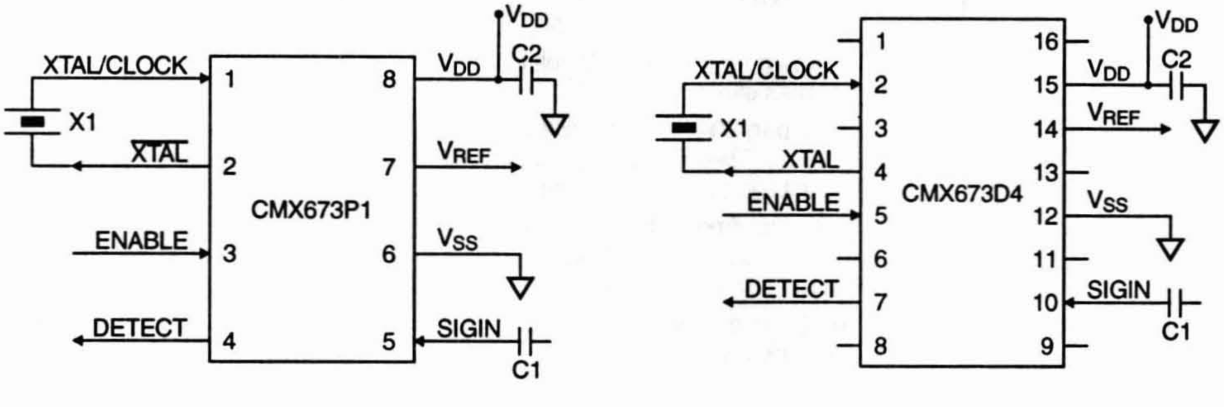


Figure 2: Recommended External Components

C1	Note 1	0.1µF	± 20%
C2		1µF	± 20%
X1	Note 2, 3	3.579545MHz	

Table 2: Recommended External Components

Note:

1. C1 is not required if the input is referenced to V_{REF}.
2. Reference Section 6.1
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4 General Description

4.1 Overall Function Description

The CMX673 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech and noise. False outputs caused by speech are a common feature with these products, and background noise may lead to a stuck "detect" output.

The CMX673, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domains, with signal amplitude forming part of the decision process. This analysis includes checks on whether the signal has a "profile" which matches international standards for Call Progress tone, or a profile more likely to match that of speech, noise or no signal.

4.2 Glossary

The following Glossary, and the Decode Truth Table in Section 4.4 provide an explanation of the decoding functions and features offered by the CMX673.

Call Progress Tones:	The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signaling.
Call Progress Band:	The nominal range 315Hz to 650Hz within which the CMX673 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.
No Signal:	No Signal is classified by the absence of an input signal, a signal below 250Hz, or a signal between 750Hz and 10kHz **Note:** Signals above 10kHz should be at a level below -38dBm to avoid aliasing.
Nominal:	Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

4.3 Block Diagram Description

Amplifier:	The input signal is amplified by a self-biased inverting amplifier. The DC bias of this input is internally set at $V_{DD}/2$.
Signal Analyzer:	The frequency range, quality and consistency of the input signal is analyzed by this functional block. To be classified as a call progress signal the input signal frequencies should lie between 315Hz and 650Hz. The signal to noise ratio must be 16dB or greater. The signal must be consistent over a period of about 80ms. These decode criteria are continuously monitored and the assessment is updated every 6ms; reference Figure 4.
Control Logic:	This block categorizes the nature of the signal into two decoded output states and controls the output pin. See the Decode Output Truth Table in Section 4.4.
Level Detector:	The level detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold. The level detector output goes to the Control and Output Logic block. The data output is gated with the level detector's output. The data output is valid only if the level detector output is true.
Xtal/Clock Oscillator:	If the on-chip Xtal oscillator is to be used, then external component X1 is required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the $\overline{\text{XTAL}}$ pin should be left unconnected.

4.4 Decode Output Truth Table

"DETECT"	CONDITIONS
0	No Signal
1	Call Progress Band: Will detect 350+440, 400+450, 440+480 400, 425,440, 450, 480+620, 600 and 620Hz tones

Note: DETECT responds to the whole range of call progress tones from 315Hz to 650Hz.

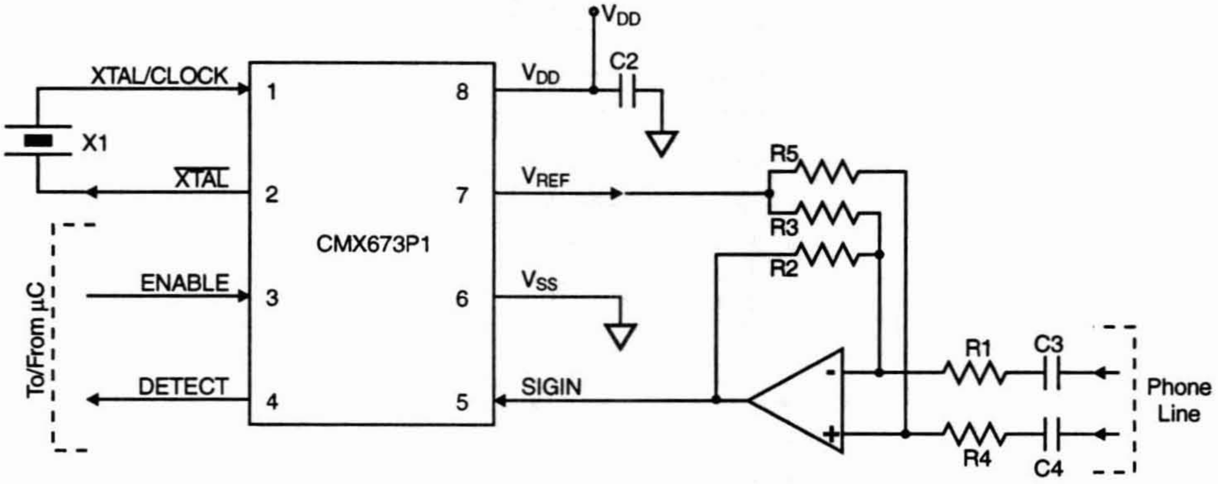
Table 3: Decode Output Truth Table

5 Application Notes

5.1 General

On power-up, it will take 80ms to initialize the internal state, this delay should be accounted for before the DETECT output is valid.

5.1.1 Typical Telephone Line Circuit



V_{DD}
XTAL/CLOCK
1
8
V_{DD}
C2
X1
$\overline{XTAL}$
2
7
V_{REF}
R5
R3
R2
CMX673P1
To/From µC
ENABLE
3
6
V_{SS}
R1
C3
DETECT
4
5
SIGIN
-
+
Phone Line
R4
C4

Figure 3: A typical Telephone Line Circuit Application

R1	Note 1	470kΩ	±1%
R2	Note 1	470kΩ	±1%
R3	Note 1	240kΩ	±1%
R4	Note 1	470kΩ	±1%

R5	Note 1	160kΩ	±1%
C3	Note 1	0.01µF 250V	±2%
C4	Note 1	0.01µF 250V	±2%

Note:

1. Resistor and Capacitor tolerance levels are as indicated, unless otherwise stated.
2. A low offset opamp is needed.

An Alternative set of component values can be used:

R1	Note 1	499kΩ	±1%
R2	Note 1	499kΩ	±1%
R3	Note 1	54.9kΩ	±1%
R4	Note 1	499kΩ	±1%

R5	Note 1	49.9kΩ	±1%
C3	Note 1, 2	0.001µF (300V)	±2%
C4	Note 1, 2	0.001µF (300V)	±2%

Note:

1. Resistor and Capacitor tolerance levels are as indicated, unless otherwise stated.
2. A higher value of C3 and C4 will reduce the level sensitivity tolerance at around -38dBm.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P1 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13.0	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
D4 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13.0	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Xtal Frequency		3.57	3.59	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, S/N = 16dB, Noise Bandwidth = 5kHz,
V_{DD} = 3.0V to 5.0V, T_{AMB} = -40°C to 85°C, 0dB = 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ENABLE = '1')					
(V_{DD} = 5.0V)	1		1.0	1.5	mA
(V_{DD} = 3.0V)	1		0.5	1.0	mA
AC Parameters					
SIGIN pin					
Input Impedance	2		0.1		MΩ
Minimum Input Signal Level			-38.0		dB
Input Signal Dynamic Range		40.0			dB
Signal to Noise Ratio		16.0			
Xtal/Clock Input					
'High' Pulse Width	3	100			ns
'Low' Pulse Width	3	100			ns
Gain (input = 1mV_{RMS} at 100Hz)		20.0			dB
Level Detector					
Must Detect Signal Level	4	-38.0			dB
Must Not Detect Signal Level	4			-50.0	dB
Call Progress Band					
Must Detect Range		315		650	Hz
Must Not Detect Range	7	750		250	Hz
Logic Interface					
Input Logic "1" Level	5	80%			V_{DD}
Input logic "0" level	5			20%	V_{DD}
Input leakage current (V_{IN} = 0 to V_{DD})	5	-5.0		5.0	µA
Input Capacitance	5		10.0		pF
Output logic "1" level (I_{OH} = 120µA)	6	90%			V_{DD}
Output logic "0" level (I_{OL} = 360µA)	6			10%	V_{DD}

Notes:

1. Not including any current drawn from the detector pins by external circuitry.
2. Small signal impedance over the frequency range 100Hz to 2000Hz and at V_{DD} = 5.0V.
3. Timing for an external input to the XTAL/CLOCK pin.
4. Input signal level at V_{DD} = 5.0V, scale signal for different V_{DD}.
5. ENABLE pin.
6. DETECT pin.
7. Nominal values that are subject to dynamic tolerances within the signal analysis process, as a result of using stochastic signal processing techniques.

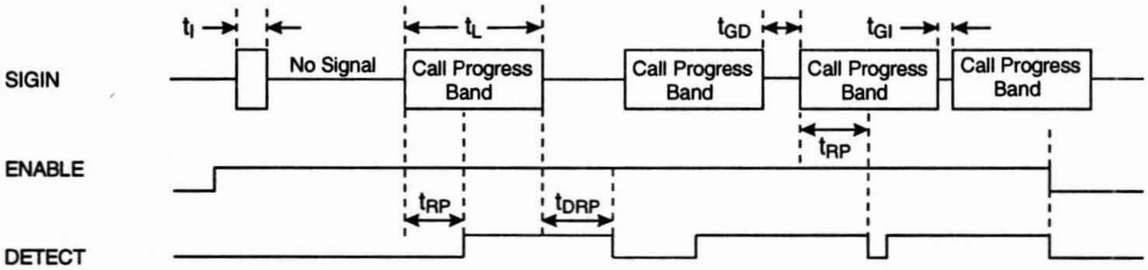
6.1.4 Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz, V_{DD} = 3.0V to 5.0V, T_{AMB} = -40°C to +85°C, S/N = 20dB.

Signal Timings		Notes	Min.	Typ.	Max.	Units
t_I	Burst Length Ignored				40.0	ms
t_L	Burst Length Detected		80.0			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1			20.0	ms
t_{GD}	Call Progress Tone Gap Length Detected	1	40.0			ms
t_{RP}	Call Progress Tone Response Time				80.0	ms
t_{DRP}	Call Progress Tone De-Response Time				80.0	ms

Notes:

1. Only applies to bursts of the same frequency.

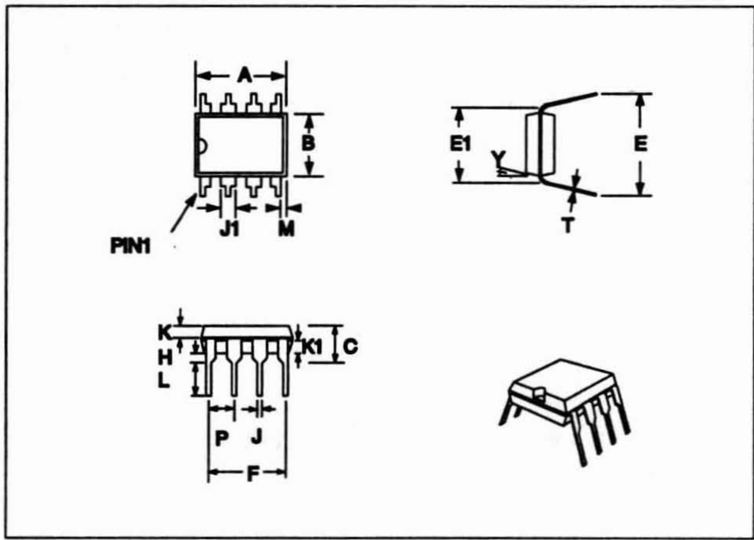


t_I
t_L
t_{GD}
t_{GI}
SIGIN
No Signal
Call Progress Band
Call Progress Band
Call Progress Band
Call Progress Band
t_{RP}
ENABLE
t_{RP}
t_{DRP}
DETECT

Figure 4: µC Parallel Interface Timings

6.2 Packaging

The CMX673 is available in the following packages. Additional package styles may be available to meet specific design requirements.



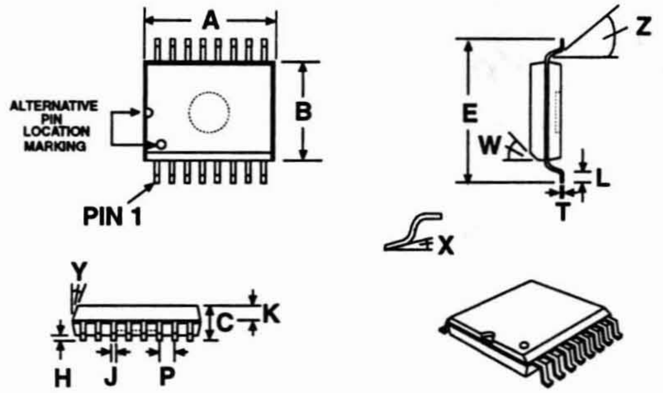
A
B
J1
M
PIN1
E1
Y
E
T
K
H
L
K1
C
P
J
F

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.346 (8.790)		0.400 (10.16)
B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.87).
E1	0.290 (7.37)		0.325 (8.22)
F		0.30 (7.62)	
H	0.015 (0.38)		0.040 (1.01)
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.060 (1.52)	
K1		0.060 (1.52)	
L	0.121 (3.07)		0.150 (3.81)
M	0.020 (0.51)		0.033 (0.84)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 8-pin PDIP Mechanical Outline: ***order as part no. CMX673P1***


A
B
ALTERNATIVE PIN LOCATION MARKING
PIN 1
E
Z
W
L
T
X
Y
C
K
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: ***order as part no. CMX673D4***

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

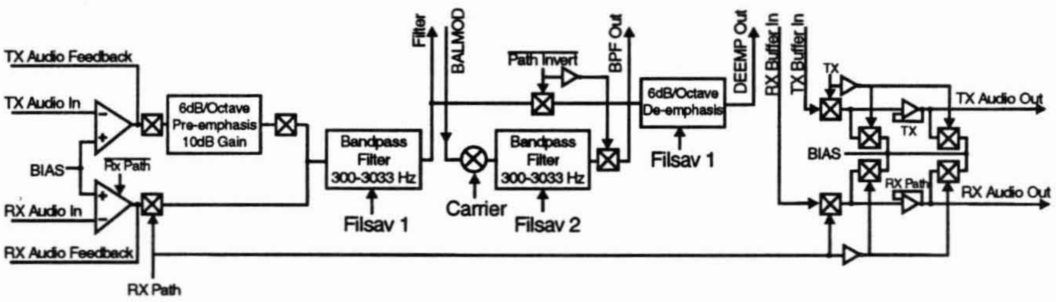
MX014 Voice Band inverter

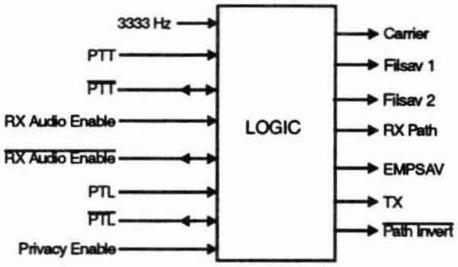
Features

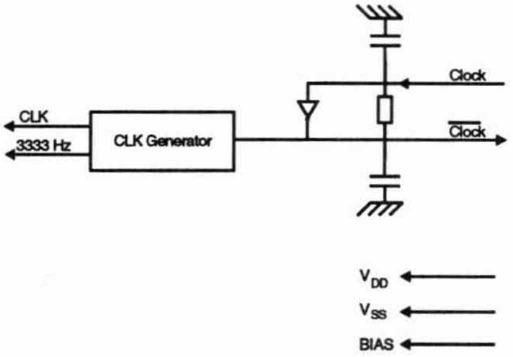
- CTCSS Compatible
- Fixed Frequency Inversion
- Low Power CMOS

Applications

- Land Mobile Radio Systems
- Community Repeaters


TX Audio Feedback
TX Audio In
BIAS
Rx Path
RX Audio In
RX Audio Feedback
RX Path
6dB/Octave Pre-emphasis 10dB Gain
Bandpass Filter 300-3033 Hz
Filsav 1
Filter
BALMOD
Carrier
Path Invert
Bandpass Filter 300-3033 Hz
Filsav 2
BPF Out
6dB/Octave De-emphasis
Filsav 1
DEEMP Out
RX Buffer In
TX Buffer In
TX
TX Audio Out
TX
BIAS
RX Path
RX Audio Out


3333 Hz
PTT
PTT
RX Audio Enable
RX Audio Enable
PTL
PTL
Privacy Enable
LOGIC
Carrier
Filsav 1
Filsav 2
RX Path
EMPSAV
TX
Path Invert


Clock
CLK
3333 Hz
CLK Generator
Clock
V_DD
V_SS
BIAS

The MX014 Voice Band Inverter gives the security of private voice communications to land mobile radio users, as well as to the users of other shared radio channel systems. Designed for use in half-duplex systems, the MX014 exchanges high and low frequencies in the voiceband and renders transmitted messages unintelligible. This privacy function is achieved by a single frequency inversion. When used with CTCSS, ***PvtSQUELCH***™ privacy adapter operation is achieved.

Sharp cut-off in the internal voiceband filters permits operation with CTCSS and similar sub-audio signaling schemes. This results in high quality recovered audio.

The core of the MX014 consists of two audio band pass filters and a balanced modulator. The device uses a programmable clock divider which controls the carrier and filter cut-off frequencies. Control of the RX/TX, PTL and privacy function is by pin selection.

The MX014 operates from a single 5V supply and uses a 4 MHz crystal oscillator to ensure the correct pitch in recovered speech. Signal coupling and decoupling are the only external components needed. The device is available in 24-pin PLCC (MX014LH), 24-pin PDIP (MX014P) and 24-pin CDIP (MX014J) packages.

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

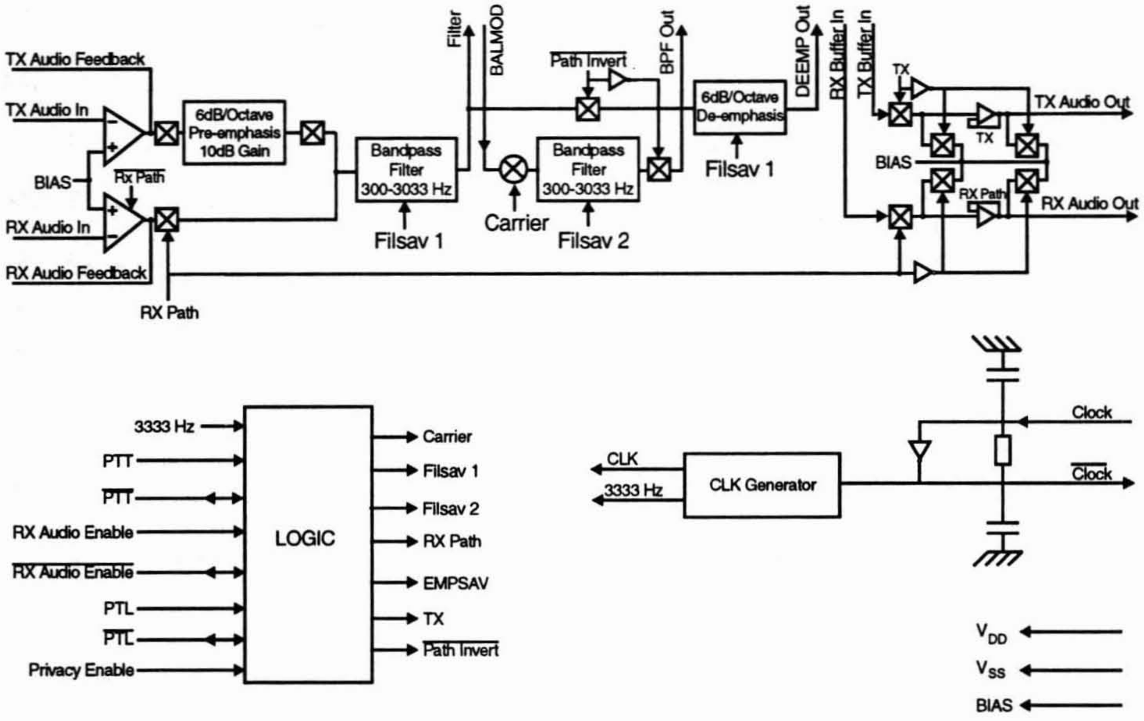

TX Audio Feedback
TX Audio In
BIAS
$\overline{\text{Rx Path}}$
RX Audio In
RX Audio Feedback
RX Path
6dB/Octave Pre-emphasis 10dB Gain
Bandpass Filter 300-3033 Hz
Filsav 1
Filter
BALMOD
Carrier
$\overline{\text{Path Invert}}$
Bandpass Filter 300-3033 Hz
Filsav 2
BPF Out
6dB/Octave De-emphasis
Filsav 1
DEEMP Out
RX Buffer In
TX Buffer In
TX
TX Audio Out
TX
BIAS
RX Path
RX Audio Out
3333 Hz
PTT
$\overline{\text{PTT}}$
RX Audio Enable
$\overline{\text{RX Audio Enable}}$
PTL
$\overline{\text{PTL}}$
Privacy Enable
LOGIC
Carrier
Filsav 1
Filsav 2
RX Path
EMPSAV
TX
$\overline{\text{Path Invert}}$
CLK
3333 Hz
CLK Generator
Clock
$\overline{\text{Clock}}$
V_{DD}
V_{SS}
BIAS

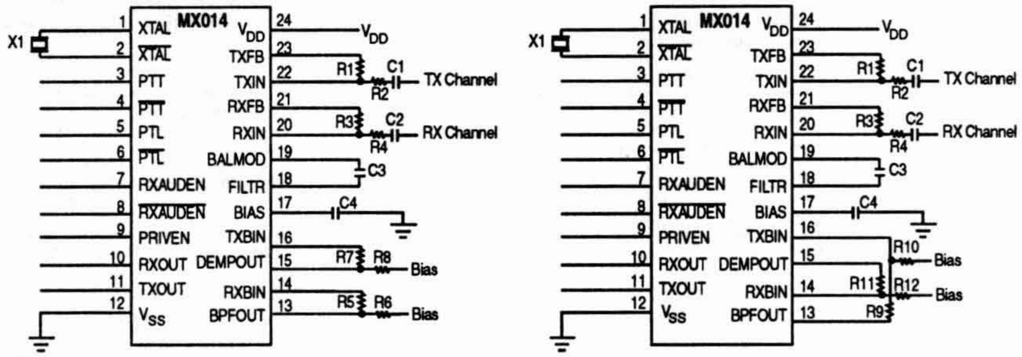
Figure 1: Device Block Diagram

2. Signal List

Pin No.	Name	Description
1	XTAL	An external 4MHz clock can be applied to this input. The clock circuit on chip has a resistor and capacitors so that only one external crystal is required.
2	$\overline{\text{XTAL}}$	This is the inverted 4MHz clock output for use when a crystal oscillator is used, or as a buffer for driving other clocked devices.
3	PTT	Push To Talk is an input with a 3MΩ pull-down resistor.
4	$\overline{\text{PTT}}$	This is the inverted PTT output. It has a 100kΩ output impedance.
5	PTL	Push To Listen is an input with a 3MΩ pull-down resistor.
6	$\overline{\text{PTL}}$	$\overline{\text{Push To Listen}}$ is the inverted output of PTL; it has a 100kΩ output impedance.
7	RXAUDEN	RX Audio Enable is an input with a 3MΩ pull-down resistor.
8	$\overline{\text{RXAUDEN}}$	$\overline{\text{RX Audio Enable}}$ is the inverted output of RX Audio Enable; it has a 100kΩ output impedance.
9	PRIVEN	Privacy Enable controls the input action of the balanced modulator by switching the carrier clock. When audio signals are inverted, the signal path gain is adjusted automatically to compensate for the upper sideband loss. It contains a 3MΩ pull-down resistor.
10	RXOUT	This is the receive audio output pin. It is biased at $V_{DD}/2$ when in the TX mode.
11	TXOUT	This is the "send" voice output pin. It is biased at $V_{DD}/2$ when in RX mode.
12	V_{SS}	The negative supply pin (ground).
13	BPFOUT	For a gain of one in the RX Output stage, these two pins are wire linked together. However, if gain is introduced at the RX input, attenuation may be introduced at the RX Output using these pins and two resistors.
14	RXBIN	
15	DEMPOUT	The pre-emphasis circuit has a 10dB gain at 1 kHz. Additional gain, or attenuation can be introduced as in the RX path.
16	TXBIN	
17	BIAS	This is the internally generated $V_{DD}/2$ decoupling pin.
18	FILTR	This filter is the output of the Input Audio BPF and must be a.c. coupled into the Balanced Modulator Input through a 0.1µF capacitor.
19	BALMOD	This is the input to the balanced modulator. It must be a.c. coupled to the Filter Output.
20	RXIN	This is a negative input of an op-amp at the input of the RX path. It can be used, along with RX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve the S/N.
21	RXFB	RX Audio Feedback is the output of an op-amp at the input of the RX path. See RXIN.
22	TXIN	The negative input of an op-amp at the input of the TX path. It can be used, along with TX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve S/N.
23	TXFB	TX Audio Feedback is the output of an op-amp at the input of the TX path. See TXIN.
24	V_{DD}	The positive supply pin.

Table 1: Signal List

3. External Components



Configuration for Radios with Existing Pre- and De-emphasis.

For Use in Radios without Pre- and De-emphasis.

X1
MX014
1 XTAL
2 XTAL
3 PTT
4 PTT
5 PTL
6 PTL
7 RXAUDEN
8 RXAUDEN
9 PRIVEN
10 RXOUT
11 TXOUT
12 V_{SS}
24 V_{DD}
23 TXFB
22 TXIN
21 RXFB
20 RXIN
19 BALMOD
18 FILTR
17 BIAS
16 TXBIN
15 DEMPOUT
14 RXBIN
13 BPFOUT
V_{DD}
R1
R2
C1
TX Channel
R3
R4
C2
RX Channel
C3
C4
R7
R8
R5
R6
R9
R10
R11
R12
Bias

Figure 2: External Components Connections

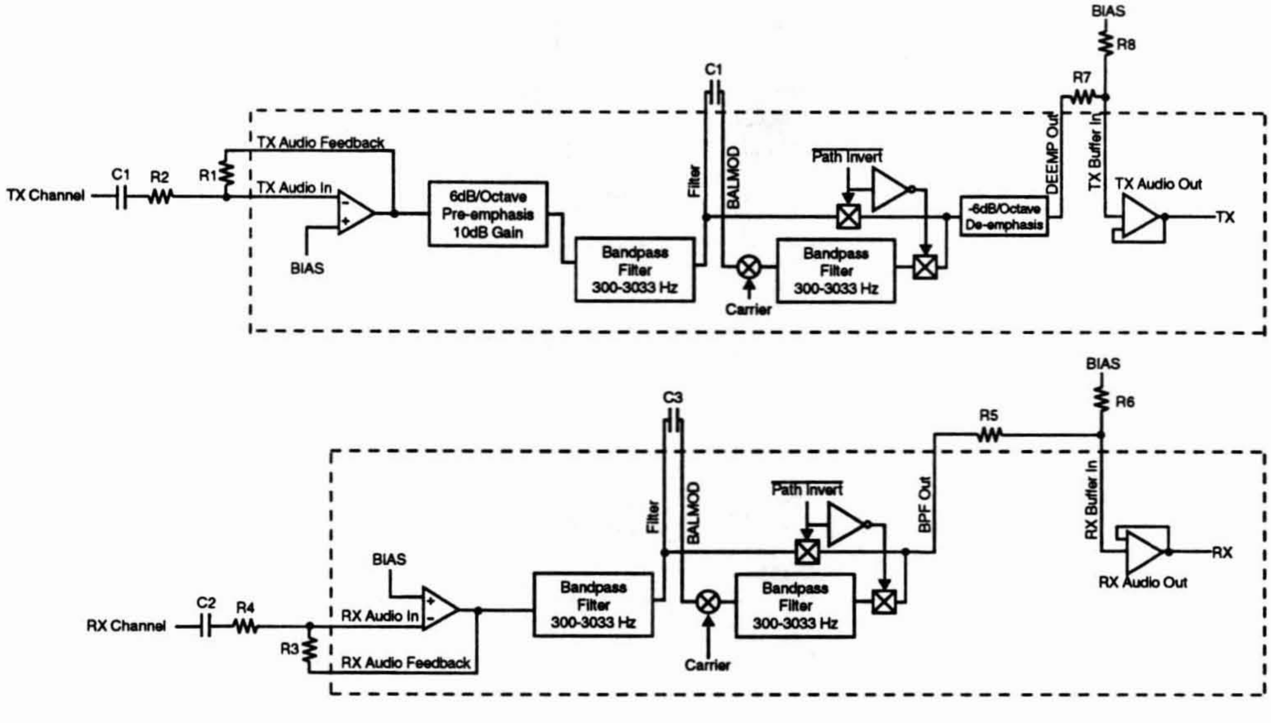
TX Attenuation = $\frac{R8}{R7+R8}$ For a gain of 1, R8 = ∞, R7 = 0	TX Attenuation = $\frac{R10}{R9+R10}$ For a gain of 1, R9 = 0, R10 = ∞
RX Attenuation = $\frac{R6}{R5+R6}$ For a gain of 1, R6 = ∞, R5 = 0	RX Attenuation = $\frac{R12}{R11+R12}$ For a gain of 1, R11= 0, R12 = ∞

Table 2: Gain and Attentuation Calculations

Recommended External Component Notes:

1. Component Values: C1- C3 = 0.1 µF, C4 = 1.0 µF, X1 = 4 MHz crystal
2. R1 to R12 values will depend on the configuration and the gain or attenuation required. However R1, R3, R5, R7, and R11 should be 100 kΩ or greater. To add gain or attenuate, use R5-R12 as shown. See pin descriptions for more information.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of VDD, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

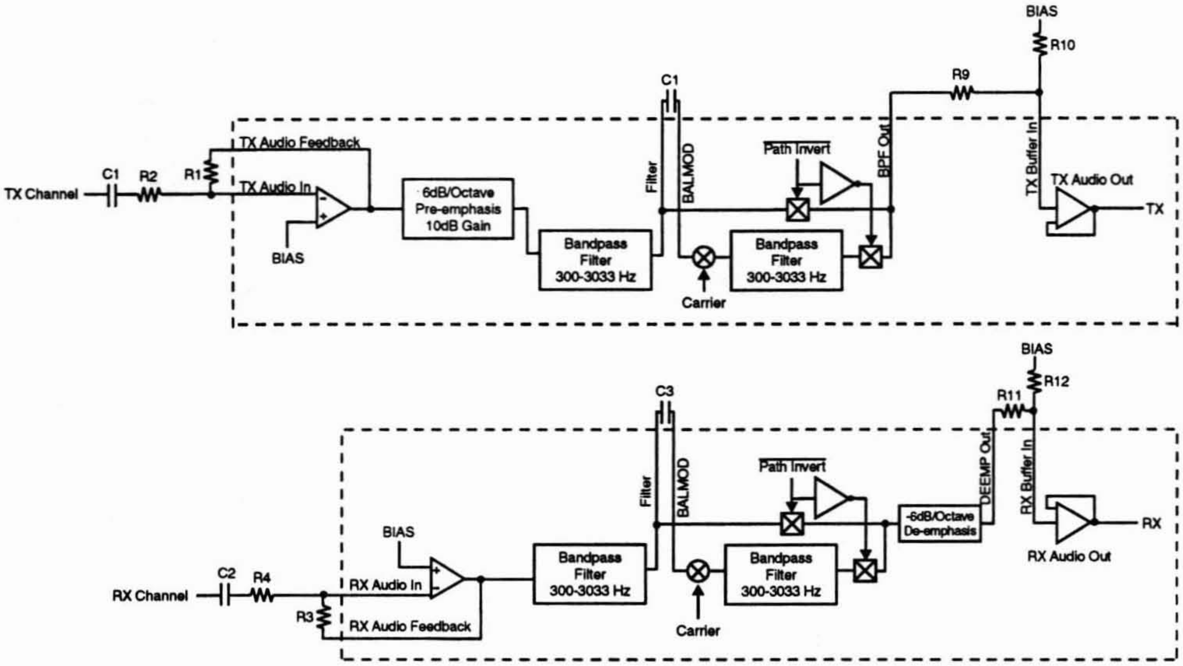
4. Application



BIAS
R8
C1
R7
TX Audio Feedback
C1
R2
R1
TX Channel
TX Audio In
BIAS
6dB/Octave Pre-emphasis 10dB Gain
Bandpass Filter 300-3033 Hz
Filter
BALMOD
Carrier
Path Invert
Bandpass Filter 300-3033 Hz
-6dB/Octave De-emphasis
DEEMP Out
TX Buffer In
TX Audio Out
TX
BIAS
R6
C3
R5
Filter
BALMOD
Path Invert
BPF Out
RX Buffer In
BIAS
Bandpass Filter 300-3033 Hz
Bandpass Filter 300-3033 Hz
RX
RX Audio Out
C2
R4
RX Channel
RX Audio In
R3
RX Audio Feedback
Carrier

Note: Dotted Lines contain on-chip functions

Figure 3: Voice Privacy Application (Add-on)


BIAS
R10
R9
C1
TX Audio Feedback
Path Invert
BPF Out
Filter
BALMOD
TX Buffer In
TX Audio Out
TX
TX Channel
C1
R2
R1
TX Audio In
BIAS
6dB/Octave
Pre-emphasis
10dB Gain
Bandpass
Filter
300-3033 Hz
Carrier
Bandpass
Filter
300-3033 Hz
BIAS
R12
R11
C3
Path Invert
DEEMP Out
RX Buffer In
Filter
BALMOD
-6dB/Octave
De-emphasis
RX
RX Audio Out
BIAS
Bandpass
Filter
300-3033 Hz
Bandpass
Filter
300-3033 Hz
RX Channel
C2
R4
RX Audio In
R3
RX Audio Feedback
Carrier

Note: Dotted Lines contain on-chip functions

Figure 4: Voice Processing Application (OEM)

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0	V
Input Voltage at any pin			
(ref. V_{SS} + 0 V)	-0.3	(V_{DD} + 0.3)	V
Current:			
V_{DD}		30	mA
V_{SS}		30	mA
Any other pin		20	mA
J / P / LH Packages			
Maximum Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature Range:	-40	85	°C
Storage Temperature Range:	-55	125	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	4.5	5.0	5.5	V
Clock Frequency		4.0		MHz
Operating Temperature	-40		85	°C

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V at T_{AMB} = 25°C
Clock Frequency = 4.0MHz, 0dB reference = 300mV$_{RMS}$ (Note: Measured at pin 18, the FILTR output. This pin must not exceed 300mV$_{RMS}$ at 1kHz in Tx and 500mV$_{RMS}$ at any frequency in Rx, or clipping may occur. The difference in levels is due to the pre-emphasis filter in the Tx path.

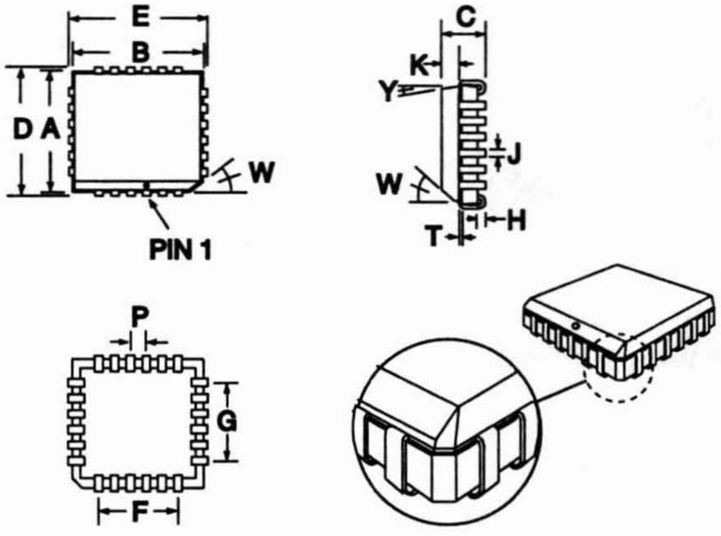
	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current:					
RX/TX Operating (Private)				11.0	mA
RX/TX Operating (Clear)				8.0	mA
Standby	4			1.8	mA
Audio Input Impedance			10		MΩ
Audio Output Impedance	5		0.5		kΩ
Digital Output Impedance(Pulldown)		1			MΩ
Digital I/O Impedance			100		kΩ
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}

	Notes	Min.	Typ.	Max	Units
RX Clear Performance					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mV_{RMS}
Passband Gain			0		dB
Passband Ripple (300-3033 Hz)	1	-3		+2	dB
Stopband Attenuation					
(fin > 3333 Hz)			20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 Hz)			42		dB
RX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2,3		4		mV_{RMS}
Passband Ripple (300 - 3033 Hz)	3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)			50		dB
(fin > 3633 Hz)			60		dB
Highpass Attenuation					
(fin < 250 Hz)			60		dB
TX Clear					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mV_{rms}
Passband Gain					
(fin = 300 - 3033 Hz)	1		0		dB
Passband ripple					
(fin = 300 - 3033 Hz)	1			4	dB
Stopband Attenuation					
(fin > 3333 Hz)	2		20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 Hz)			42		dB
TX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2		4		mV_{rms}
Passband Ripple					
(fin = 300 - 3333 Hz)	1,3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)	3		50		dB
(fin > 3633 Hz)	3		60		dB
(fin < 250 Hz)	3		60		dB
Pre-Emphasis					
Frequency Response			6		dB/Octave
Gain at 1 kHz			10		dB
De-emphasis					
Frequency response			-6		dB/Octave
Gain at 1 kHz			0		dB

Operating Characteristics Notes:

1. Input signal = 1kHz tone 0dB (300 mV_{RMS})
2. Input AC short circuit, audio path enabled. Measured in 30 kHz band
3. Due to frequency inversion (and pre- and de-emphasis), this refers to deviation from expected ideal response
4. Standby occurs in RX with RX Audio Enable = 0, RX Audio Enable = 1, and PTL = 1
5. TX Audio Out and RX Audio Out only

5.2 Packaging

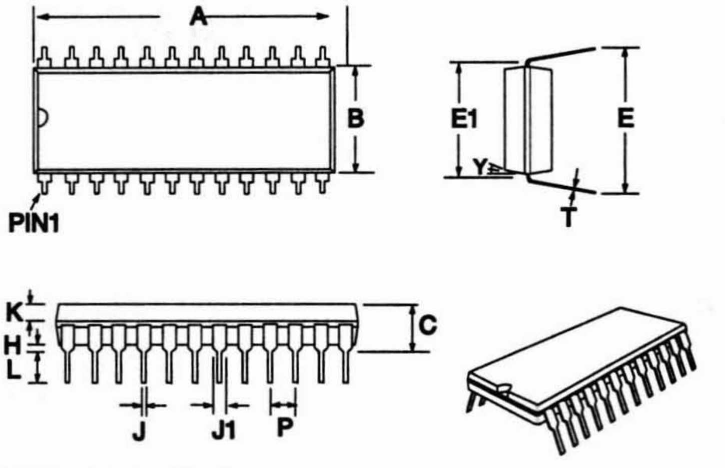


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin PLCC Mechanical Outline: Order as part no. MX014LH

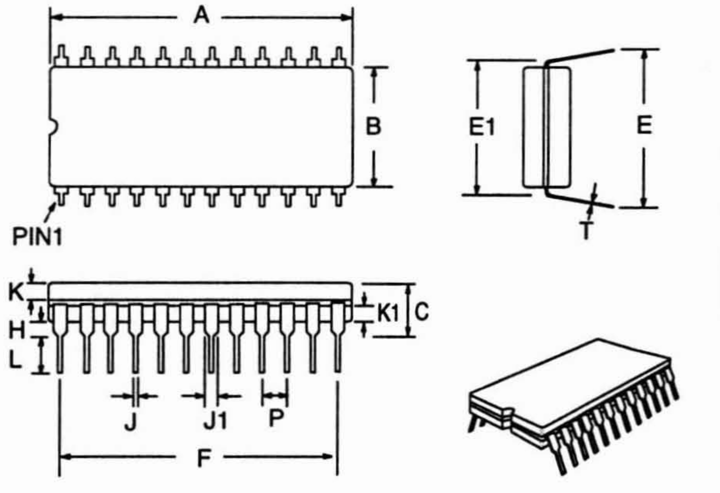


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin PDIP Mechanical Outline: Order as part no. MX014P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin CDIP Mechanical Outline: Order as part no. MX014J

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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

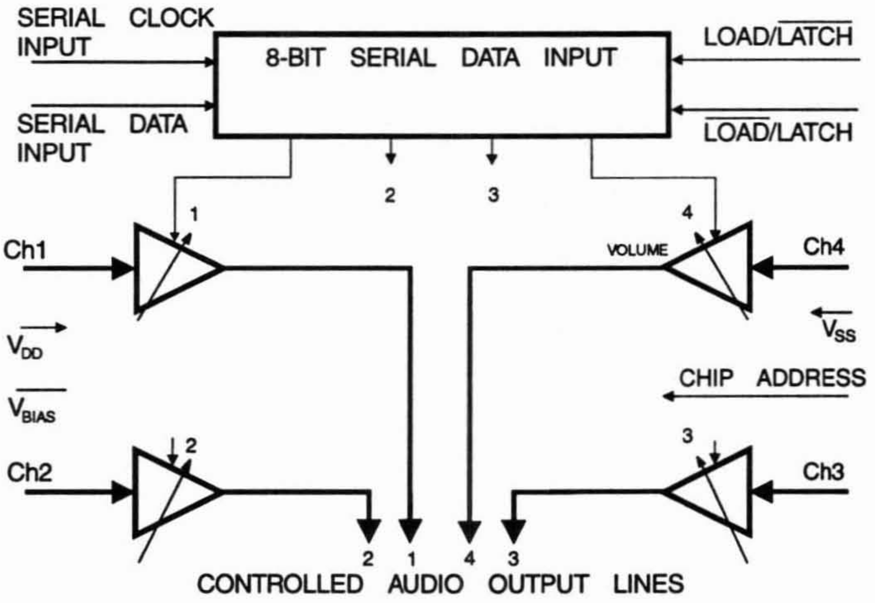
MX019 Quad Digital Control Amplifier

FEATURES

- 4 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps
- 3 Amplifiers
  ± 3dB Range in 0.43dB Steps
- 1 'Volume' Amplifier
  ±14dB Range in 2dB Steps
- 8-Bit Serial Data Control
- Output Mute Function

APPLICATIONS

- Gain Control Applications
  - Audio
  - Data
- Telecommunications, Radio, & Industrial Applications



The MX019 Digitally Adjustable Amplifier Array replaces trimmer potentiometers and volume controls in Cellular, LMR, Telephony and Communication applications where voice or data signals need adjustment.

The MX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a ±3dB range in steps of 0.43dB, while the remaining amplifier offers a ±14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which, when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two MX019s in a system. The MX019 uses the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration, and operation. Such applications include:

1. Control, adjustment, and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, RX Audio Level etc.
2. Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.
3. Fully automated servicing and re-alignment.

The MX019 is a low-power, single 5-volt CMOS device available in 24-pin TSSOP (MX019TN), 16-pin SOIC (MX019DW), 16-pin CDIP (MX019J) and 16-pin PDIP (MX019P) package versions.

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

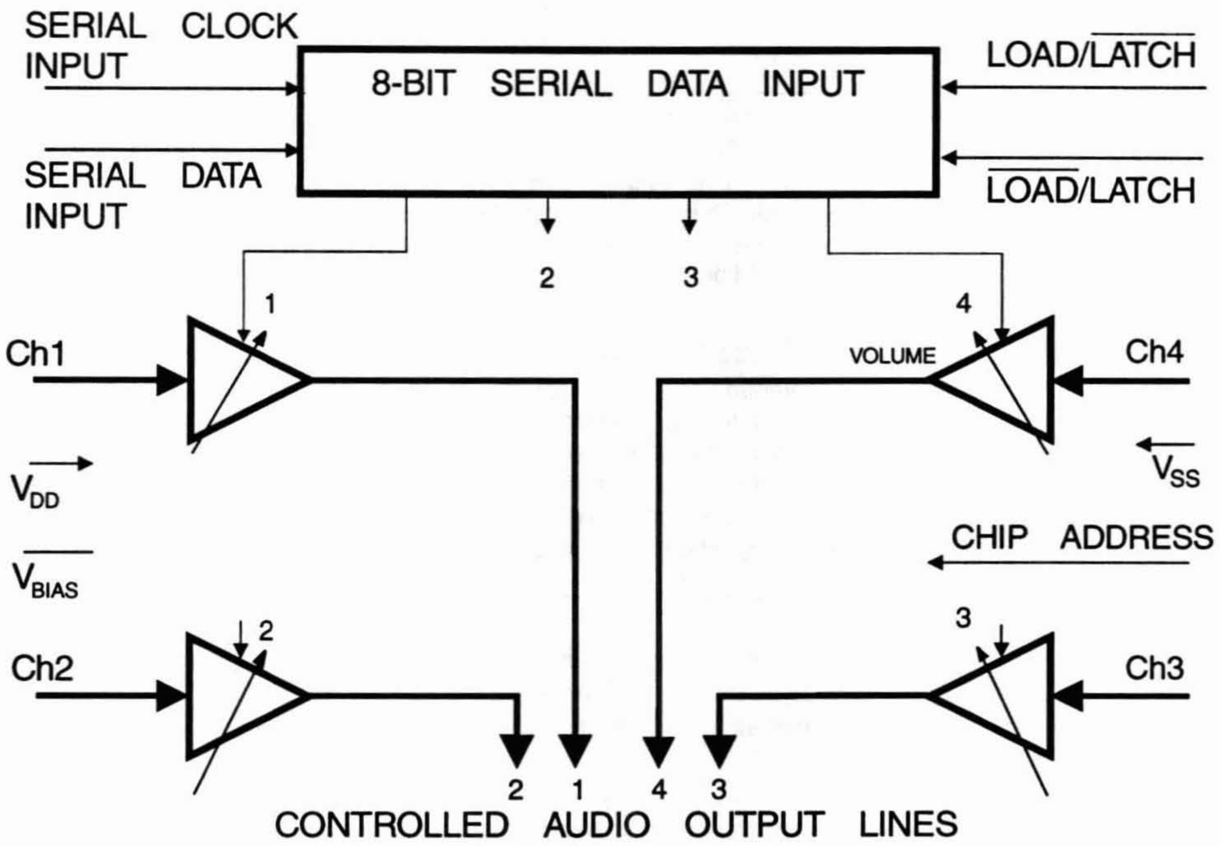
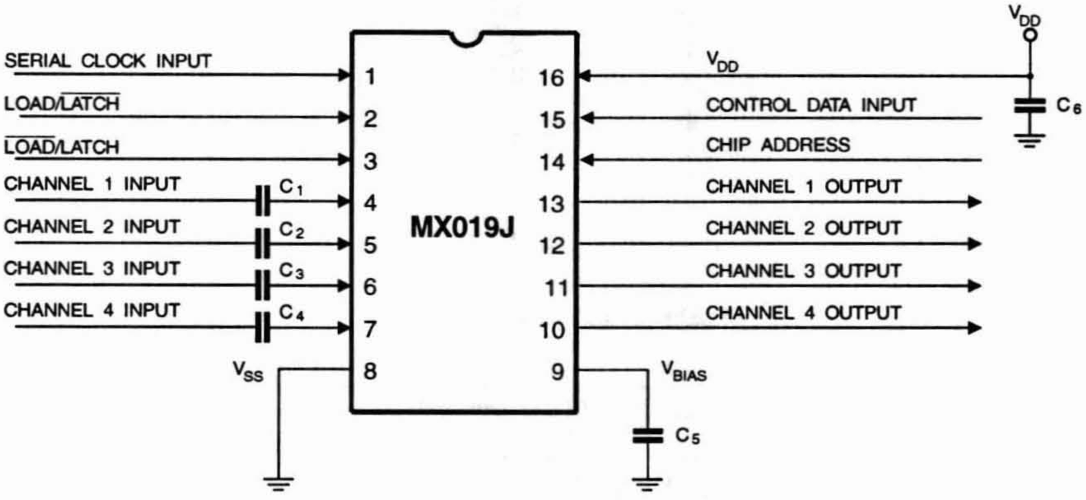

SERIAL CLOCK INPUT
SERIAL DATA INPUT
8-BIT SERIAL DATA INPUT
LOAD/$\overline{\text{LATCH}}$
$\overline{\text{LOAD}}$/LATCH
2
3
1
4
Ch1
VOLUME
Ch4
V_{DD}
V_{SS}
$\overline{V_{BIAS}}$
CHIP ADDRESS
2
3
Ch2
Ch3
2
1
4
3
CONTROLLED AUDIO OUTPUT LINES

Figure 1: Device Block Diagram

2. Signal List

Pin No.		Name	Description
J/P DW	TN		
1	1	Serial Clock	This external clock pulse input is used to "clock in" the Control Data. See Figure 3. This input has an internal 1MΩ pullup resistor.
2	2	Load/$\overline{\text{Latch}}$	This input governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0 - 1 - 0' to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load}}$/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	4	$\overline{\text{LOAD}}$/LATCH	This inverted Load/$\overline{\text{Latch}}$ input governs the loading and execution of control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	5	Ch1 Input	**Analog Inputs :** These individual amplifier inputs are self-biasing; AC input analog signals must be capacitively coupled to these pins, as shown in Figure 2. Note that amplifiers Ch1 to Ch4 are 'inverting amplifiers.'
5	6	Ch2 Input	
6	7	Ch3 Input	
7	8	Ch4 Input	
8	12	V_{SS}	Negative supply rail (GND).
9	13	V_{BIAS}	The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{ss} as shown in Figure 2.
10	14	Ch4 Output	**Controlled Analog Outputs :** These are individual "Gain Controlled" amplifier outputs. Ch1 to Ch3 range from -3dB to +3dB in 0.43dB steps, Ch4 can be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps. In the "OFF" mode there is no output from the selected amplifier.
11	17	Ch3 Output	
12	18	Ch2 Output	
13	19	Ch1 Output	
14	20	Chip Address	A logic input to select one of two MX019 ICs in a system (see Table 1). This input has an internal 1MΩ pulldown resistor.
15	23	Control Data Input	Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Table 1, Table 2 and Figure 3. This input has an internal 1MΩ pullup resistor.
16	24	V_{DD}	Positive supply rail. A single +5V power supply is required.

3. External Components


SERIAL CLOCK INPUT
LOAD/$\overline{\text{LATCH}}$
$\overline{\text{LOAD}}$/LATCH
CHANNEL 1 INPUT
CHANNEL 2 INPUT
CHANNEL 3 INPUT
CHANNEL 4 INPUT
C1
C2
C3
C4
V_{SS}
MX019J
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{DD}
CONTROL DATA INPUT
CHIP ADDRESS
CHANNEL 1 OUTPUT
CHANNEL 2 OUTPUT
CHANNEL 3 OUTPUT
CHANNEL 4 OUTPUT
V_{BIAS}
C5
V_{DD}
C6

C1 to C4	0.1µF	± 20%
C5	1.0µF	± 20%
C6	1.0µF	± 20%

Figure 2: Recommended External Components

Notes:

1. Channel Amplifiers 1 to 4 are inverting amplifiers.
2. Analog input capacitors C1 to C4 are only required for AC input signals, DC input signals do not require these components.

4. General Description

4.1 Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the MX019 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

4.1.1 Data Loading

The 8-bit data word is loaded bit 7 first and bit 0 last.

Bit 7 must be a logic "1" to address the chip.

If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Address input permits the use of two devices in a system by indicating to the chip what its address is, a "1" or a "0." Bit 6 in the address section of the control word is then used to select which device is being controlled. Figure 3 shows the timing information required to load and operate this device.

Data is loaded to the MX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/$\overline{\text{Latch}}$ ($\overline{\text{Load}}$/Latch) pulse.

Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 3 describing the data loading operation and timing.

Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Address	Chip Address	Chip Number
1	0	0	0	1	0	Chip 1
1	0	0	1	2	0	
1	0	1	0	3	0	
1	0	1	1	4	0	
1	1	0	0	1	1	Chip 2
1	1	0	1	2	1	
1	1	1	0	3	1	
1	1	1	1	4	1	

Table 1: Address Bits Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1, 2, 3 (0.43dB)	Stage 4 (2.0dB)
0	0	0	0	OFF	OFF
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0
0	0	1	1	-2.143	-10.0
0	1	0	0	-1.714	-8.0
0	1	0	1	-1.286	-6.0
0	1	1	0	-0.857	-4.0
0	1	1	1	-0.428	-2.0
1	0	0	0	0	0
1	0	0	1	0.428	2.0
1	0	1	0	0.857	4.0
1	0	1	1	1.286	6.0
1	1	0	0	1.714	8.0
1	1	0	1	2.143	10.0
1	1	1	0	2.571	12.0
1	1	1	1	3.0	14.0

Table 2: Gain Control Bits Format

4.1.2 Timing

Timing (Figure 3)		**Min.**	**Typ.**	**Max.**	**Units**
Serial Clock "High" Pulse Width	(t_{PWH})	250			ns
Serial Clock "Low" Pulse Width	(t_{PWL})	250			ns
Data Set-up Time	(t_{DS})	150			ns
Data Hold Time	(t_{DH})	50.0			ns
Load/Latch Pulse Width	(t_{LLW})	150			ns
Load/Latch Delay	(t_{LLD})	200			ns
Load/Latch Over	(t_{LLO})			0.0	ns
Serial Data Clock Frequency				2.0	MHz

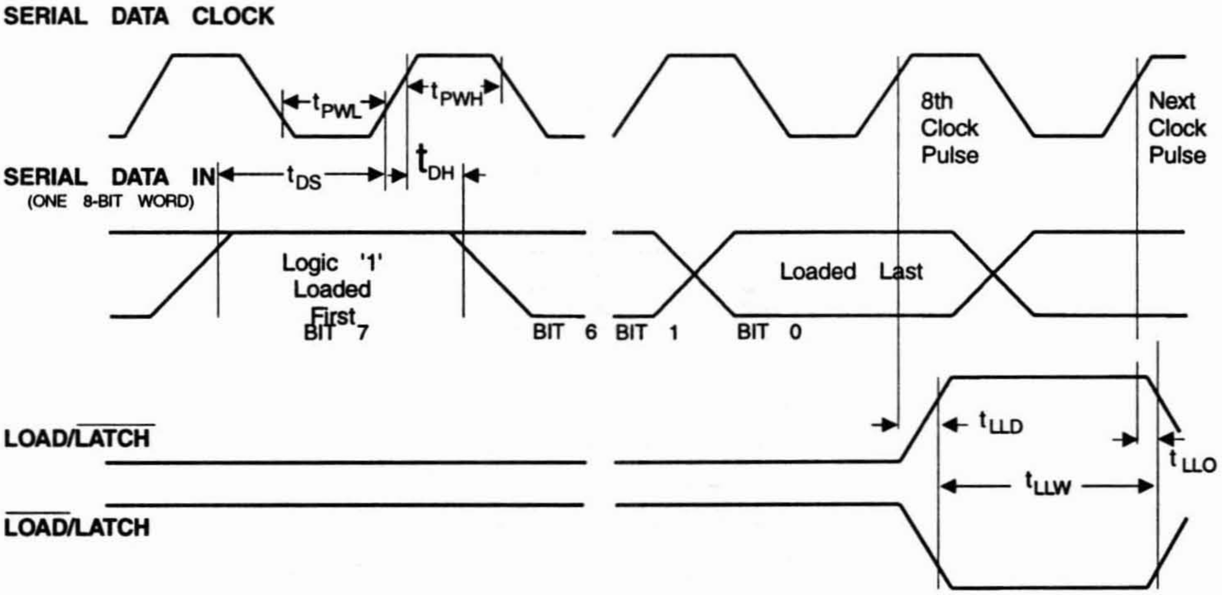

SERIAL DATA CLOCK
tPWL
tPWH
8th Clock Pulse
Next Clock Pulse
SERIAL DATA IN
(ONE 8-BIT WORD)
tDS
tDH
Logic '1' Loaded First
BIT 7
BIT 6
BIT 1
BIT 0
Loaded Last
LOAD/LATCH
tLLD
tLLO
tLLW
LOAD/LATCH

Figure 3: Serial Control Data Loading Diagram

5. Application

To avoid excess noise and instability you should take note of the following:

1. A noisy or badly regulated power supply can cause instability and/or variance of selected gains.
2. Care should be taken on the design and layout of the printed circuit board.
3. All external components (Figure 2) should be kept close to the MX019 package.
4. Inputs and outputs should be shielded wherever possible.
5. Tracks should be kept short.
6. Analog tracks should not run parallel to digital tracks.
7. A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.
8. Do not run high-level output tracks close to low-level input tracks.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply Voltage	-0.3	7.0	V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3	(V_{DD} + 0.3)	V
Current			
V_{DD}		±30	mA
V_{SS}		±30	mA
Any other pins		±20	mA
J/P/DW Packages			
Total Device Dissipation @ T_{AMB} 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
TN Packages			
Total Device Dissipation @ T_{AMB} 25°C		500	mW
Derating above 25°C		9	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	**Typ.**	**Max.**	**Units**
V_{DD}	4.5	5.0	5.5	V
Operating Temperature	-40		85	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C
Audio Level 0dB ref. = 775mV$_{RMS}$, Amplifier Gain Set = 0dB

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			1.5		mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5			V
Input Logic '0'				1.5	V
Digital Input Impedances		0.5	1.0		MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		20.0			kHz
Output Impedance			1.0		kΩ
Total Harmonic Distortion	1		0.35	0.5	%
Output Noise Level (per stage)	2		180.0	400.0	µV$_{RMS}$
Onset of Clipping	3		1.73		V$_{RMS}$
Gain Variation	4			0.1	dB
Interstage Isolation			60.0		dB
"Trimmer" Stages (Ch1 – Ch3)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)			0.43		dB
Step Error				0.2	dB
Input Impedance		100.0			kΩ
"Volume" Stage (Ch4)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)			2.0		dB
Step Error				0.4	dB
Input Impedance		50.0			kΩ

Operating Characteristics Notes:

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 4.
4. Over the temperature and supply voltage range.

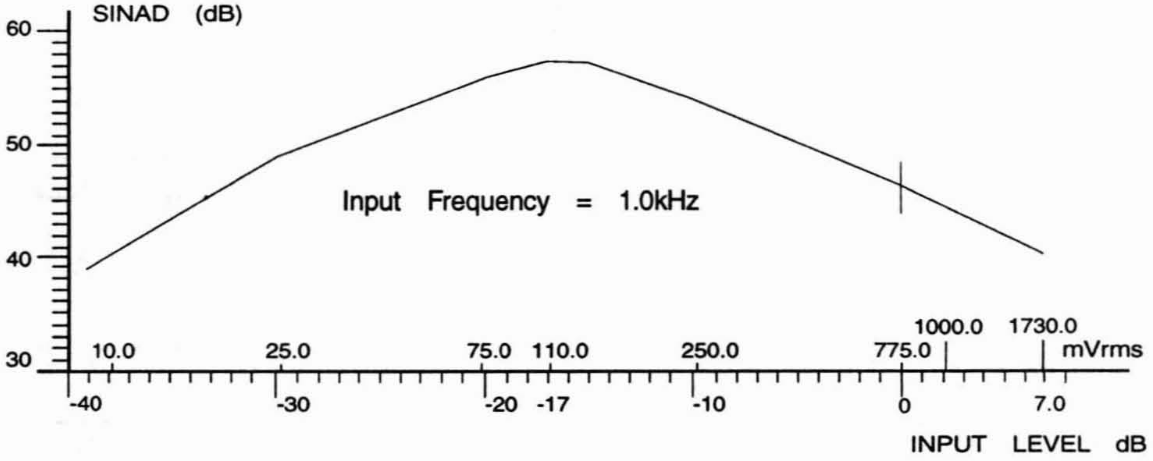
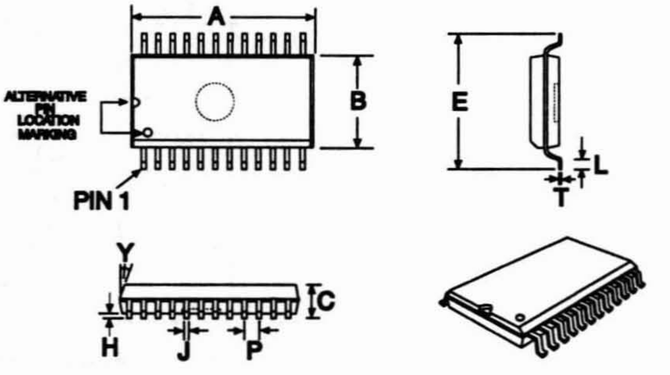


Figure 4: SINAD vs Input Level – Typical Values

6.2 Packaging

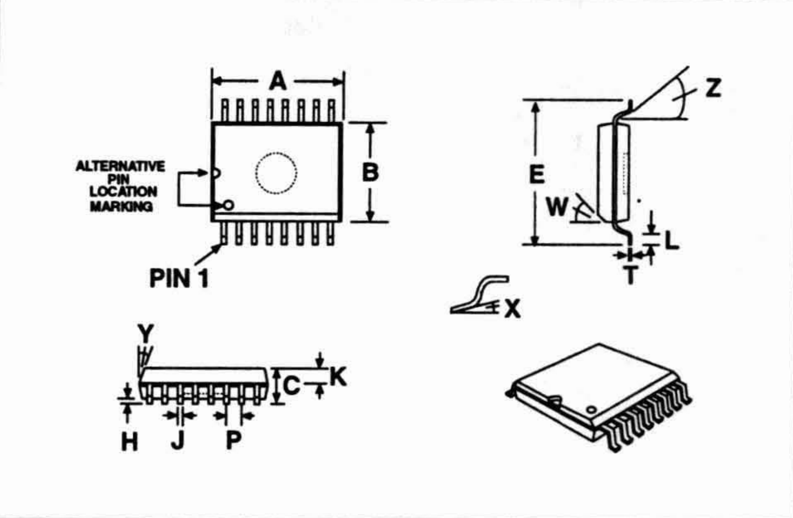

A
B
E
L
T
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	---------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin TSSOP Mechanical Outline: Order as part no. MX019TN

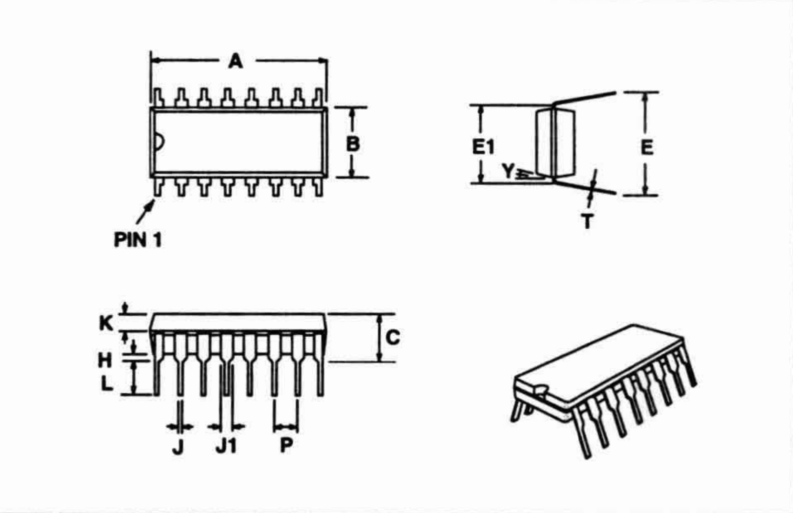


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: Order as part no. MX019DW

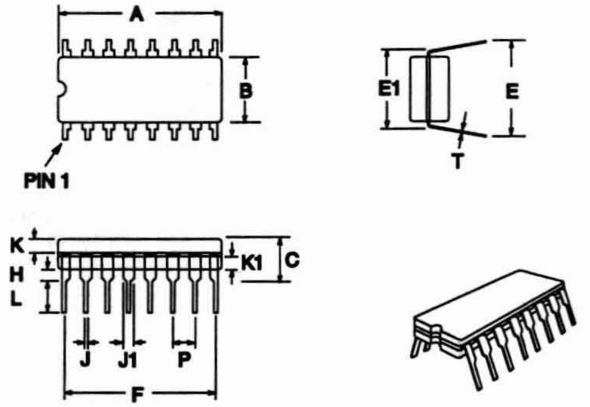


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin PDIP Mechanical Outline: Order as part no. MX019P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 16-pin CDIP Mechanical Outline: Order as part no. MX019J

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX029 Dual Digitally Controlled Amplifier

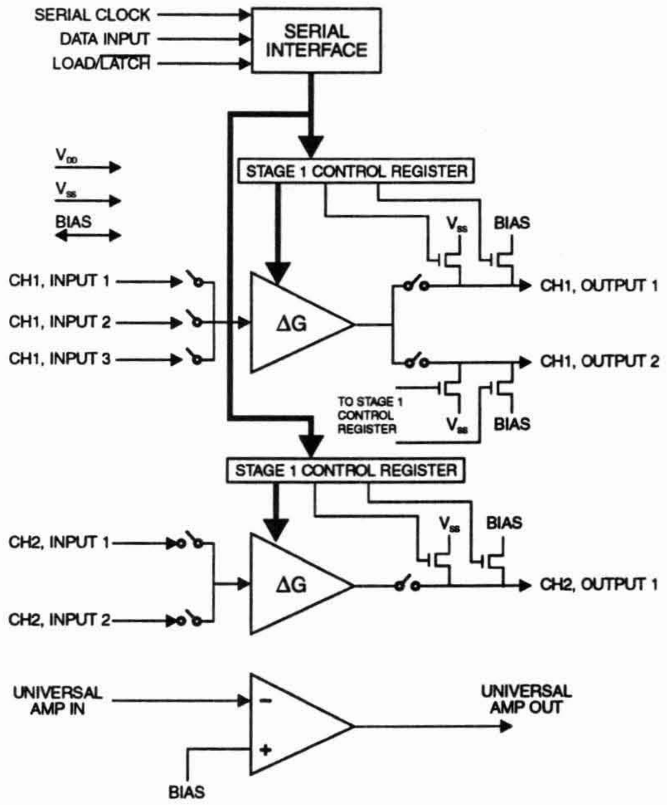
PRELIMINARY INFORMATION

Features

- 2 Digitally Controlled Amplifiers
- ±48dB Gain/Attenuation in 2dB Steps + Mute
- Individual Control with a 14-Bit Serial Word
- Separate Fixed Gain Buffer Amplifier

Applications

- Cellular and LMR Radios
- PABX's, Electronic Mail, TAM's
- Automatic Test Equipment
- Remote Gain Adjustments
- Digitally Set Audio Control Levels


SERIAL CLOCK
DATA INPUT
LOAD/$\overline{\text{LATCH}}$
SERIAL INTERFACE
V_{DD}
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH1, INPUT 1
CH1, INPUT 2
CH1, INPUT 3
ΔG
CH1, OUTPUT 1
CH1, OUTPUT 2
TO STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH2, INPUT 1
CH2, INPUT 2
ΔG
CH2, OUTPUT 1
UNIVERSAL AMP IN
UNIVERSAL AMP OUT
BIAS

The MX029 Digitally Controlled Amplifier Array replaces audio level controls in radio and wireline communications applications. It is a single-chip LSI circuit comprised of two discrete, digitally controlled gain sections. Each section has 48 distinct gain steps (+/-48dB of range in 2dB steps) plus MUTE.

As shown in Figure 1, both gain stages have switchable inputs. This switching allows for selection of three different input signals on one channel and two on the other channel. One of the channels also has output switching. In addition to two digitally controlled gain stages, there is a general purpose inverting amplifier. The gain of this amplifier is controlled externally via negative feedback. Control of each gain control section is accomplished through the serial interface. All switching is accomplished using controlled rise and fall times, thereby assuring no transients (clicks or pops).

The MX029 requires a single 5-volt supply and is available in the following packages: 16-pin SOIC (MX029DW), 16-pin CDIP (MX029J), and 24-pin TSSOP (MX029TN).

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3. External Components ...... **3 - 169**

4. Application ...... **3 - 169**
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1. Block Diagram

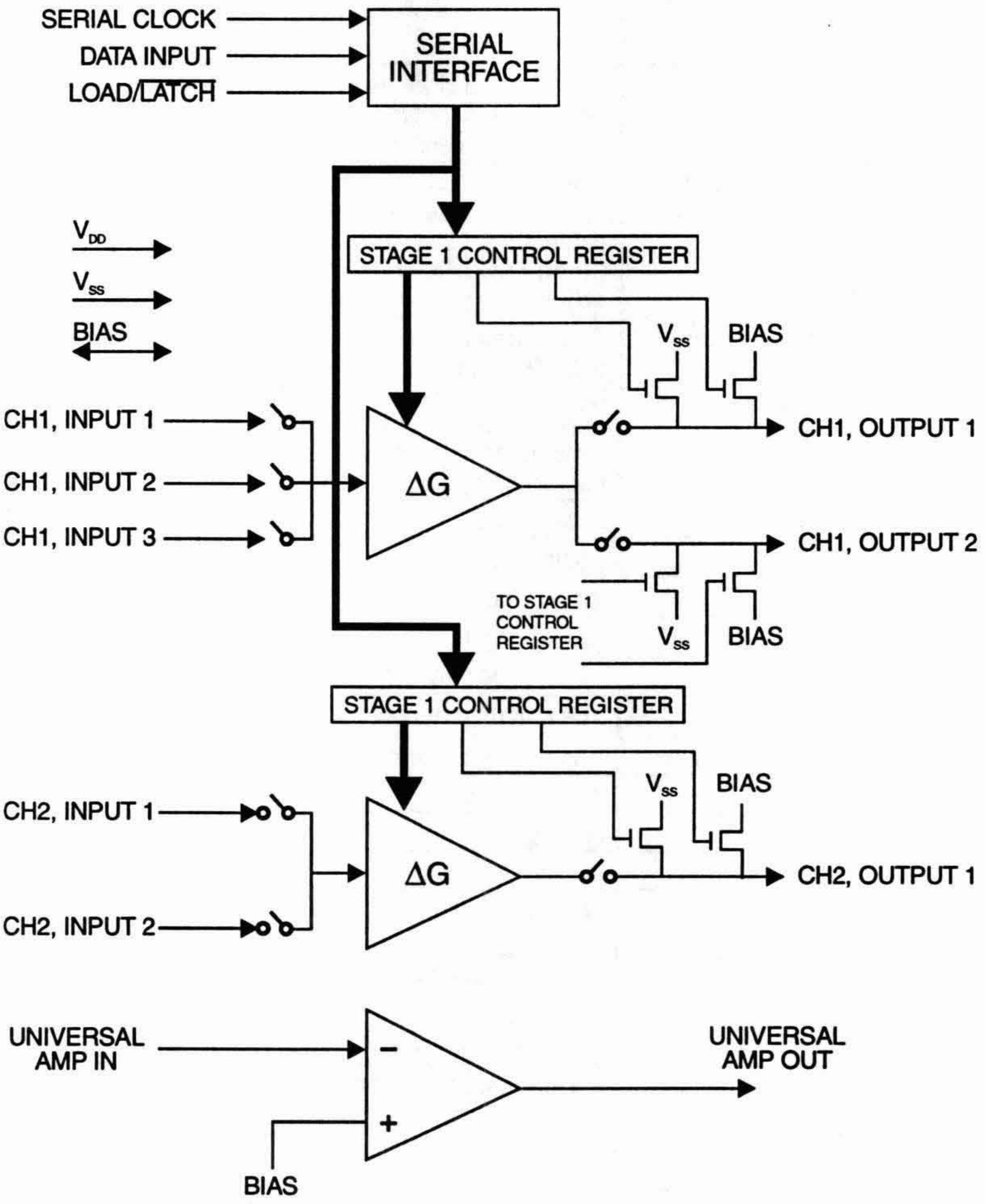
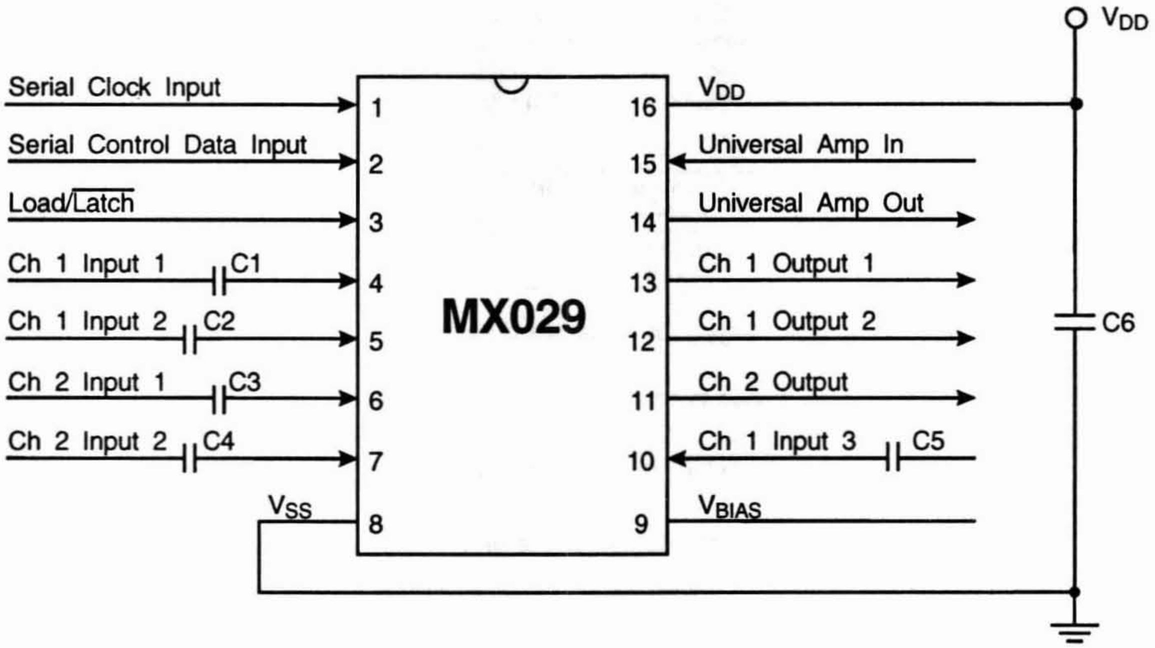

SERIAL CLOCK
DATA INPUT
LOAD/$\overline{\text{LATCH}}$
SERIAL INTERFACE
V_{DD}
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH1, INPUT 1
CH1, INPUT 2
CH1, INPUT 3
ΔG
CH1, OUTPUT 1
CH1, OUTPUT 2
TO STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH2, INPUT 1
CH2, INPUT 2
ΔG
CH2, OUTPUT 1
UNIVERSAL AMP IN
−
+
BIAS
UNIVERSAL AMP OUT

Figure 1: Device Block Diagram

2. Signal List

Pin No.		Type	Description
J, DW	TN		
1	1	Serial Clock	This external clock input is used to "clock in" the Control Data. See Figure 4 for timing information. This input has an internal 1MΩ pullup resistor.
2	4	Control (Data)	Input: Operation of the two amplifier channels (Ch1 - Ch2) is controlled by the data entered serially at this pin. The data is entered (bit 13 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1-5 and Figure 3. This input has an internal 1MΩ pullup resistor.
3	5	Load/$\overline{\text{Latch}}$	This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 14 bits have been loaded this input should be strobed "1 - 0 -1" to latch the new data in. Data is executed on the rising edge of the strobe.
4	6	Ch 1 Input 1	Analog Input.
5	7	Ch 1 Input 2	Analog Input.
6	8	Ch 2 Input 1	Analog Input.
7	9	Ch 2 Input 2	Analog Input.
8	12	V_{SS}	Negative supply (GND).
9	13	V_{BIAS}	The output of the on-chip bias circuitry, held at $V_{DD}/2$.
10	16	Ch 1 Input 3	Analog Input. Normally used for FSK data.
11	17	Ch 2 Output	Analog Output.
12	18	Ch 1 Output	Analog Output.
13	20	Ch 1 Output	Analog Output.
14	21	Universal Amp Out	Output from general purpose amplifier.
15	23	Universal Amp In	Inverting input to general purpose amplifier.
16	24	V_{DD}	Positive supply rail. A single +5-volt power supply is required.
	2, 3, 10, 11,14, 15, 19, 22	N/C	No internal connection

3. External Components


VDD
Serial Clock Input
Serial Control Data Input
Load/Latch
Ch 1 Input 1
Ch 1 Input 2
Ch 2 Input 1
Ch 2 Input 2
C1
C2
C3
C4
VSS
MX029
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VDD
Universal Amp In
Universal Amp Out
Ch 1 Output 1
Ch 1 Output 2
Ch 2 Output
Ch 1 Input 3
C5
VBIAS
C6

C1 to C5	Note 1	0.1µF	±20%
C6		1.0µF	±20%

Notes:

1. Analog input capacitors C1 to C5 are only required for a.c. input signals; d.c. input signals do not require these components.

Figure 2: Recommended External Components

4. Application

4.1 Recommendations

To avoid noise and instability the following practices are recommended:

1. Use a clean, well-regulated power supply.
2. Keep leads short.
3. Inputs and outputs should be shielded wherever possible.
4. Analog tracks should not run parallel to digital tracks.
5. A "Ground Plane" connected to Vss will assist in eliminating external pick-up on the channel input and output pins.
6. Avoid running High Level Outputs adjacent to Low Level Inputs.

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5. Control Data and Timing

The gain and I/O signal path for each section (Channels 1 and 2) is set individually by a 14-bit data word (D0 to D13). Data is loaded on the rising edge of the Serial Clock. Loaded data is executed on the rising edge of the Load/Latch pulse. The 14-bit word consists of 1 channel address bit (D7) for selection of the channel to be programmed, 6 bits for setting the gain/attenuation level (D8-D13), 3 bits for input selection (D4 and D6), and 4 bits for output settings (D0-D3). This format is illustrated in Figure 3.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ΔG SET	ΔG SET	ΔG SET	ΔG SET	ΔG SET	ΔG SET	CHAN ADDR	IN SEL	IN SEL	IN SEL	OUT SET	OUT SET	OUT SET	OUT SET
GAIN/ATTN LEVEL						CHANNEL ADDRESS	INPUT SELECT			OUTPUT SETTINGS			

Figure 3: Data Word Format

Tables 1-5 show how the data word is used to control channel selection, gain/attenuation, input selection and output settings, respectively.

To calculate the data word used to control channel gain/attenuation use the following formula:

$$25+\left(\frac{\text{gain dB}}{2}\right)=\text{The decimal equivalent of binary Data Word}$$

For example: using a gain of +34dB,

$$25+\left(\frac{+34\text{dB}}{2}\right)=42=\$2A=\frac{\text{D13-D8}}{101010}$$

D13	D12	D11	D10	D9	D8	GAIN SET (dB)
0	0	0	0	0	0	MUTE
0	0	0	0	0	1	-48
0	0	0	0	1	0	-46
0	0	0	0	1	1	-44
0	1	1	0	0	1	0
1	0	1	1	1	0	+42
1	0	1	1	1	1	+44
1	1	0	0	0	0	+46
1	1	0	0	0	1	+48
1	1	0	0	1	0	+48
1	1	0	0	1	1	+48

Table 1: Gain/Attenuation Level

D7	Channel Selected
0	1
1	2

Table 2: Channel Selection

D6	D5	D4	INPUTS SELECTED
0	0	0	NONE
0	0	1	1
0	1	0	2
0	1	1	1 & 2
1	0	0	3
1	0	1	1 & 3
1	1	0	2 & 3
1	1	1	1, 2, & 3

Table 3: Input Select

D3	D2	OUTPUT 2 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	V_{SS}
1	1	V_{BIAS}

Table 4: Settings for Output 2 (Ch 1 only)

D1	D0	OUTPUT 1 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	V_{SS}
1	1	V_{BIAS}

Table 5: Settings for Output 1

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD}-V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	(V_{DD} + 0.3)	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	
Any other pin	-20	20	mA
Total Allowable Power Dissipation at T_{AMB} 25°C		800	mW Max.
Derating above T_{AMB} 25°C		10	mW/°C above T_{AMB} 25°C
Operating temperature	-40	85	°C
Storage temperature	-55	125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	4.5	5.0	5.5	V
Operating temperature	-40		85	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 5.0V$, $T_{AMB} = 25°C$
Audio level 0dB ref. = $775mV_{RMS}$

	Notes	Min.	Typ.	Max	Units
Current:					
All Stages Operating			3.0		mA
Digital Inputs					
Input Logic "1"		3.5			V
Input Logic "0"				1.5	V
Digital Input Impedance		0.5	1.0		MΩ
Gain Control Amplifier Stages					
Bandwidth (-3dB)	1	3.3			kHz
Output Impedance			1.0	2.0	kΩ
Total Harmonic Distortion	2, 4		0.35	0.5	%
Interstage Isolation			60.0		dB
Gain/Attenuation		46	48		dB
Gain/Attenuation Steps (48 total)			2.0		dB
Step Error				0.4	dB
Input Impedance		50.0			kΩ
Input Referred Offset Voltage (V_{IOS})			10		mV
Universal Amplifier					
Bandwidth (-3dB)	3	10			kHz
Output Impedance			1.0	2.0	kΩ
Total Harmonic Distortion	3		0.35	0.5	%
Open Loop DC Gain			60		dB

Notes:

1. Gain set to maximum (+48 dB)
2. Gain Set 0dB. Input Level 1kHz -3.0dB ($549mV_{rms}$)
3. Gain externally set to 10 dB.
4. With a 100k load on the output.

6.2 Serial Interface Timing

	Parameter	Min.	Typ.	Max.	Units
t_{PWH}	Serial Clock "High" Pulse Width	250			ns
t_{PWL}	Serial Clock "Low" Pulse Width	250			ns
t_{DS}	Data Set-up Time	150			ns
t_{DH}	Data Hold Time	50			ns
t_{LLO}	Load/Latch Over Time			0	ns
t_{LLD}	Load/Latch Delay	200			ns
t_{LLW}	Load/Latch Pulse Width	150			ns
	Serial Data Clock Frequency			2.0	MHz

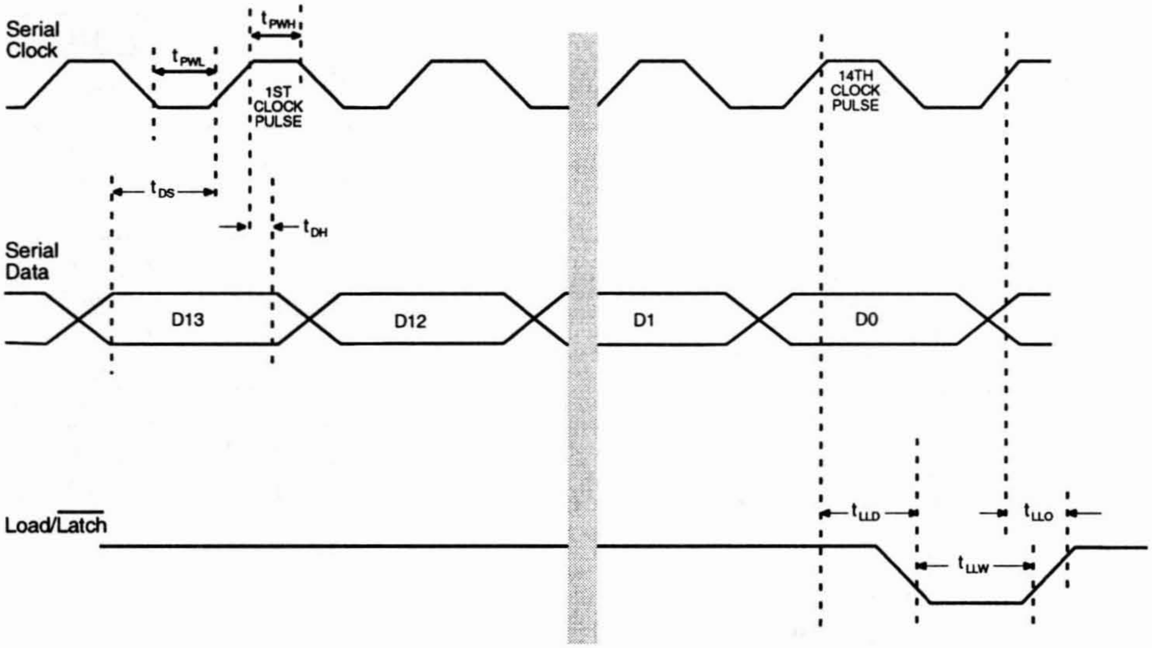
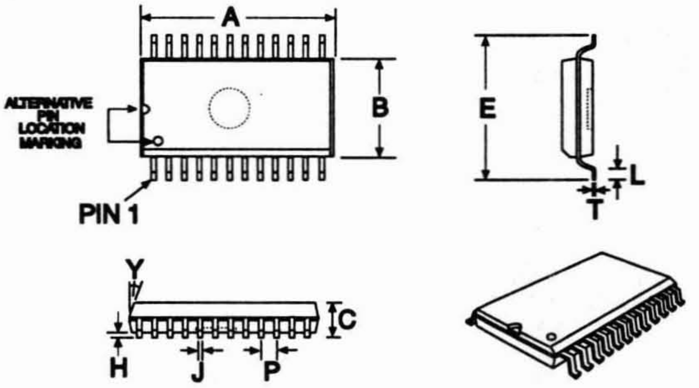

Serial Clock
t PWH
t PWL
1ST CLOCK PULSE
14TH CLOCK PULSE
t DS
t DH
Serial Data
D13
D12
D1
D0
Load/Latch
t LLD
t LLO
t LLW

Figure 4: Serial Timing Diagram

6.3 Packaging

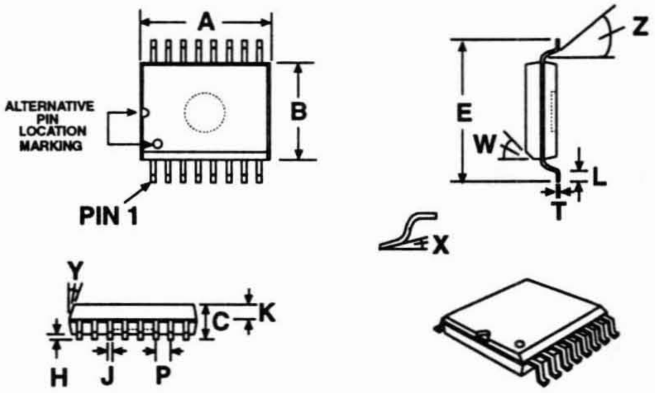

A
B
E
L
T
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin TSSOP Mechanical Outline: Order as part no. MX029TN

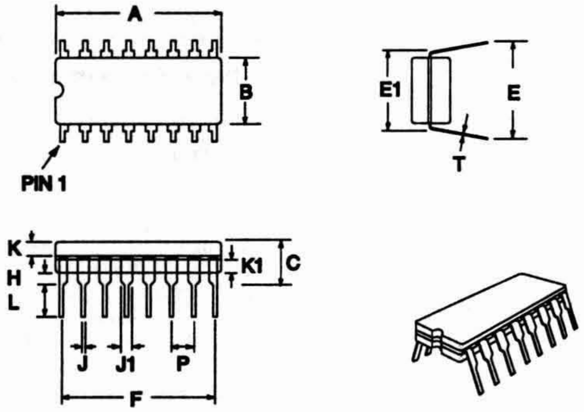

A
B
E
Z
W
L
T
X
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
K
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: Order as part no. MX029DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin CDIP Mechanical Outline: Order as part no. MX029J

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX102

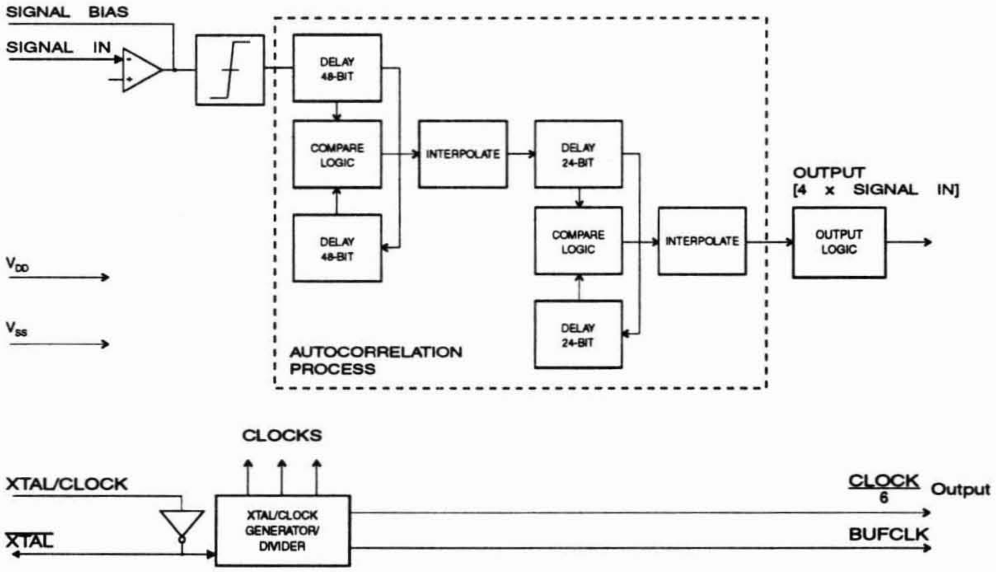
Autocorrelating Signal Processor

Features

- **Low Signal Level Input of 10mVrms**
- **Wide Signal Frequency Range from 17Hz to 13kHz**
- **On-Chip Gain Amplifier**
- **Digital Output Signal (f_{IN} x 4)**
- **Divided-Down Clock Output**
- **Low Supply Voltage Operation of 2.5 V**
- **Low Current Drain**

Applications

- **Medical Instruments**
- **Sonar Detection**
- **Remote Signaling**
- **Pagers**
- **Mobile Radio**
- **Slow Data Rate Communication**
- **Tone Detection**


SIGNAL BIAS
SIGNAL IN
DELAY 48-BIT
COMPARE LOGIC
DELAY 48-BIT
INTERPOLATE
DELAY 24-BIT
COMPARE LOGIC
DELAY 24-BIT
INTERPOLATE
OUTPUT [4 x SIGNAL IN]
OUTPUT LOGIC
V$_{DD}$
V$_{SS}$
AUTOCORRELATION PROCESS
CLOCKS
XTAL/CLOCK
XTAL
XTAL/CLOCK GENERATOR/ DIVIDER
CLOCK/6 Output
BUFCLK

The MX102 is a single-chip device to extract single periodic signals from very high random-noise environments.

Using patented autocorrelation techniques the MX102 will enhance the input signal's signal-to-noise ratio by as much as 8.5dB and provide a digital output signal centered at four times (x4) the input frequency.

The amplitude of non-periodic components of the signal is substantially reduced. The patented autocorrelator compares the incoming signal to itself; the more elements of the waveform that are seen as periodic, the higher the energy at the microcircuit output.

The MX102 cascades two autocorrelators, each one improving the signal-to-noise ratio

With a random noise input the output will swing rail-to-rail at random (peak-limited). The input/output signal delay is fixed by the choice of clock frequency and the length of the internal register. The MX102 will operate at supply voltages of between 2.5 volts and 5.5 volts and with Xtal/clock frequencies from 20kHz to 2.5MHz. Using various Xtal/clock inputs th device can be set to accept input signal frequencies, in bands, from 17.0Hz to 13.0kHz.

Two uncommitted clock outputs are available: one to supply a 'divided-down' Xtal/clock frequencies and the second is a buffered output for use in external and peripheral functions.

This MX102 is available in the following package styles: 16-pin SOIC (MX102DW) and 16-pin CDIP (MX102J).

CONTENTS

Section **Page**

1. **Block Diagram** .... **3 - 179**

2. **Signal List** .... **3 - 180**

3. **External Components** .... **3 - 181**

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   4.2 Input Frequency Range .... 3 - 182

5. **Performance Specification** .... **3 - 184**
   5.1 Electrical Performance .... 3 - 184
   5.2 Packaging .... 3 - 186

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

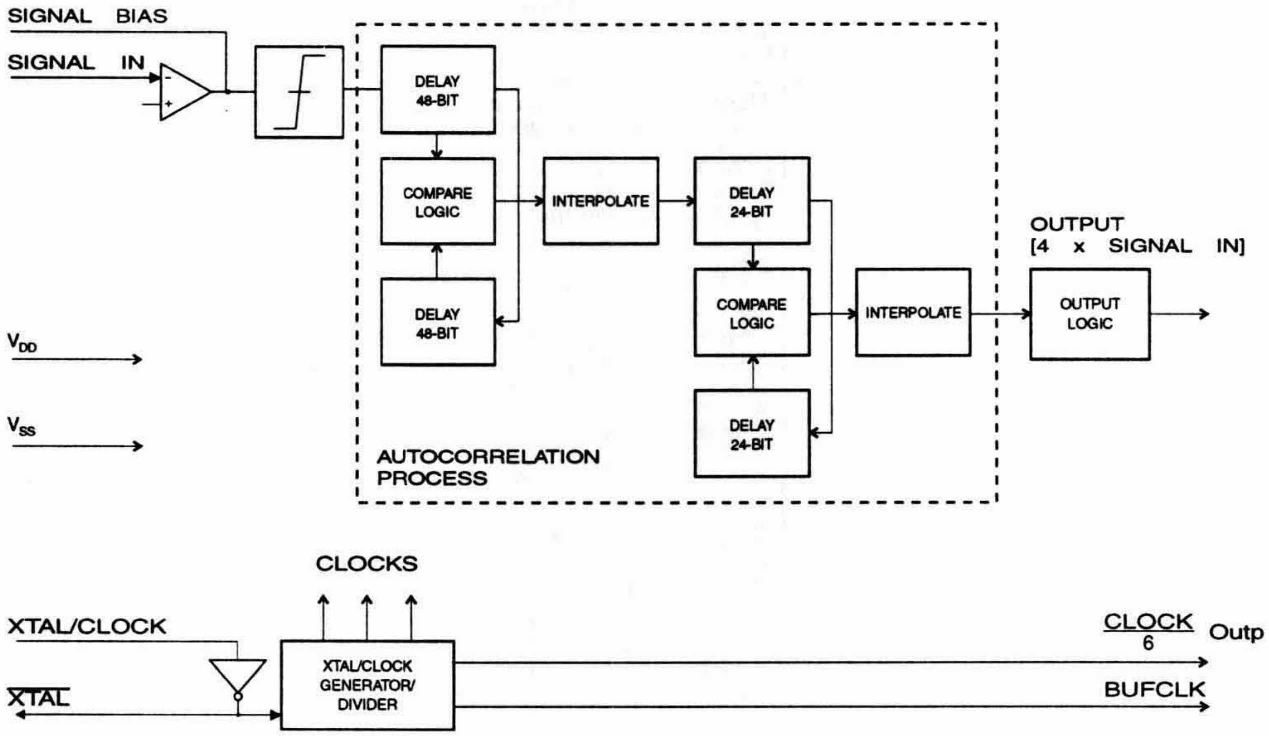

SIGNAL BIAS
SIGNAL IN
DELAY 48-BIT
COMPARE LOGIC
DELAY 48-BIT
INTERPOLATE
DELAY 24-BIT
COMPARE LOGIC
DELAY 24-BIT
INTERPOLATE
OUTPUT [4 x SIGNAL IN]
OUTPUT LOGIC
V_{DD}
V_{SS}
AUTOCORRELATION PROCESS
CLOCKS
XTAL/CLOCK
$\overline{XTAL}$
XTAL/CLOCK GENERATOR/ DIVIDER
$\frac{CLOCK}{6}$ Outp
BUFCLK

Figure 1: Device Block Diagram

2. Signal List

Packages	Signal		Description
DW/J	Name	Type	
1	Signal In	input	The inverting input to the analog amplifier/comparator. Used with the Signal Bias pin; external coupling components are required. See Figure 2
3	Signal Bias	output	The output of the analogue amplifier/comparator. Do not load this pin with peripheral circuitry; there is no drive capacity for off-chip signaling. The feedback resistor should be not less than 200kΩ. See Figure 2.
4	V_{DD}	power	Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; this input is positioned to prevent cross-talk, either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin.
5	BUFCLK	output	Buffered inverter oscillator digital output. May be used as test point to align clock frequency or to drive other circuitry.
6	$\overline{\text{XTAL}}$	output	The output of the on-chip clock oscillator inverter.
8	Xtal/Clock	input	The input to the on-chip clock oscillator inverter; this may be a Xtal, resonator or clock pulse input. The selection of this frequency will affect the operational input signal bandwidth (and output frequency) of this device; refer to Table 4. Note that the choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency. Operation of this microcircuit without an active Xtal or clock input may cause device damage. A clock pulse input is fed directly into this pin; Xtal/clock components are not required. See Table 2.
9	V_{SS}	power	Negative Supply
11	CLK ÷ 6	output	A squarewave output clock signal at the rate of Clock/6; provided for peripheral and test purposes.
13	OUTPUT	output	(fOUT = 4 x fSIGNAL IN). The auto-correlated output signal at four times (x 4) the input signal (see Figure 3). There is a time delay between input and output signals (see Specifications).
16	V_{DD}	power	Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin. The choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency (see Figure 4).
2, 7, 10, 12, 14, 15		N/C	No internal connection. Leave open circuit

Table 1: Signal List

V_{DD} (V)	Max. Xtal/Clock Freq. (MHz)
2.5	0.625
3.0	1.0
5.0	2.5

Table 2: Maximum Usable Xtal/Clock Frequencies

3. External Components

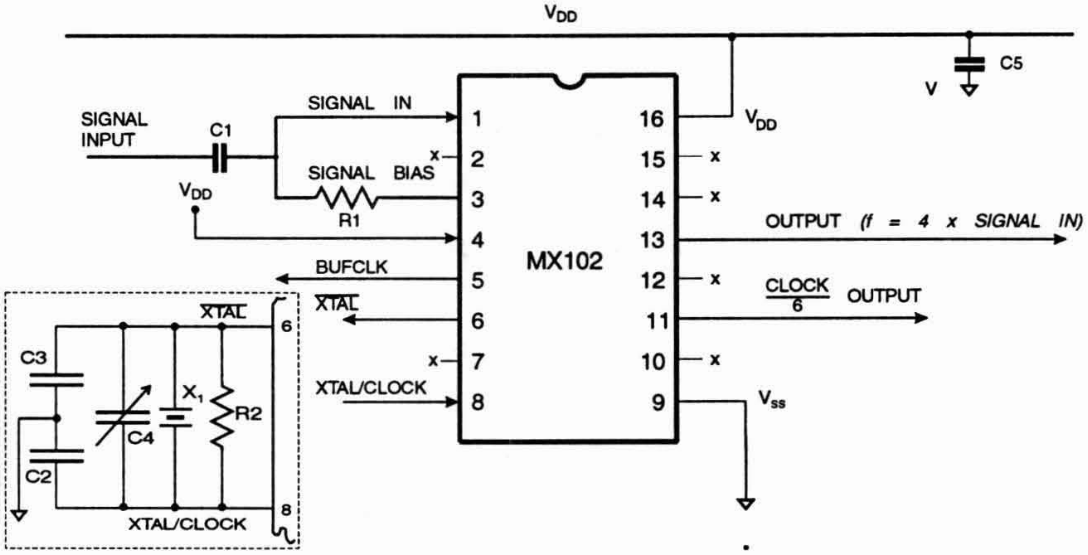

V_{DD}
C5
V
SIGNAL INPUT
C1
SIGNAL IN
SIGNAL BIAS
R1
V_{DD}
BUFCLK
XTAL
XTAL/CLOCK
x
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MX102
V_{DD}
OUTPUT (f = 4 x SIGNAL IN)
CLOCK/6 OUTPUT
V_{ss}
C3
C2
C4
X₁
R2
XTAL
XTAL/CLOCK
6
8

Figure 2: Recommended External Components

R1		2.2MΩ
R2		1.0MΩ
C1		0.01µF
C2	Note 1	47.0pF -see below
C3	Note 1	47.0pF -see below
C4	Note 2	5 - 65pF -see below
C5		1.0µF
X1		560kHz resonator
X1 range		20kHz to 2.5MHz

Table 3: Recommended External Components

Recommended External Component Notes:

1. Values of capacitors C2 and C3 should be reduced for higher Xtal frequencies and/or lower supply voltages (V_{DD}).
2. C4 is suggested for frequency setting when using a resonator; when a Xtal is used C4 is omitted.

4. General Description

4.1 Signal

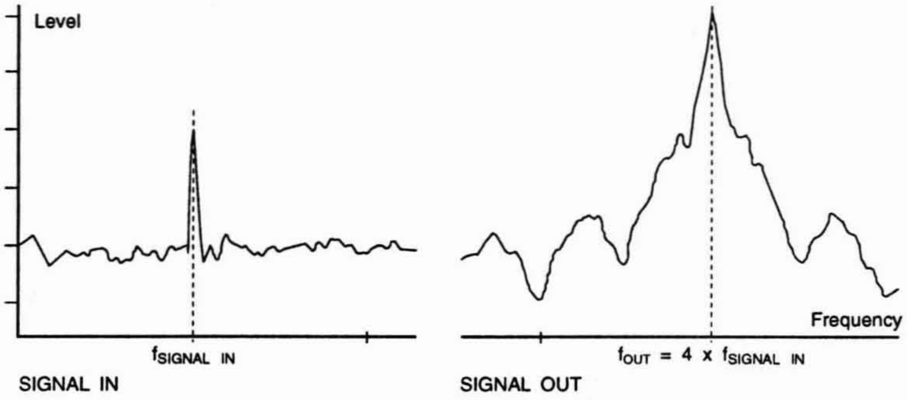


Figure 3: MX102 Input/Output Relationships

Note:

1. The frequency of the output signal is four times (x4) that of the input signal.

4.2 Input Frequency Range

The MX102 has a wide frequency range, but care must be taken to choose the Xtal frequency appropriate for your application.

Xtal/Clock Frequency (kHz)	Input Freq. (Hz)		BW (Hz)
	Min.	Max.	
20	17	105	88
100	88	526	443
200	166	1052	886
300	250	1579	1329
400	333	2105	1772
500	416	2632	2216
560	467	2947	2480
600	500	3158	2658
700	583	3684	3101
800	667	4210	3543
900	750	4737	3987
1000	833	5263	4430
2000	1667	10526	8859
2500	2083	13157	11074

Table 4: Input Signal Ranges vs Xtal/Clock Frequency

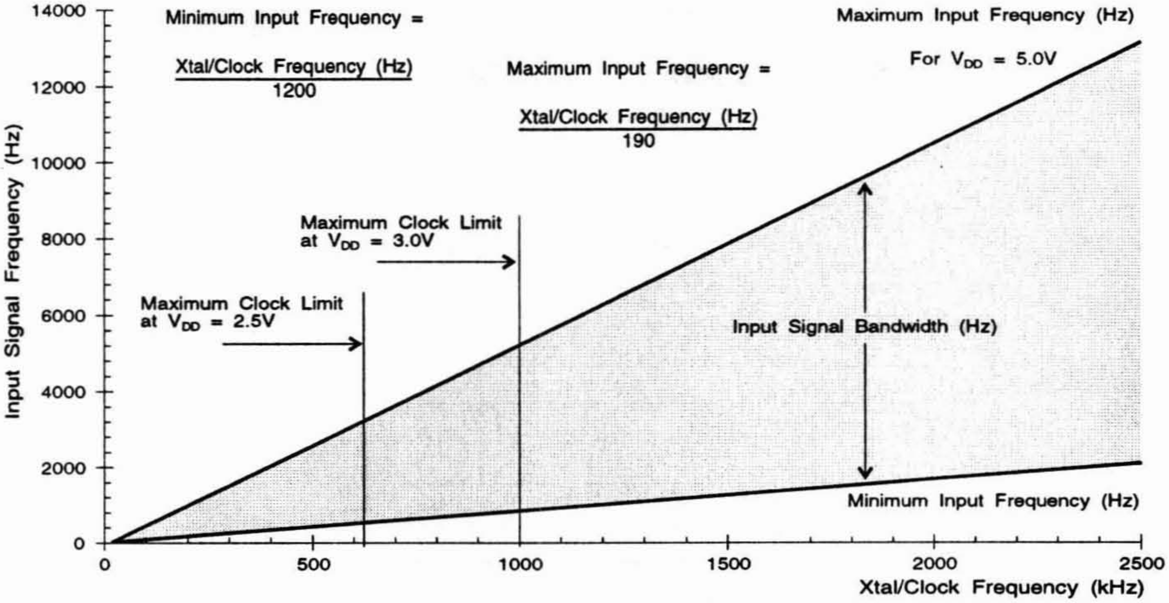


Figure 4: Input Signal Ranges vs Xtal/Clock Frequency

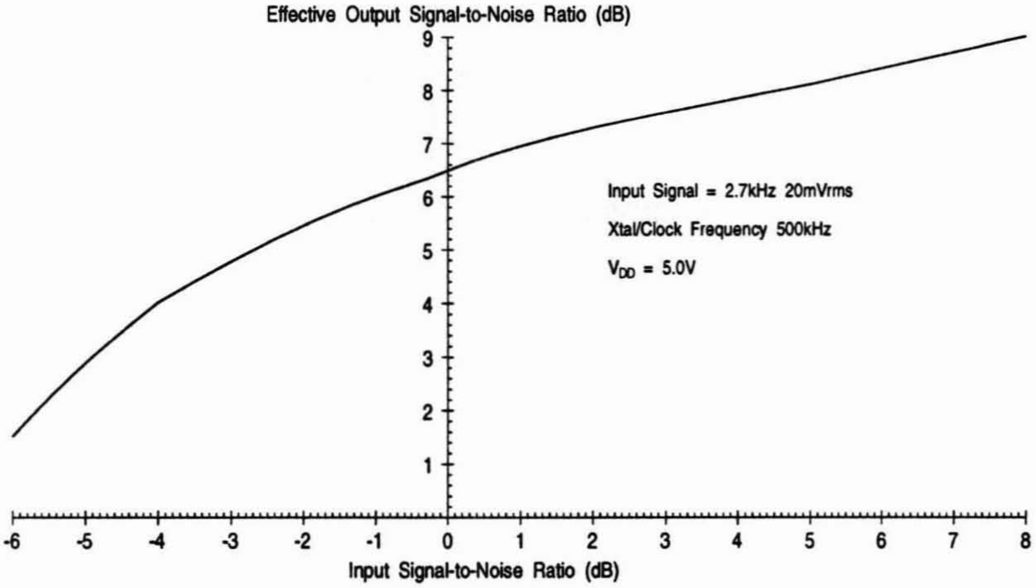


Figure 5: Enhancement of Signal-To-Noise Ratio

Note:

1. The graph shown in Figure 5 illustrates the signal-to-noise enhancement that can be obtained, under varying input conditions, from the MX102.

5. Performance Specification

5.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0 volts	V
Input Voltage at any pin	-0.3	(V_{DD}+0.3 volts)	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
Maximum Device Dissipation	100		mW
Operating Temperature	-40°	85	°C
Storage Temperature	-40°	125	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	2.5	3.3/5.0	5.5	V
Xtal/Clock	20		2500	kHz
Operating Temperature	-40		85	°C

Operating Characteristics

For the following conditions unless otherwise specified:

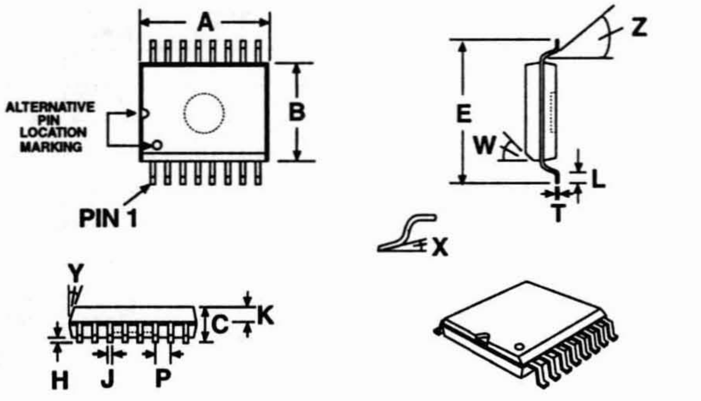
$V_{DD} = 5.0V$, $T_{AMB} = 25°C$
Xtal/Clock = 560kHz, Input Test Signal = $200mV_{RMS}$

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current		-	1.0	2.5	mA
	2	-	4.0	-	mA
Logic '1' Level		80%	-	-	V
Logic '0' Level		-	-	20%	V
Digital Output Impedance		-	4.0	10.0	kΩ
Dynamic Values					
Signal Input	3	20.0	-	1000	mV_{RMS}
Analog (Input) Amplifier Gain	4	20.0	-	-	dB
	5	9.0	-	-	dB
	6	10.0	-	-	dB
Recommended Input Signal Duty Cycle Ratio		35	50	-	%
Frequency Out/Frequency In Ratio		4.0	-	4.0	%
Maximum Xtal/Clock Frequency	1	2.5	-	-	MHz
Minimum Xtal/Clock Frequency				20.0	kHz
Frequency Input Range					
Xtal/Clock = 560kHz	7	500	-	3000	Hz
Table 4		1/1200		1/190	Xtal/Clock
Input to Output Delay	8	-	1.4		ms
Output resolution		-	1/6	-	Xtal/Clock

Operating Characteristics Notes:

1. Maximum Xtal/clock frquency allowed varies with applied supply voltage (V_{DD}).
2. I_{DD} requirement for Xtal/clock frequency of 2.24MHz.
3. Signal input level required to provide a constant autocorrelated output.
4. Measured with a 6.0kHz sinewave at the signal input.
5. Measured with V_{DD} = 2.5 volts.
6. Measured with a 12kHz input signal.
7. Recommended input signal frequency range to correlation circuits.
8. Input (Signal In) to output (Output) time with a 2.24MHz Xtal/clock input.

5.2 Packaging

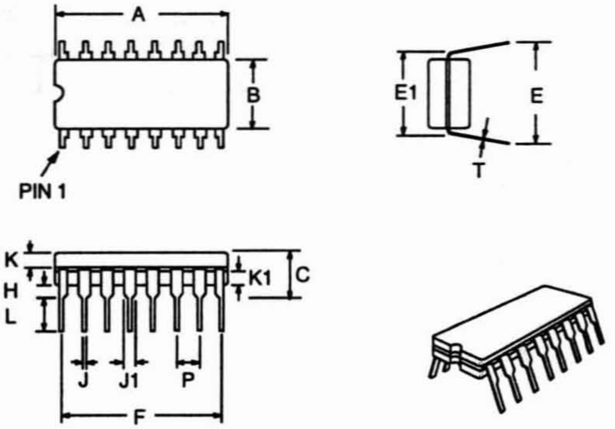


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: ***Order as part no. MX102DW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin CDIP Mechanical Outline: ***Order as part no. MX102J***

MX•COM, INC. MiXed Signal ICs

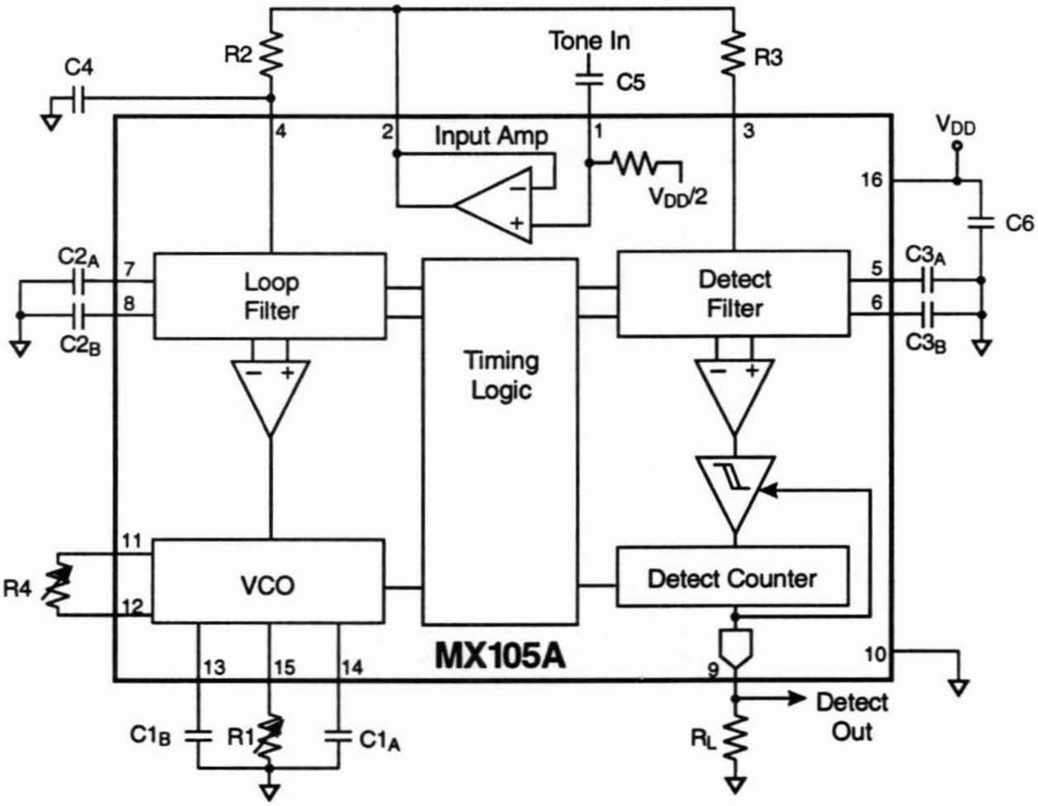
DATA BULLETIN

MX105A Tone Detector

PRELIMINARY INFORMATION

- **FEATURES**
- **Operates in High Noise Conditions**
- **≥36 dB Signal Input Range**
- **High Sensitivity**
- **Low Power Operation 2.7 V to 5.5 V**
- **Adjustable Bandwidth**
- **Adjustable Frequency**

- **APPLICATIONS**
- **Single and Multitone System Applications**


Tone In
C4
R2
R3
C5
4
2
Input Amp
1
3
VDD/2
VDD
16
C6
C2A
7
8
C2B
Loop Filter
Timing Logic
Detect Filter
5
6
C3A
C3B
11
R4
12
VCO
Detect Counter
13
15
14
MX105A
9
10
C1B
R1
C1A
RL
Detect Out

The MX105A is a monolithic CMOS tone detector for tone decoding in single and multitone signaling systems. Using phase locked loop (PLL) decoding techniques, the MX105A recognizes tones in the presence of high noise levels and strong adjacent channel tones. Detection frequency and bandwidth can each be independently adjusted. The design is immune to high levels of harmonic and sub-harmonic noise. It also maintains excellent noise immunity and constant bandwidth over a wide range of input signal levels.

The MX105A requires a voltage supply of 2.7V to 5.5V and is available in the following package styles: 16-pin SOIC (MX105ADW), 16-pin PDIP (MX105AP), and 24-pin PLCC (MX105ALH).

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

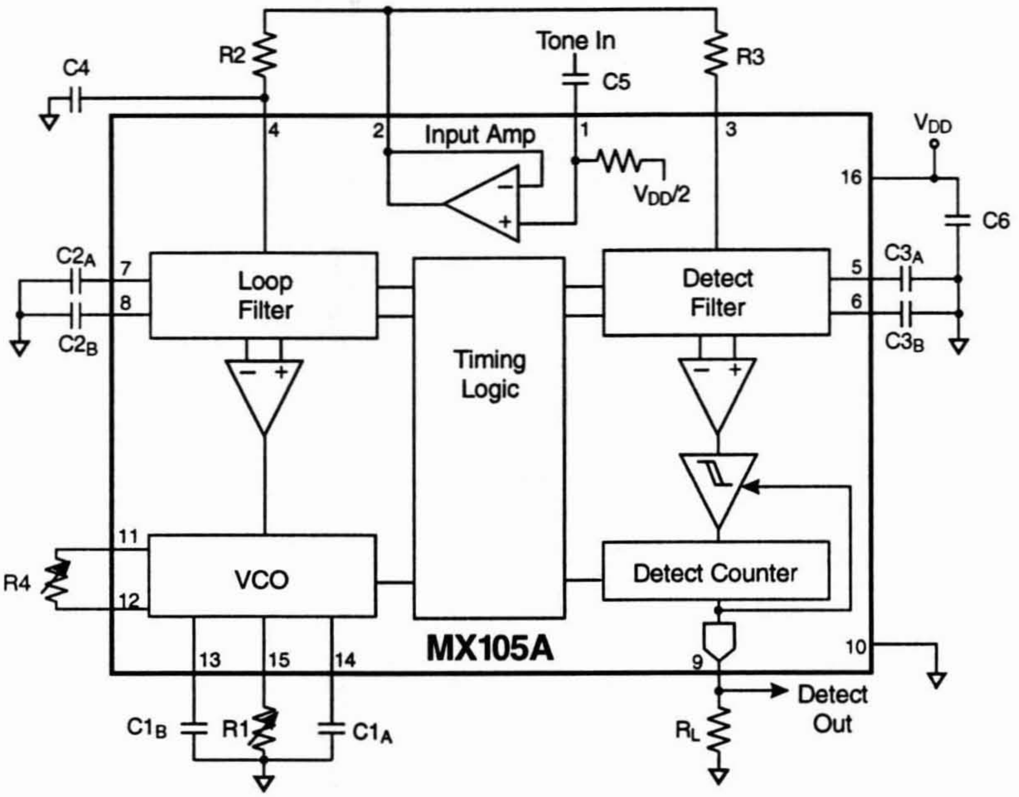

C4
R2
Tone In
C5
R3
VDD
4
2
Input Amp
1
3
VDD/2
16
C6
C2A
7
8
C2B
Loop Filter
Timing Logic
Detect Filter
5
6
C3A
C3B
11
12
R4
VCO
Detect Counter
MX105A
13
15
14
9
10
C1B
R1
C1A
RL
Detect Out

Figure 1: Block Diagram

2. Signal List

Pin No.	Pin No.	Name	Type	Description
DW/P	LH			
1	1	INPUT AMP IN	input	AC couple to this input. Nominal input impedance is 200 kΩ.
2	3	INPUT AMP OUT	output	Nominal output impedance is 1 kΩ.
3	5	R3	input	Detect filter resistor pin.
4	6	R2	input	PLL loop filter resistor pin. For improved performance C4 may be chosen to provide 30° of phase shift at the loop filter input.
5	7	$C3_A$	output	Detect filter capacitor pin A
6	8	$C3_B$	output	Detect filter capacitor pin B
7	10	$C2_A$	output	Loop filter capacitor pin A
8	11	$C2_B$	output	Loop filter capacitor pin B
9	13	DETECT OUT	output	PMOS open drain output - active on detect.
10	14	V_{SS}	power	Ground.
11	16	$R4_A$	input	Bandwidth control resistor pin A
12	17	$R4_B$	input	Bandwidth control resistor pin B
13	19	$C1_B$	output	VCO capacitor B
14	20	$C1_A$	output	VCO capacitor A
15	22	R1	input	VCO discharge resistor. When potentiometer tuning is required, a series resistor is recommend to prevent possible shorting to ground.
16	24	V_{DD}	power	Power supply.

3. External Components

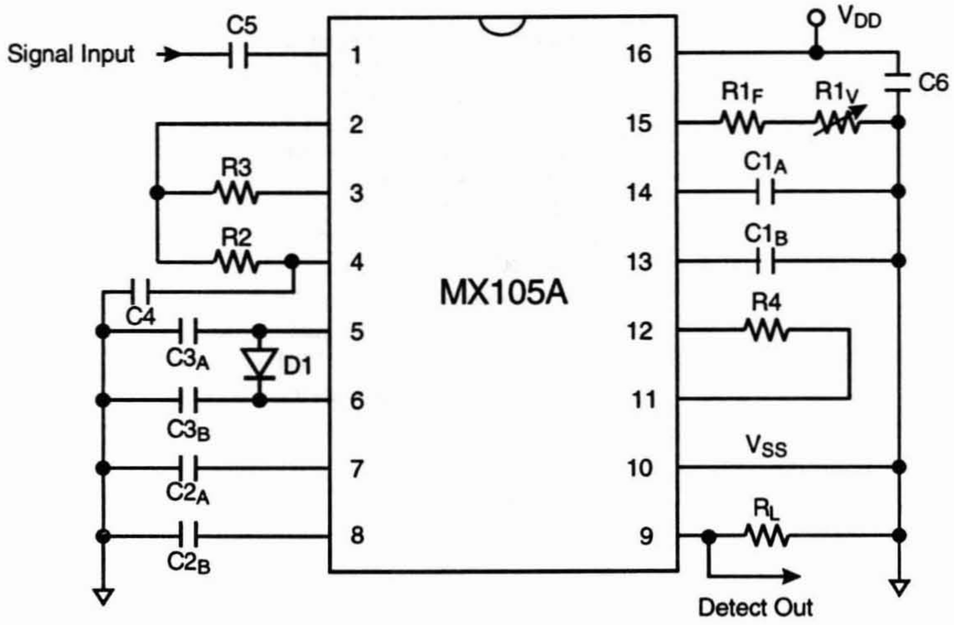

C5
Signal Input
1
2
3
4
5
6
7
8
R3
R2
C4
C3A
D1
C3B
C2A
C2B
MX105A
16
15
14
13
12
11
10
9
VDD
R1F
R1V
C6
C1A
C1B
R4
VSS
RL
Detect Out

Figure 2: Recommended External Components

$R1_F$	See Section 5.2	300kΩ	
$R1_V$	See Section 5.2	100kΩ	
R2	See Section 5.6		
R3	See Section 5.8		
R4	See Section 5.5		
R_L	Note 4	20kΩ	±20%
$C1_A$	See Section 5.2 Note 2		
$C1_B$	See Section 5.2 Note 2		

$C2_A$	See section 5.6 Note 2		
$C2_B$	See Section 5.6 Note 2		
$C3_A$	See Section 5.8 Note 2		
$C3_B$	See Section 5.8 Note 2		
C4	See Section 5.11 Note 1, 2		
C5		0.27µF	±20%
C6		0.1µF	±20%
D1	See Section 5.9 Note 3	small signal diode (1N914)	

External Components Notes:

1. For improved performance, C4 may be chosen to provide 30° phase shift at the VCO loop filter input.
2. For compatibility with the MX105; capacitors (C1 - C4) may be connected to V_{DD} instead of V_{SS}.
3. For improved de-response time, a diode (D1) may be added.
4. Any value load resistance (R_L) may be used, providing the maximum load current does not exceed the value in 'Maximum Ratings Specifications'.

4. General Description

The MX105A implements a frequency detector with a phase locked loop (PLL) and a lock detector. The voltage controlled oscillator (VCO) center frequency, detection bandwidth, loop filter, and detect filter are all independently controlled by external components.

The MX105A provides a pair of pseudo-sinewave multipliers for splitting the input signal into approximately orthogonal components. These multipliers are implemented with commutating filters (cyclically sampling filters) which translate an in band AC input signal to DC. The commutating loop filter is used as the phase detector of the PLL while the commutating detect filter provides for lock detection. Each pseudo-sinewave has a cyclic form (1 1 0 -1 -1 0) to eliminate low order harmonic responses. The loop filter produces an error signal, which when applied to the VCO input allows frequency locking. A limiter between the loop filter output and the VCO input provides tunable control of the detection bandwidth (BW). Once lock is achieved the detect filter produces a DC value proportional to the input tone amplitude. An internally generated reference is compared to the detect filter output to determine whether the PLL is locked to an input tone. Once lock is determined the internal reference is reduced by 50% to minimize output chatter with marginal input signals.

The sampling clocks of the detect filter lag those of the loop filter by 60°. To improve performance, a capacitor (C4) can be used to phase shift the input to the loop filter by 30°. This shifts all sampling clocks an additional 30° relative to the input tone to phase align the detect filter sampling clocks with the amplitude peaks of the input tone.

Figure 3 shows the sampling clocks relative to an in band input tone; this figure represents the steady state 'locked' condition without C4.

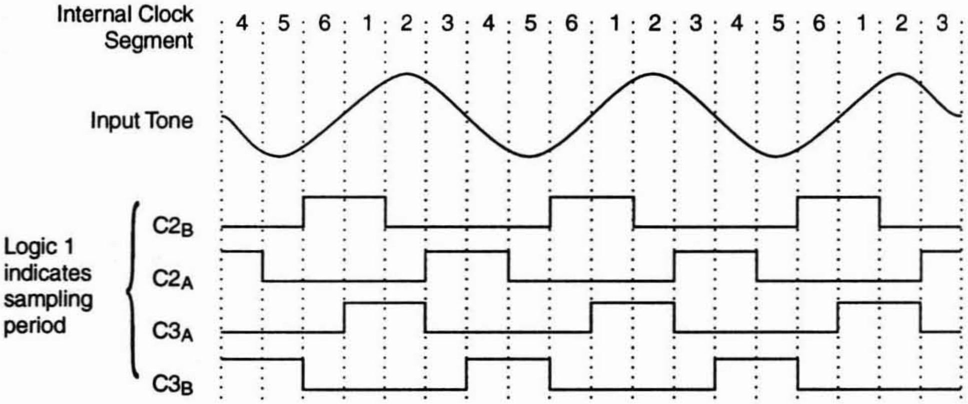


Figure 3: Sampling Clocks of Commutating Filters

5. Application

The external components shown in Figure 2 are used to adjust the various performance parameters of the MX105A. The signal-to-noise performance, response time and signal bandwidth are all interrelated factors which should be optimized to meet the requirements of the application.

By selecting component values in accordance with the following formulas, optimum circuit performance is obtained for any given application.

First define the following application parameters:

A. The center frequency to be detected (f_0).

B. The MX105A Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the MX105A f_0 due to supply voltage and any temperature effect of the MX105A and its supporting components.

C. The maximum permissible MX105A response time.

D. The minimum input signal amplitude.

Note: Using this information the appropriate component values can be calculated, and the signal-to-noise performance can be read from a chart. Do not add large safety margins for response time and minimum signal amplitude; reasonable margins are already included in the formulas. Excessive margins may result in reduced noise immunity.

5.1 Method for Calculating External Component Values

The examples on the following pages demonstrate the calculation of component values for any given application. For the purpose of the examples, the values below are used:

A. $f_0 = 2800$ Hz

B. $\Delta TEMP = 100\ ^\circ C$, $\Delta V_{DD} = 1V$, $\Delta f_{IN} = 0.5\%$

C. Maximum allowed response time = 50ms

D. Minimum input signal amplitude = 200 mV_{RMS}.

5.2 Define f_0

The components R1, $C1_A$ and $C1_B$ set the free running frequency of the VCO and therefore the f_0 of the MX105A. As shown below, the frequency of 2800 Hz corresponds to a capacitor value of 220pF and a resistor value of 385 kΩ. This resistance can be achieved with a 300 kΩ fixed resistor for $R1_F$ and for $R1_V$ a 100 kΩ potentiometer. The capacitance of $C1_A$ and $C1_B$ should include 10-20pF parasitic capacitance due to the device and its package plus any board parasitic capacitance.

$$f_0 = \frac{1}{K \cdot R1(C1_A + C1_B)} \Rightarrow R1 \times C1_A = \frac{1}{2Kf_0}$$

$$\text{where: } K = 2.1 \pm 5\%$$

$$R1 = (R1_F + R1_V)$$

5.3 Calculate Minimum Usable Bandwidth

Minimum Usable Bandwidth (MUBW) is the TOTAL bandwidth required for the following:

A. Input signal frequency tolerance

B. MX105A f_0 temperature coefficient ($T_C = 100$ ppm/°C)

C. MX105A f_0 supply voltage coefficient ($V_C = 5000$ ppm/V)

Note: Add A, B and C and express as TOTAL bandwidth, not as a ± percentage (%) value.

$$MUBW = \Delta f_0 + T_C \Delta TEMP + V_C \Delta V$$

$$MUBW = 0.5 + 0.01 \times 100 + 0.5 \times 1 = 2\%$$

5.4 Calculate The Recommended Operating Bandwidth

$$BW = \frac{10 + MUBW}{2} = \frac{10 + 2}{2} = 6\%$$

5.5 Select R4 for Operating BW

$$R4 = \frac{4.8 \times BW}{10.35 - BW} = \frac{4.8 \times 6}{10.35 - 6} \approx 6.8\text{k}\Omega$$

The exact bandwidth given by any value of R4 will vary slightly. In applications where an exact bandwidth is required, R4 should be a variable resistor to permit adjustment.

5.6 Calculate R2×C2$_A$

$$R2 \times C2_A \approx \frac{100}{3 \times f_0 \times BW}$$

For a frequency of 2800 Hz, a bandwidth of 6%, and a choice of $C2_A = 0.01\mu F \Rightarrow R_V = 200k\Omega$.

Note: Use nearest preferred values.

5.7 Define Maximum Allowed Response Time

The maximum response time (T_{ON}) is the sum of the VCO lock time (T_{LOCK}) and the DETECT integration time (T_{DETECT}). The MX105A's T_{ON} must not exceed the maximum time allowed for the application, but a value lying near the maximum gives the best S/N performance.

A. Calculate T_{LOCK}

$$T_{LOCK} = \frac{150}{f_0 \times BW}$$

Using the formula above, for a frequency of 2800 Hz and a bandwidth of 6% the approximate Lock time (T_{LOCK}) will be 9 ms. Since the maximum response time is 50 ms, a DETECT time of 41 ms is allowed.

Note: T_{LOCK} may vary from near zero to the value given, causing corresponding variations in actual T_{ON}.

B. Calculate Maximum Allowable T_{DETECT}

$$T_{DETECT} = T_{ON_{MAX}} - T_{LOCK}$$

C. Define Minimum Expected Signal Amplitude $\left(V_{IN_{MIN}}\right)$

This is used in calculating T_{DETECT} components.

5.8 Calculate R3×C3$_A$

$$R3 \times C3_A \approx \frac{T_{DETECT}}{-3 \times \ln\left(1 - \frac{V_{TH}}{V_{IN_{MIN}}}\right)}$$

where: V_{TH} is the detect filter sensitivity.

Note:

1. For a signal amplitude of 200 mV$_{RMS}$, a resistor value R3 of 510 kΩ with a 0.1µF capacitor for C3$_A$ and C3$_B$ will yield a T_{DETECT} time of 20ms. This in turn yields a response time of 9ms + 20 ms = 29ms.
2. Use nearest preferred values.

5.9 Calculate Maximum De-response Time

$$T_{OFF} \approx -3 \times \ln\left(\frac{V_{TH}}{V_{IN_{MAX}}}\right) R3 \times C3_A$$

where: V_{TH} is the detect filter sensitivity.

For improved de-response time, a diode (1N914 or similar) can be placed between pins 5 and 6, as shown in Figure 3. The formula and figure below show the approximate time the MX105A will take to turn off after an in-band signal has been removed. The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300 mV_{RMS}. This graph is for $V_{DD} = 5V$; for lower V_{DD} KDT increases.

$$T_{OFF} \approx K_{DT} \times R3 \times C3_A$$

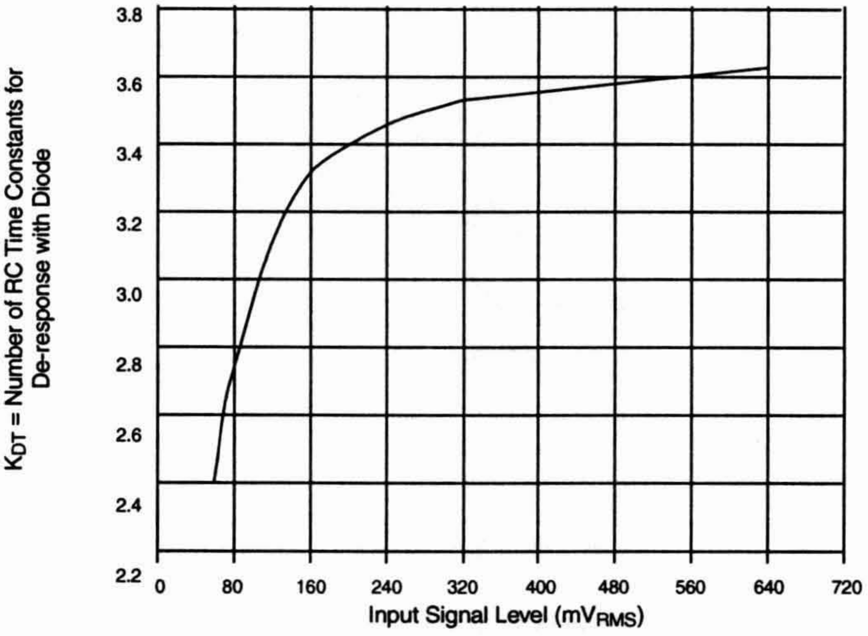


Figure 4: K_{DT} Factor for T_{OFF} vs. Signal Input Amplitude

5.10 Calculate Signal to Noise Performance

Worst-case S/N calculations depend on calculation of a value "M" using the formula shown below:

$$M = \frac{R3 \times C3_A}{3 \times R2 \times C2_A}$$

substituting example values,

$$M = \frac{510 \times 0.1}{3 \times 200 \times 0.01} = 8.5$$

By substituting this value for M in Figure 5, the minimum required S/N of an in band tone with respect to an adjacent interfering tone can be found. This then has to be increased depending on the input tone amplitude.

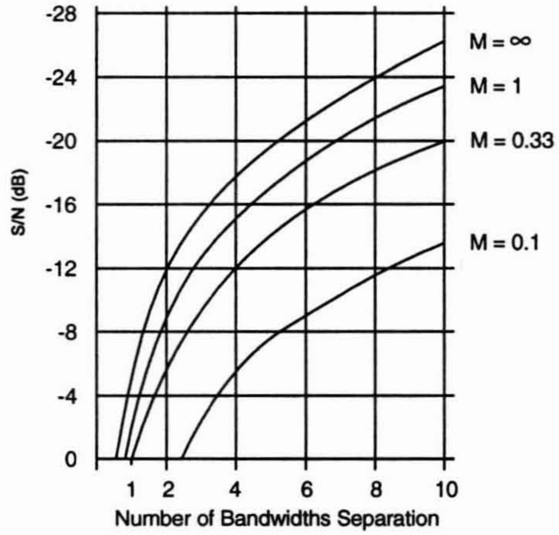


Figure 5: S/N vs. BW Separation

The following formula expresses the reduction in noise immunity as the input signal approaches the detect filter sensitivity V_{TH}.

$$\text{required } \frac{S}{N} = 20\log\left(\frac{V_{IN}}{V_{IN} - V_{TH}}\right) + \frac{S}{N_{\text{Figure 5}}}$$

If this S/N is better than required for the application, $R3 \times C3_A$ can be reduced, or the operating bandwidth can be increased to obtain a faster tone detection time.

If the S/N performance is not adequate, the operating bandwidth can be reduced toward the MUBW, or $R3C3_A$ can be increased to improve S/N performance at the expense of slower response time.

5.11 Calculate C4 for 30° Phase Shift

Capacitor C4 is used to phase shift the input to the VCO commutating filter by 30°, thereby shifting the sampling clocks by the same amount. This enables the Detect sampling filter to sample and integrate at the maximum and minimum of the input tone.

$$C4 = \frac{\tan(30^\circ)}{2\pi \times f_0 \times R_V} \approx \frac{0.092}{f_0 \times R_V} \approx 164\text{pF}$$

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
Max. Output Switch Load Current		10	mA
P/LH/DW Package			
Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-30	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		2.7	3.3/5.0	5.5	V
Operating Temperature		-30		85	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0 V @ T_{AMB} = 25°C
Load resistance on decoder output = 20kΩ.

	Notes	Min.	Typ.	Max.	Units
Static Parameters					
I_{DD}			1.0		mA
Amplifier Input Impedance		160	200		kΩ
Digital Output Impedance			500	1000	Ω
Analog Output Impedance			1000	1200	Ω
Dynamic Parameters					
Input Signal					
Frequency		40		20,000	Hz
Lowest Must Detect Level	1		30		mV_{RMS}
Highest Will Not Detect Level	1		20		mV_{RMS}
Highest Will Not Detect $f_0/2$	1, 2		30 790		dB mV_{RMS}
Highest Will Not Detect $5(f_0)$	1, 2		20 250		dB mV_{RMS}
VCO					
Frequency	3	120		120,000	Hz
Frequency Stability			100 5000		ppm/°C ppm/V
BW Limiter					
BW Range		2		10	$\%f_0$
Amplifier					
Open Loop Gain			60		dB
GBWP			1.0		MHz
Closed Loop Gain			0		dB
Detect Commutating Filter					
Sensitivity (V_{TH})	1		25		mV_{RMS}

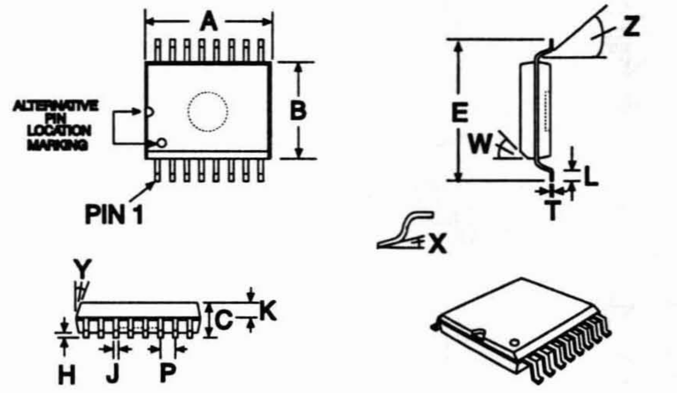
Operating Characteristics Notes:

1. Multiply by V_{DD} /5V for other supply values.
2. The reference level is V_{TH}. The following formula converts dB to mV_{RMS}.

$$mV_{RMS} = 10^{(dB/20)} \times V_{TH}$$

3. Observing pins 13, 14, or 15 (DW/J package) will cause a frequency shift due to additional loading. If tuning center frequency by observing oscillator, design in a buffer amplifier between pin 15 and probe/calibration point and tune with no input signal. Otherwise, tune by observing detect output band edges while sweeping input signal. VCO center frequency is $6(f_0)$ at pin 15 while it is $3(f_0)$ at pins 13 and 14.

6.2 Packaging

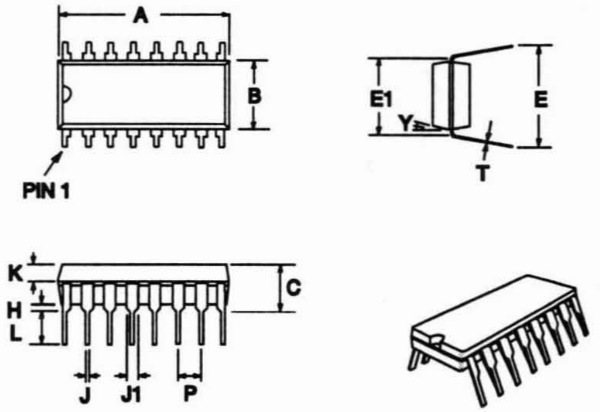


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: ***Order as part no. MX105ADW***

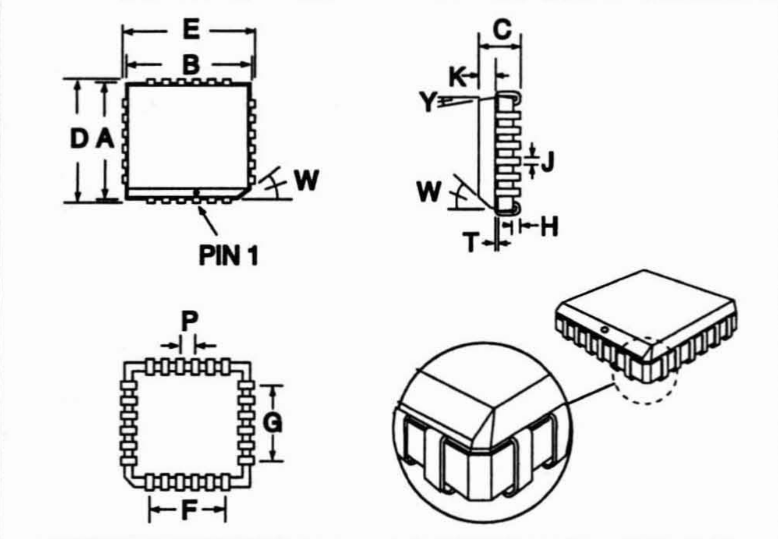


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7e	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin PDIP Mechanical Outline: ***Order as part no. MX105AP***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PLCC Mechanical Outline: ***Order as part no. MX105ALH***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

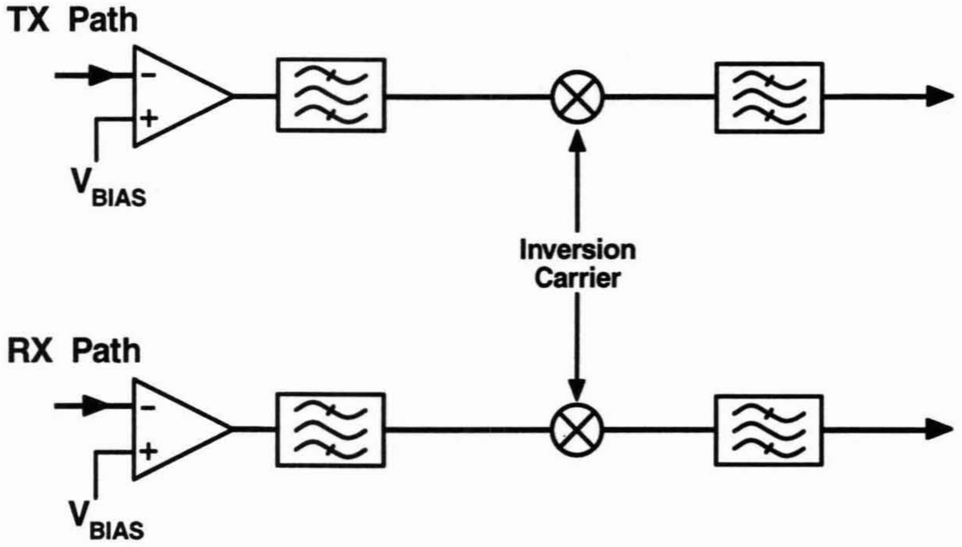
MX128 Cordless Telephone Scrambler

Features

- Full-Duplex Audio Processing
- On-Chip Filters
- Carrier Rejection >55dB
- Uses IF (10.24 MHz) Clock
- Requires No Extra Crystal
- Excellent Audio Quality
- Low Voltage 3.3V/5.0V Operation
- ECPA* Qualified Voice Protection

Applications

- Battery Powered Portability
- Cordless Telephones
- Wireless PBXs



The MX128 is a full-duplex frequency inversion scrambler designed to provide secure conversations for 46/49 MHz cordless telephone users. The RX and TX audio paths consist of the following:

1. A switched-capacitor balanced modulator with high baseband and carrier rejection.
2. A 3.3 kHz inversion carrier (injection tone).
3. A 3100 Hz lowpass filter.
4. Input op-amps with externally adjustable gain.

The MX128 uses mixed signal CMOS switched-capacitor filter technology and operates from a single supply in the range of 3.0V to 5.5V. The inversion carrier's frequency and filter switching clock are generated on-chip using an external 10.24 MHz or 3.58/3.6864 MHz crystal or clock input (selectable).

The MX128 is available in the following package styles: 16-pin SOIC (MX128DW) and 16-pin PDIP (MX128P).

*Electronics Communications Privacy Act (Title 18, US Code 2510 et seq.)

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4. **Application** .... **3 - 206**
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5. **Performance Specification** .... **3 - 207**
   - 5.1 Electrical Performance .... 3 - 207
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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

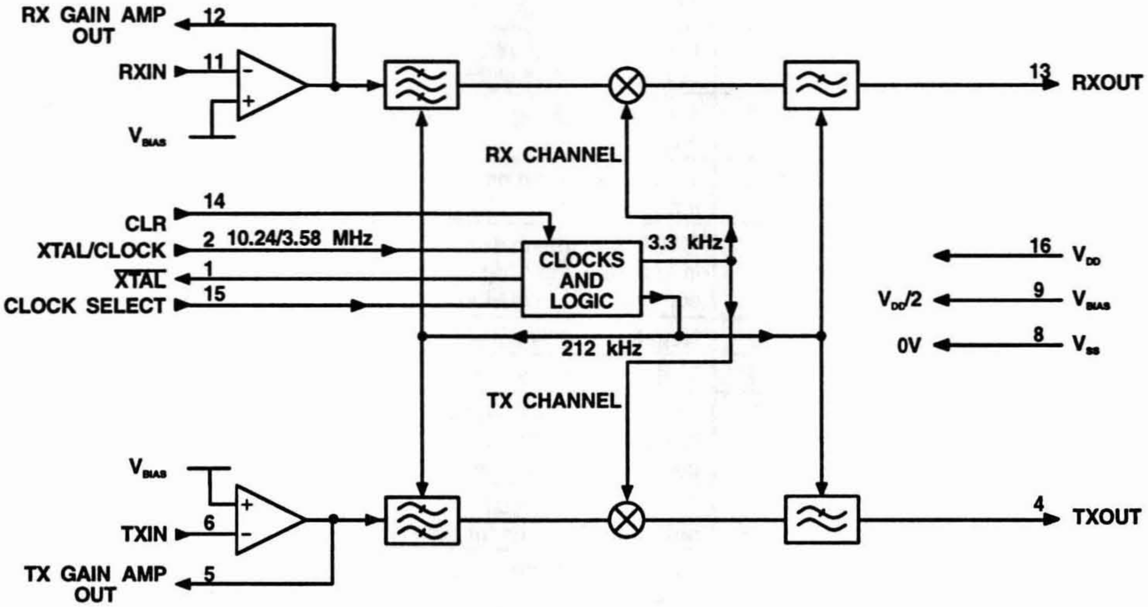
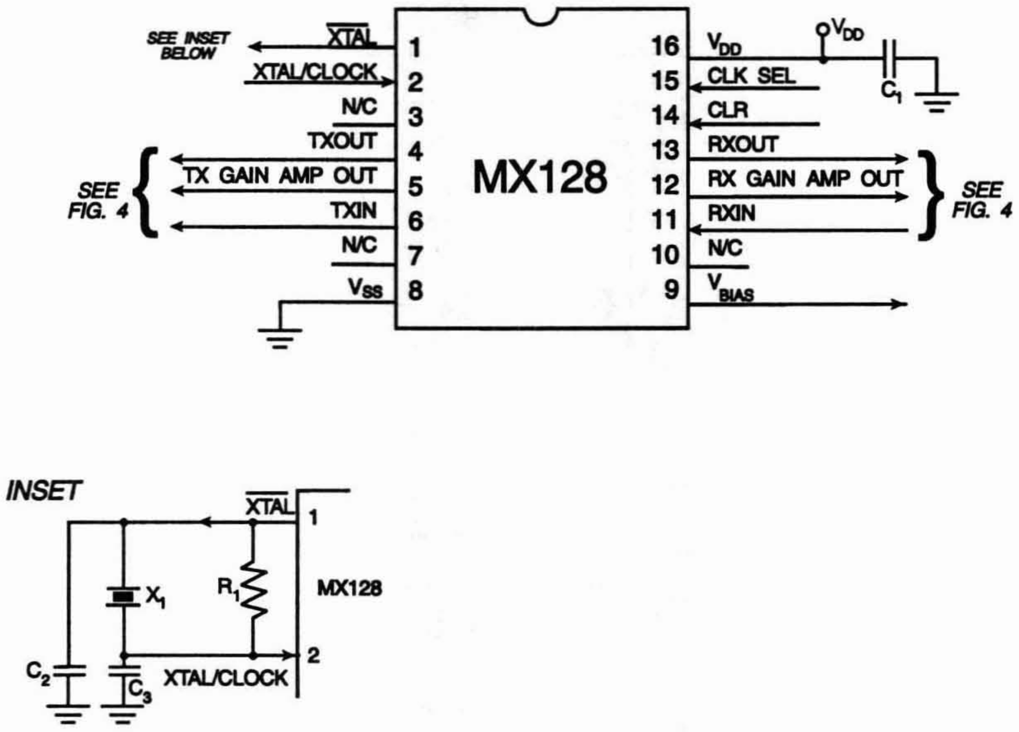

RX GAIN AMP OUT
12
RXIN
11
V_{BIAS}
RX CHANNEL
13
RXOUT
CLR
14
XTAL/CLOCK
2 10.24/3.58 MHz
XTAL
1
CLOCK SELECT
15
CLOCKS AND LOGIC
3.3 kHz
212 kHz
16 V_{DD}
$V_{DD}/2$
9 V_{BIAS}
0V
8 V_{SS}
TX CHANNEL
V_{BIAS}
TXIN
6
TX GAIN AMP OUT
5
4
TXOUT

Figure 1: Device Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{\text{Xtal}}$	output	This is the output of the clock oscillator inverter
2	Xtal/Clock	input	A 10.24 MHz, 3.58/3.6864 MHz, or an externally derived clock signal is injected at this pin. See Figure 3
4	TXOUT	output	This is the analog output of the transmit channel. It is internally biased at $V_{DD}/2$
5	TX Gain Ampout	output	This is the output pin of the transmit channel gain adjusting op-amp. See Figure 4 for gain setting components
6	TXIN	input	This is the analog signal input to the transmit channel. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
8	V_{SS}	power	Negative supply (GND)
9	V_{BIAS}	output	This is an internally generated bias voltage output ($V_{DD}/2$)
11	RXIN	input	This is the analog signal input to the receive channel. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
12	RX Gain Ampout	output	This is the output pin of the receive channel gain adjusting op-amp. See Figure 4 for gain setting components
13	RXOUT	output	This is the analog output of the receive channel. It is internally biased at $V_{DD}/2$
14	CLR		A logic 1 on this input selects the invert mode. A logic 0 selects the clear (not inverted) mode
15	Clock Select		Selects either 10.24 or 3.58/3.6864 MHz clock frequency. A logic "1" selects 10.24 MHz, and a logic "0" selects 3.58/3.6864 MHz. This input is internally pulled high
16	V_{DD}	power	Positive supply of 3.0V to 5.5 V
3, 7, 10	N/C		No internal connections

3. External Components


SEE INSET BELOW
XTAL
XTAL/CLOCK
N/C
TXOUT
TX GAIN AMP OUT
TXIN
N/C
VSS
SEE FIG. 4
1
2
3
4
5
6
7
8
MX128
16
15
14
13
12
11
10
9
VDD
CLK SEL
CLR
RXOUT
RX GAIN AMP OUT
RXIN
N/C
VBIAS
VDD
C1
SEE FIG. 4
INSET
XTAL
1
X1
R1
MX128
2
C2
C3
XTAL/CLOCK

10.24 MHz			
R1		1.0MΩ	±10%
C1		0.47µF	±20%
C2		22.0pF	±20%
C3		22.0pF	±20%
X1		10.24 MHz	

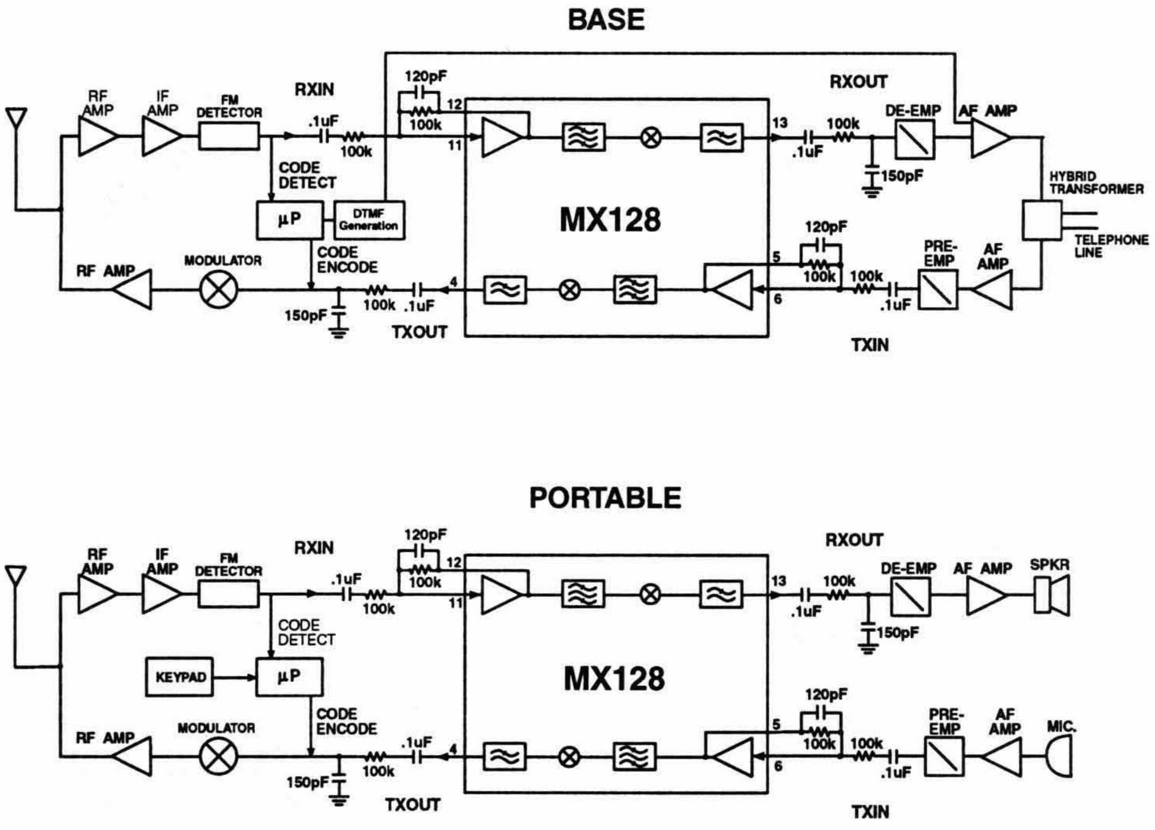
3.58/3.6864 MHz			
R1		1.0MΩ	±10%
C1		0.47µF	±20%
C2		33.0pF	±20%
C3		47.0pF	±20%
X1	Note 1	3.58/3.6864 MHz	

Figure 2: Recommended External Components

External Components Note:

1. For best results, a crystal oscillator should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak - peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. Application


BASE
RF AMP
IF AMP
FM DETECTOR
RXIN
.1uF
100k
120pF
12
100k
11
CODE DETECT
µP
DTMF Generation
CODE ENCODE
MX128
RF AMP
MODULATOR
100k .1uF
4
150pF
TXOUT
RXOUT
13
100k
.1uF
DE-EMP
AF AMP
150pF
HYBRID TRANSFORMER
TELEPHONE LINE
120pF
5
100k
100k
6
.1uF
PRE-EMP
AF AMP
TXIN
PORTABLE
RF AMP
IF AMP
FM DETECTOR
RXIN
.1uF
100k
120pF
12
100k
11
CODE DETECT
KEYPAD
µP
CODE ENCODE
MX128
RF AMP
MODULATOR
.1uF
100k
4
150pF
TXOUT
RXOUT
13
100k
.1uF
DE-EMP
AF AMP
SPKR
150pF
120pF
5
100k
100k
6
.1uF
PRE-EMP
AF AMP
MIC.
TXIN

Note: Components shown set a gain of 0dB.

Figure 3: Block Diagram of a Typical Application of the MX128 (Cordless Phone)

4.1 Application Notes

Formulas for calculating the carrier frequency, upper cutoff frequency and lower cutoff frequency with clock select pin high are as follows:

Carrier Frequency = (3.2995kHz / 10.24MHz) * XTAL frequency
Upper Cutoff Frequency = (2.800kHz / 10.24MHz) * XTAL frequency
Lower Cutoff Frequency = (400Hz / 10.24MHz) * XTAL frequency

Formulas for calculating the carrier frequency, upper cutoff frequency and lower cutoff frequency with clock select pin low are as follows:

Carrier Frequency = (3.2995kHz / 3.415MHz) * XTAL frequency
Upper Cutoff Frequency = (2.800kHz / 3.415MHz) * XTAL frequency
Lower Cutoff Frequency = (400Hz / 3.415MHz) * XTAL frequency

5. Performance Specification

5.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P/DW Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW max.
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Clock Frequency			10.24	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C
Clock Frequency = 10.24MHz
Audio Level 0dB ref. @ 1kHz = (V_{DD}-1) x 150mV_{RMS} e.g. V_{DD} = 3.3V 0dB = 345mV_{RMS}.

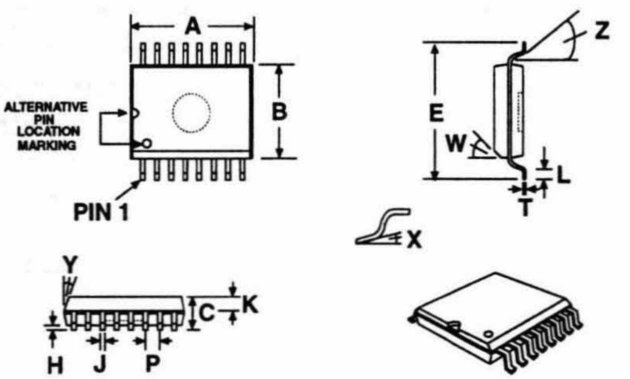
	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			2.0	3.0	mA
Input Impedance					
Digital	2	100			kΩ
Amplifiers	2	1.0	10.0		MΩ
Output Impedance (RXOUT, TXOUT)			1.0		kΩ
Input Logic 1 Voltage	1	70%			V_{DD}
Input Logic 0 Voltage	1			30%	V_{DD}
Dynamic Values					
Analog Signal Input Levels		-16.0		3	dB
Analog Output Noise	4		2.5	5.0	mV_{RMS}
Clear Mode					
Passband -3dB Cutoff Frequencies					
Low				300	Hz
High		3000			Hz
Passband Ripple (300-3000Hz)					
RX Channel		0		3.6	dB
TX Channel		0		2.9	dB
Passband Ripple (500-2750Hz)					
RX Channel		0		2.2	dB
TX Channel		0		2.0	dB
Filter Attenuation at 3.3 kHz					
RX Channel			30		dB
TX Channel			30		dB
Filter Attenuation at 3.6 kHz					
RX Channel			45		dB
TX Channel			45		dB
Passband Gain (@1kHz ref.)					
RX Channel		-1.5		0.5	dB
TX Channel		-1.5		0.5	dB
Switched-Capacitor Filter Sampling			211.066		kHz
Carrier Frequency			3298		Hz
Invert Mode Combined TX and RX Response					
Passband -3dB Cutoff Frequencies					
Low				400	Hz
High		2800			Hz
Passband Gain		-3		0.5	dB
Distortion (@1kHz)	3		1.75	2.75	%
Passband Gain (@1kHz ref.)	5	-2.5	-1.5	0	dB
Low Frequency Roll-off (<200 Hz)		12			dB/octave

	Notes	Min.	Typ.	Max	Units
Invert Mode Single Channel Response					
Unwanted Modulation Products	3				
RX Channel			-40		dB
TX Channel			-40		dB
Carrier Breakthrough	3				
RX Channel			-55		dB
TX Channel			-55		dB
Baseband Breakthrough	3				
RX Channel			-40		dB
TX Channel			-40		dB

Operating Characteristics Notes:

1. Batch sampled only
2. By characterization only
3. Measured with Input Level 0dB
4. Short circuit RX or TX input, measure noise at corresponding analog output, in 30KHz bandwidth
5. Op Amp gain 0dB
6. Clear mode only

5.2 Packaging

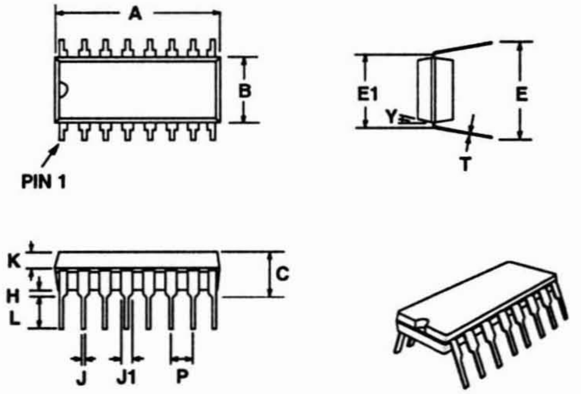


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 4: 16-pin SOIC Mechanical Outline: Order as part no. MX128DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
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E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin PDIP Mechanical Outline: Order as part no. MX128P

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX165C

Low Voltage CTCSS Encoder/Decoder

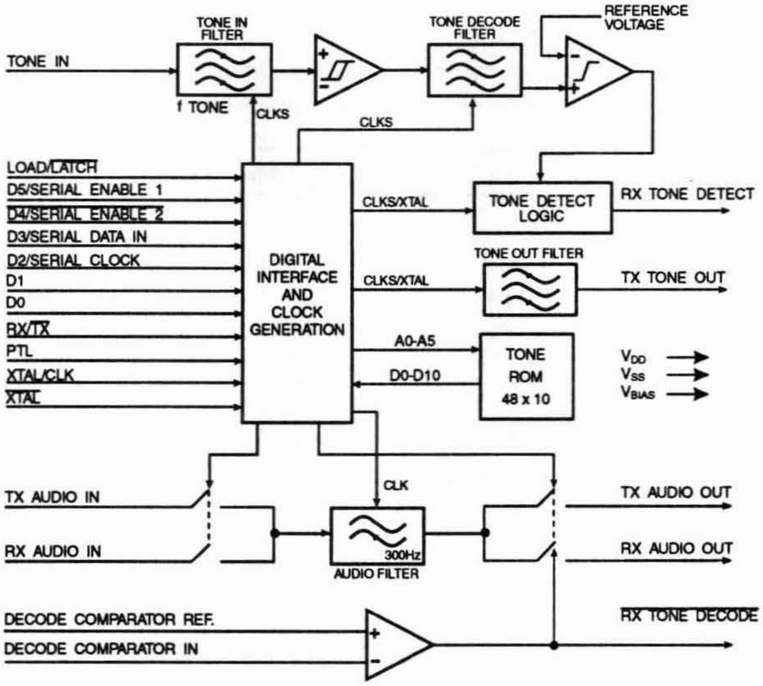
with TX/RX Filters

Features

- Meets TIA/EIA-603 Standards
- 47 CTCSS Tones + Notone
- TX/RX Speech Filters
- Improved Sinad
- Serial or Parallel Programming
- Easy µP Interface
- Scanning on any Channel
- Standard 1MHz Xtal (See MX465 for 4MHz)
- Low Voltage 3.3V to 5.0V

Applications

- Mobile Radio Channel Sharing
- Scan Trunking
- Wireless Intercom Traffic Control
- Hookswitch Supervision
- Repeater Control


TONE IN FILTER
TONE DECODE FILTER
REFERENCE VOLTAGE
TONE IN
f TONE
CLKS
CLKS
LOAD/LATCH
D5/SERIAL ENABLE 1
D4/SERIAL ENABLE 2
D3/SERIAL DATA IN
D2/SERIAL CLOCK
D1
D0
RX/TX
PTL
XTAL/CLK
XTAL
DIGITAL INTERFACE AND CLOCK GENERATION
CLKS/XTAL
TONE DETECT LOGIC
RX TONE DETECT
TONE OUT FILTER
CLKS/XTAL
TX TONE OUT
A0-A5
D0-D10
TONE ROM 48 x 10
V_{DD}
V_{SS}
V_{BIAS}
CLK
TX AUDIO IN
RX AUDIO IN
300Hz
AUDIO FILTER
TX AUDIO OUT
RX AUDIO OUT
DECODE COMPARATOR REF.
DECODE COMPARATOR IN
RX TONE DECODE

The MX165C CTCSS Encoder/Decoder is a low voltage, CMOS device that meets TIA/EIA-603 Standards. The MX165C will encode and decode the tones 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz in addition to the 39 standard CTCSS tones, for a total of 47 CTCSS tones + Notone. With the incorporation of the on-chip TX and RX speech filter, the MX165C enhances voice/tone multiplexing by attenuating TX and RX speech 36dB at frequencies below 250Hz while passing signals > 300Hz with only 1dB of ripple. This not only minimizes CTCSS talk-off i the TX mode but also improves Hum and Noise performance in the RX mode.

Available in the following package styles: 24-pin TSSOP (MX165CTN), 24-pin SOIC (MX165CDW), 24-pin PLCC (MX165CLH), and 24-pin PDIP (MX165CP), the MX165C requires a single 3.3V to 5.0V supply and a 1MHz clock or crystal.

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MX•COM, Inc. Reserves the right to change specifications at any time and without notice

1 Block Diagram

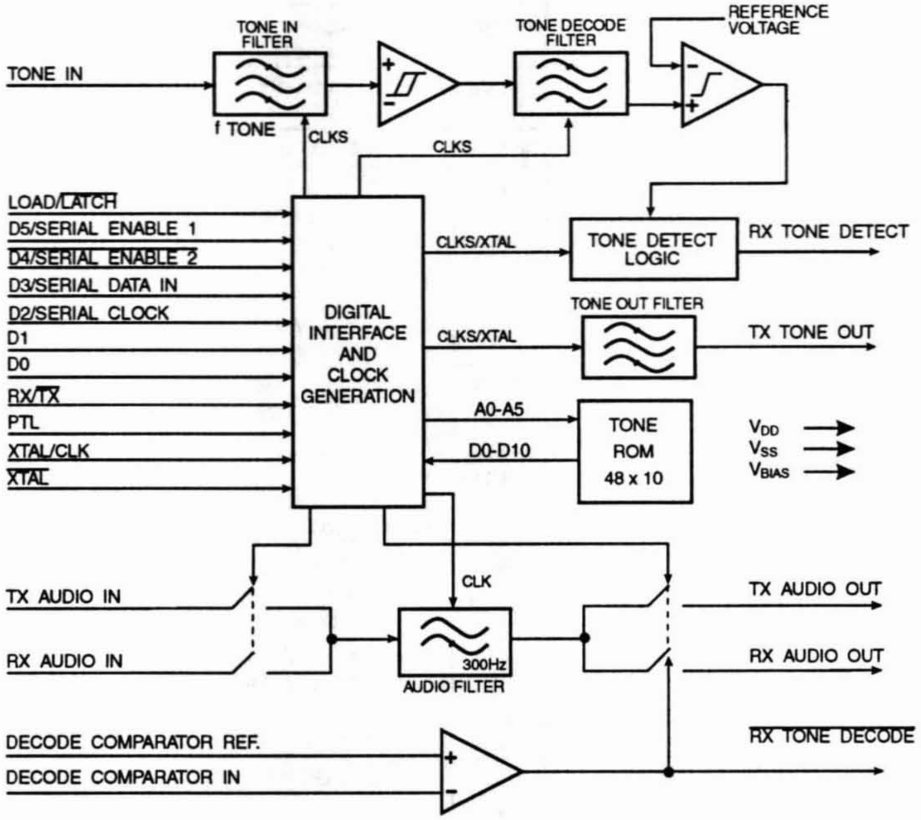

TONE IN
TONE IN FILTER
f TONE
CLKS
TONE DECODE FILTER
REFERENCE VOLTAGE
CLKS
LOAD/LATCH
D5/SERIAL ENABLE 1
D4/SERIAL ENABLE 2
D3/SERIAL DATA IN
D2/SERIAL CLOCK
D1
D0
RX/TX
PTL
XTAL/CLK
XTAL
DIGITAL INTERFACE AND CLOCK GENERATION
CLKS/XTAL
TONE DETECT LOGIC
RX TONE DETECT
TONE OUT FILTER
CLKS/XTAL
TX TONE OUT
A0-A5
D0-D10
TONE ROM 48 x 10
VDD
VSS
VBIAS
CLK
TX AUDIO IN
RX AUDIO IN
300Hz
AUDIO FILTER
TX AUDIO OUT
RX AUDIO OUT
DECODE COMPARATOR REF.
DECODE COMPARATOR IN
RX TONE DECODE

Figure 1 : Block Diagram

2 Signal List

Pin No.	Signal	Type	Description
1	V_{DD}	power	Positive supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
2	XTAL/CLOCK	input	Input to the on-chip inverter used with a 1MHz Xtal or external clock source.
3	$\overline{\text{XTAL}}$	output	Output of the on-chip inverter (clock output).
4	LOAD/$\overline{\text{LATCH}}$	input	Controls 8 on-chip latches. It is used to latch RX / $\overline{\text{TX}}$, PTL, and D0-D5. A logic 1 applied to this input places the 8 latches in the 'transparent' mode. A logic 0 applied to this input places the 8 latches in the 'latched' mode. In Parallel Mode, data is loaded and latched by a logic 1-0 transition (see Figure 4). In Serial Mode, data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Figure 5). Internally pulled to V_{DD}
5	D5 / SERIAL ENABLE 1	input	Data input D5 (Parallel Mode). A logic 1 applied to this input together with a logic 0 applied to D4/$\overline{\text{SERIAL ENABLE 2}}$ will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
6	D4 / $\overline{\text{SERIAL ENABLE 2}}$	input	Data input D4 (Parallel Mode). A logic 0 applied to this input together with a logic 1 applied to D5 / SERIAL ENABLE 1 will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
7	D3 / SERIAL DATA IN	input	Data input D3 (Parallel Mode). In Serial Mode this pin becomes the serial data input for D5-D0, RX / $\overline{\text{TX}}$ and PTL (see Figure 5). D5 is clocked first and PTL last. Internally pulled to V_{DD}.
8	D2 / SERIAL CLOCK	input	Data input D2 (Parallel Mode). In Serial Mode this pin becomes the SERIAL CLOCK input. Data is clocked on the positive going edge (see Figure 5). Internally pulled to V_{DD}.
9	D1	input	Data input D1 (Parallel Mode). Internally pulled to V_{DD}.
10	D0	input	Data input D0 (Parallel Mode). Internally pulled to V_{DD}.
11	V_{SS}	power	Negative supply.
12	DECODE COMPARATOR REF.	input	Internally biased to $V_{DD}/3$ or 2 $V_{DD}/3$ via 1M resistors depending on the logic state of the $\overline{\text{RX TONE DECODE}}$ pin. $\overline{\text{RX TONE DECODE}}$ = 1 will bias this input 2 $V_{DD}/3$; a logic 0 will bias this input $V_{DD}/3$. This input provides the DECODE COMPARATOR REFERENCE voltage, and the switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.
13	$\overline{\text{RX TONE DECODE}}$	output	Gated output of the decode comparator. This output is used to gate the RX Audio path. A logic 0 on this pin indicates a successful decode and the DECODE COMPARATOR IN pin is more positive than the DECODE COMPARATOR REF. input (see Table 3).
14	DECODE COMPARATOR IN	input	Inverting input of the DECODE COMPARATOR. This pin is normally connected to the integrated output of the RX TONE DETECT line.
15	RX TONE DETECT	output	In RX mode this output will go to logic 1 during a successful decode. It must be externally integrated to control response and deresponse times (see Table 3).
16	TX TONE OUT	output	The CTCSS sinewave output appears on this pin under control of the RX / $\overline{\text{TX}}$ pin. When not transmitting a tone, TX TONE OUT may be biased to $V_{DD}/2$. (see Table 3).
17	RX / $\overline{\text{TX}}$	input	RX or TX modes selected in Parallel Mode (see Figure 4). In Serial Mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.

Pin No.	Signal	Type	Description
18	PTL	input	In RX mode this pin operates as a 'Push To Listen' function by enabling the RX audio path, thus overriding the tone squelch function (Parallel Mode). In Serial Mode this function is loaded serially. Internal pull-up to V_{DD}
19	RX AUDIO OUT	output	High pass filtered RX AUDIO OUT. This pin outputs audio when $\overline{\text{RX TONE DECODE}}$ = logic 0, PTL = logic 1, or when Notone is programmed (see Table 4). In TX mode this pin is biased to $V_{DD}/2$.
20	TX AUDIO OUT	output	High pass filtered TX AUDIO OUT pin. In TX mode this pin outputs audio present at the TX AUDIO IN pin. In RX mode this pin is biased to $V_{DD}/2$
21	V_{BIAS}	output	Output of an internally generated V_{DD} /2 bias level that would normally be externally bypassed to V_{SS} via capacitor C6.
22	TX AUDIO IN	input	In TX mode TX AUDIO IN may be prefiltered, using the TX Audio path, thus helping to avoid talk-off due to intermodulation of speech frequencies with the transmitted CTCSS tone. Internally biased to $V_{DD}/2$.
23	RX AUDIO IN	input	Input to the audio high pass filter in RX mode. Internally biased to $V_{DD}/2$.
24	TONE INPUT	input	Input to the CTCSS tone detector. Internally biased to $V_{DD}/2$.

Table 1: Signal List

3 External Components

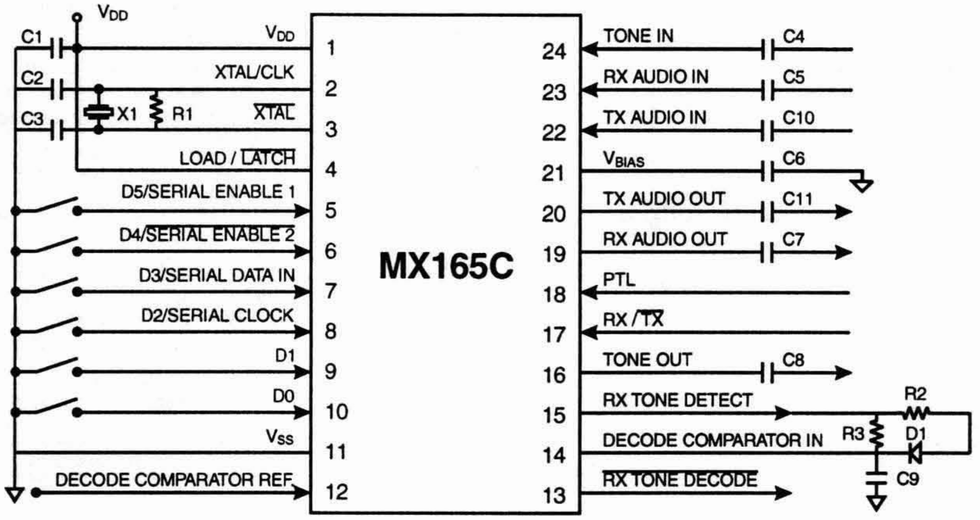

VDD
C1
C2
C3
X1
R1
VDD
XTAL/CLK
XTAL
LOAD / LATCH
D5/SERIAL ENABLE 1
D4/SERIAL ENABLE 2
D3/SERIAL DATA IN
D2/SERIAL CLOCK
D1
D0
VSS
DECODE COMPARATOR REF
1
2
3
4
5
6
7
8
9
10
11
12
MX165C
24
23
22
21
20
19
18
17
16
15
14
13
TONE IN
RX AUDIO IN
TX AUDIO IN
VBIAS
TX AUDIO OUT
RX AUDIO OUT
PTL
RX / TX
TONE OUT
RX TONE DETECT
DECODE COMPARATOR IN
RX TONE DECODE
C4
C5
C10
C6
C11
C7
C8
R2
R3
D1
C9

Figure 2 : Recommended External Components for Typical Application

R1	Note 1	4.7MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
C1		0.1µF	±20%
C2	Note 1	18pF	±20%
C3	Note 1	33pF	±20%
C4	Note 2	0.1µF	±20%
C5	Note 2	0.1µF	±20%

C6		0.47µF	±20%
C7	Note 2	0.1µF	±20%
C8	Note 2	0.1µF	±20%
C9	Note 2	0.1µF	±20%
C10	Note 2	0.1µF	±20%
C11	Note 2	0.1µF	±20%
D1		small signal	
X1	Note 1	1MHz	100ppm max.

Table 2: External Components

External Components Notes:

1. The values specified for R1, C2, and C3 have been found to be satisfactory when used with a crystal (X1) whose equivalent series resistance is ≤ 1000Ω. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. The 0.1µF value for the DC Blocking capacitors, C4, C5, C7, C8, C9, C10, and C11 is not a requirement. For the capacitors C4, C5, and C10, the input impedance is internal to the device and specified typical as 550kΩ. For the remaining capacitors external circuits will be important in determining the input impedance.

4 General Description

4.1 Description

Voice on shared radio channels are multiplexed with a subaudible CTCSS (Continuous Tone Controlled Subaudible Squelch) tone as a means of directing messages among user groups sharing the same RF frequencies. CTCSS modulates the transmitter with a discrete tone, from 39 standard CTCSS tones in the range (67.0Hz to 250.0Hz) accordin to TIA/EIA-603. There are an additional eight CTCSS tones not specified in TIA/EIA-603 that the MX165C will encode an decode. They are : 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz, for a total of 47 CTCSS tones plus Notone.

The MX165C also incorporates TX/RX on chip speech filters. In early CTCSS designs, TX speech was not filtered from the CTCSS tone, rather the filtering was dependent upon the host transmitter's pre-emphasis network. At only 6dB/octave, the attenuation of speech components at higher CTCSS tones was only a few dB which resulted in talk-off (low frequency voice components unsquelching the receiver audio).

4.2 I/O Conditions

D0-D5	Tone	No Tone	Tone	Tone	Tone	No Tone
Input Pins Condition						
RX / $\overline{\text{TX}}$	0	0	1	1	1	1
PTL	0	X	0	1	X	X
Decode Comparator In	X	X	0	0	1	X
Output Pins Condition						
RX TONE DETECT	0	0	0	0	1	X
$\overline{\text{RX TONE DECODE}}$	1	1	1	1	0	0
Result / Function						
Tone Transmitter Enabled	Yes	No (Bias)	No (Bias)	No (Bias)	No (Bias)	No (Bias)
TX Audio Path Enabled	Yes	Yes	No	No	No	No
Tone Decode Enabled	No	No	Yes	Yes	Yes	Yes
RX Audio Path Enabled	No (Bias)	No (Bias)	No (Bias)	Yes	Yes	Yes
Notes	1	2	3	4	5	6

Notes:

1. Normal tone transmit condition.
2. Notone programmed in TX mode, tone transmit output set to $V_{DD}/2$. TX audio path enabled.
3. Normal decode standby.
4. Normal decode standby with PTL used to enable audio.
5. Normal decode of correct CTCSS tone condition, PTL has no effect.
6. Notone programmed in RX mode, tone transmit output (Bias). RX audio path enabled.
7. X = don't care

Table 3: Combinations of Input / Output conditions

4.3 Filter Response

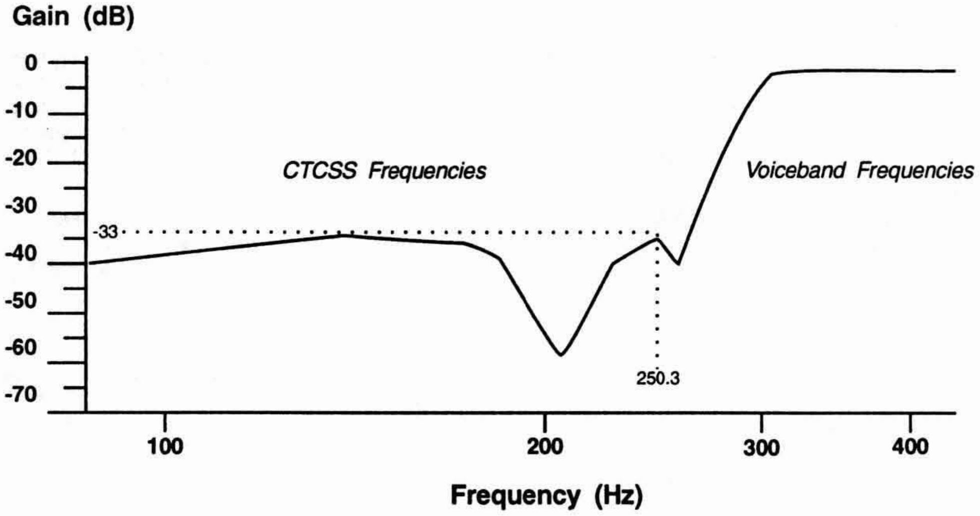


Figure 3 : Voiceband Filter Response

4.4 Serial and Parallel Mode Timing

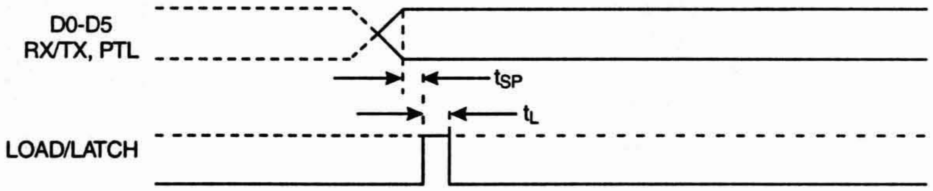
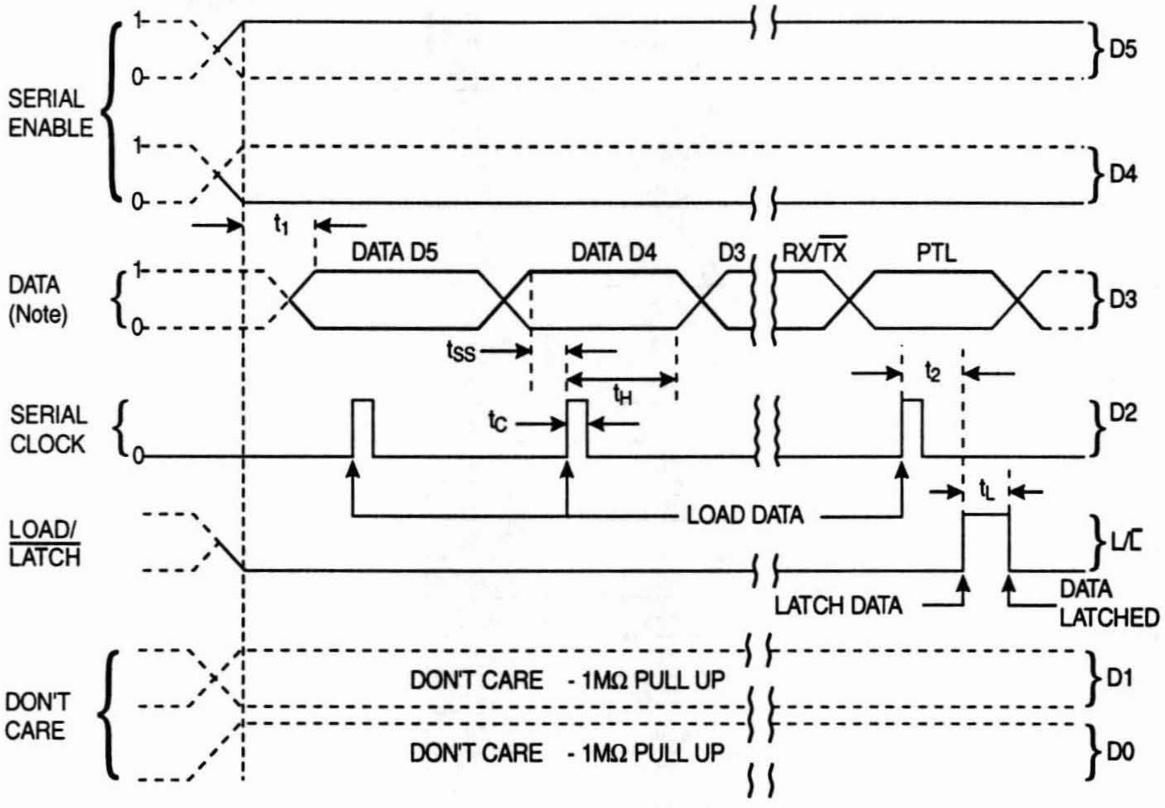

D0-D5
RX/TX, PTL
t_{SP}
t_L
LOAD/LATCH

Figure 4 : Parallel Mode


SERIAL ENABLE
1
0
D5
1
0
D4
t1
DATA D5
DATA D4
D3
RX/$\overline{TX}$
PTL
DATA (Note)
1
0
D3
tSS
tH
t2
tC
SERIAL CLOCK
0
D2
LOAD DATA
tL
LOAD/$\overline{LATCH}$
L/$\overline{L}$
LATCH DATA
DATA LATCHED
DON'T CARE
DON'T CARE - 1MΩ PULL UP
D1
DON'T CARE - 1MΩ PULL UP
D0

Note : Serial bit 1 through bit 8 = D5, D4, D3, D2, D1, D0, RX/TX and PTL respectively. Load bit 1 first, bit 8 last

Figure 5 : Serial Mode

4.5 CTCSS Programming

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX165C Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
	67.0	66.98	-0.029	1	1	1	1	1	1	3F
	69.3	69.32	0.024	1	1	1	0	0	1	39
	71.9	71.901	0.001	0	1	1	1	1	1	1F
	74.4	74.431	0.042	1	1	1	1	1	0	3E
	77.0	76.965	-0.046	0	0	1	1	1	1	0F
	79.7	79.677	-0.029	1	1	1	1	0	1	3D
	82.5	82.483	-0.021	0	1	1	1	1	0	1E
	85.4	85.383	-0.020	1	1	1	1	0	0	3C
	88.5	88.494	-0.007	0	0	1	1	1	0	0E
	91.5	91.456	-0.048	1	1	1	0	1	1	3B
	94.8	94.76	-0.042	0	1	1	1	0	1	1D
	97.4	97.435	-0.036	1	1	1	0	1	0	3A
	100.0	99.96	-0.040	0	0	1	1	0	1	0D
	103.5	103.429	-0.069	0	1	1	1	0	0	1C
	107.2	107.147	-0.05	0	0	1	1	0	0	0C
	110.9	110.954	0.049	0	1	1	0	1	1	1B
	114.8	114.84	0.035	0	0	1	0	1	1	0B
	118.8	118.793	-0.006	0	1	1	0	1	0	1A
	123.0	123.028	0.023	0	0	1	0	1	0	0A
	127.3	127.328	0.022	0	1	1	0	0	1	19
	131.8	131.674	-0.095	0	0	1	0	0	1	09
	136.5	136.612	0.082	0	1	1	0	0	0	18
	141.3	141.323	0.016	0	0	1	0	0	0	08
	146.2	146.044	-0.107	0	1	0	1	1	1	17
	151.4	151.441	0.027	0	0	0	1	1	1	07
	156.7	156.875	0.112	0	1	0	1	1	0	16
•	159.8	159.936	0.085	1	1	0	0	0	1	31
	162.2	162.311	0.069	0	0	0	1	1	0	06
	167.9	167.708	-0.114	0	1	0	1	0	1	15
	173.8	173.936	0.078	0	0	0	1	0	1	05
	179.9	179.654	-0.137	0	1	0	1	0	0	14
•	183.5	183.680	0.098	1	1	0	0	1	0	32
	186.2	186.289	0.048	0	0	0	1	0	0	04
•	189.9	190.069	0.089	1	1	0	0	1	1	33
	192.8	192.864	0.033	0	1	0	0	1	1	13
•	196.6	196.329	-0.138	1	1	0	1	0	0	34
•	199.5	199.312	-0.094	1	1	0	1	0	1	35
	203.5	203.645	0.071	0	0	0	0	1	1	03
•	206.5	206.207	-0.142	1	1	0	1	1	0	36
	210.7	210.848	0.070	0	1	0	0	1	0	12
	218.1	217.853	-0.113	0	0	0	0	1	0	02
	225.7	225.339	-0.160	0	1	0	0	0	1	11

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX165C Frequency (Hz)	Δ f_0 (%)	D5	D4	D3	D2	D1	D0	Hex
•	229.1	229.279	0.078	1	1	0	1	1	1	37
	233.6	233.359	-0.103	0	0	0	0	0	1	01
	241.8	241.970	0.070	0	1	0	0	0	0	10
	250.3	250.282	-0.007	0	0	0	0	0	0	00
•	254.1	254.162	0.024	1	1	1	0	0	0	38
	Notone		N/A	1	1	0	0	0	0	30
	Serial input mode		N/A	1	0	Data	Clock	X	X	2X

- Not specified in the TIA/EIA tone set

Table 4: CTCSS Tones

5 Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pins	-20	20	mA
TN / DW / LH / DIP Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied

	Min.	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	2.7	5.5	V
Xtal Frequency	1.0	1.0	MHz
Operating Temperature	-40	85	°C

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified

V_{DD} = 3.3V / 5.0V at T_{AMB} = 25°C, V_{SS} = 0V,
Xtal Frequency = 1.0 MHz, 100ppm max.
(Over the life of the Xtal the operating range may vary from 100ppm up to 1000ppm)
0dB ref. = 750mV_{RMS} (proportional to V_{DD}; see note 17)

Composite Signal:
1kHz test tone = 300mV_{RMS}, f_0 CTCSS tone = 30 mV_{RMS}, 75mV_{RMS} Noise (band limited to 6kHz Gaussian)

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply voltage		2.7	3.3/5.0	5.5	V
Supply current					
V_{DD} = 5.0V			3.2	4.2	mA
V_{DD} = 3.3V			1.1	1.6	mA
Rx Monitor			2.0		mA
Analog input impedance	18	480	550		kΩ
Analog output impedance	18		400	1000	Ω
Digital Input impedance	1,18	25	40		kΩ
Input logic 1	1	70%V_{DD}			V
Input logic 0	1			30%V_{DD}	V
Output Logic 1 source = 0.1mA	2	80%V_{DD}			V
Output Logic 0 sink = 0.1mA	2			20%V_{DD}	V
Dynamic Values					
Speech filter					
Total harmonic distortion	5,8,19		0.7	1.5	%
Output noise level (input ac short circuit, audio switch enabled)	8,18		0.5	1.0	mV_{RMS}
Sinad	8,9	40	50		dB
Spurious emissions	18			- 48	dB
Cutoff frequency			300		Hz
Bandpass ripple	8		1	1.8	dB
Stopband attenuation <250Hz	7,8,19	33	36		dB
Passband gain 1kHz		- 0.5	0	0.5	dB
TX/RX isolation	5		60		dB
Encoder					
Tone output level	12	-1.0	0	1.0	dB
Tone Frequency Accuracy (f error)		- 0.3		0.3	%f_0
Risetime to 90% nominal output					
f_0>100Hz	4,10		15	75	ms
f_0<100Hz	4,10		45	120	ms
Total Harmonic Distortion	19		1.5	2	%

	Notes	Min.	Typ.	Max.	Units
Decoder					
Pure tone decode threshold	19		7	15	mV_{RMS}
Composite signal decode threshold	3			30	mV_{RMS}
Decode input signal level	16	-20		3.5	dB
Pure tone decode response time	13,14	95	115	140	ms
Pure tone decode deresponse time	13,15	95	130	170	ms
Decode response time	3,6,10			250	ms
Deresponse time	3,10		180	250	ms
Decode selectivity:					
Upper decode band edge	3,11,19,20	$1.005f_0$	$1.015f_0$	$0.995f_{0+1}$	Hz
Lower decode band edge	3,11,19,20	$1.005f_{0-1}$	$0.985f_0$	$0.995f_0$	Hz
Serial / Parallel Inputs					
Parallel Set Up Time (t_{SP})		400			ns
Load / Latch Pulse Width (t_L)		400			ns
Serial Clock Pulse Width (t_C)		400			ns
Serial Data Set-Up Time (t_{SS})		400			ns
Serial Data Hold Time (t_H)		400			ns
Serial Enable Time (t_1)		400			ns
Serial Load / Latch Set-Up Time (t_2)		400			ns
Serial Clock Frequency			1		MHz

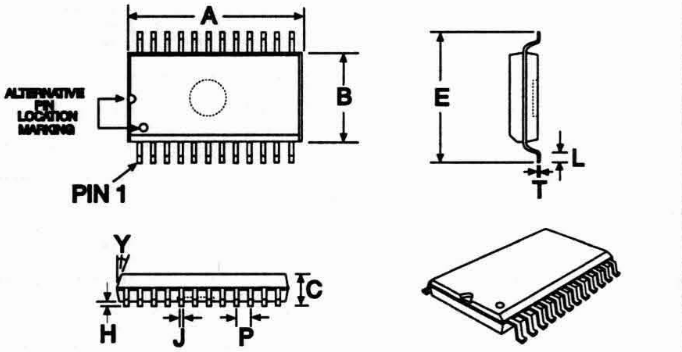
Operating Characteristics Notes:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite signal test condition.
4. Any programming tone and $R_L = 10k\Omega$, $C_L = 15pF$.
5. With an input level of 0dB @1kHz
6. f_0>100Hz (for 100 Hz> f_0>67Hz: t=100/ f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. With an input level of -3.5dB @1kHz
10. Per TIA/EIA-603.
11. Per TIA/EIA-603, device will not decode adjacent TIA/EIA-603 Tones.
12. Tone output level is proportional to V_{DD}.
13. f_0=156.7Hz @ -20dB.
14. Typically 12.5 Tone Cycles + 40ms.
15. Typically 7 Tone Cycles + 90ms.
16. Max composite signal is 3.5dB with:
    Noise (band limited 6kHz Gaussian) = -12dB ref. to 1kHz test tone
    f_0 CTCSS tone = -20dB ref. to 1kHz test tone
17. For maximum dynamic range, set audio level to 0dB, V_{DD} x150mV_{RMS}, using minimum V_{DD} under which system is intended to work. (e.g. for a 2.7V system, use 0dB equal to 405mV_{RMS}).
18. By characterization only.

19. Batch sampled only
20. For example, if: $f_0 = 100.0Hz$ ($f_{0-1} = 97.4Hz$ $f_{0+1} = 103.5Hz$)

Decode Selectivity	Min	Typ	Max	Unit
Upper Decode Band Edge	100.5	101.5	102.98	Hz
Lower Decode Band Edge	97.89	98.5	99.5	Hz

5.2 Packaging

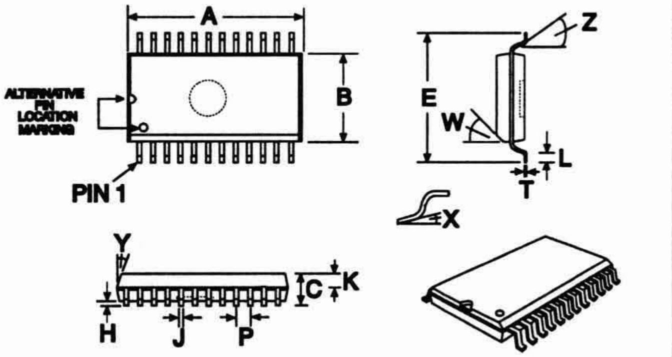

A
B
E
L
T
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	---------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin TSSOP Mechanical Outline: Order as part no. MX165CTN

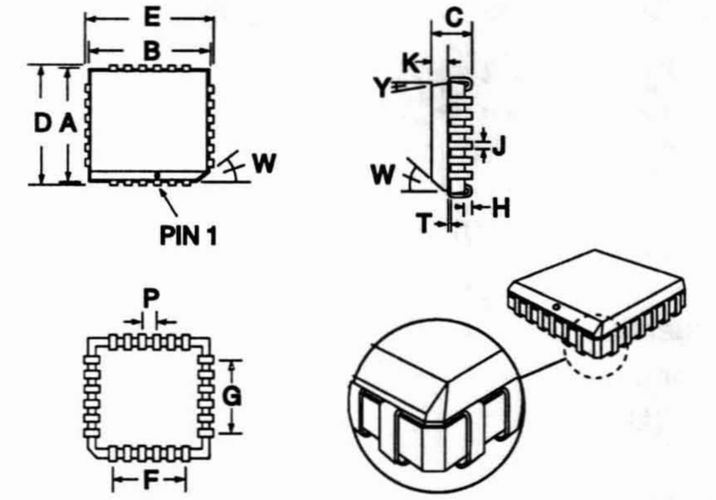

A
B
E
Z
W
L
T
X
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
K
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin SOIC Mechanical Outline: Order as part no. MX165CDW

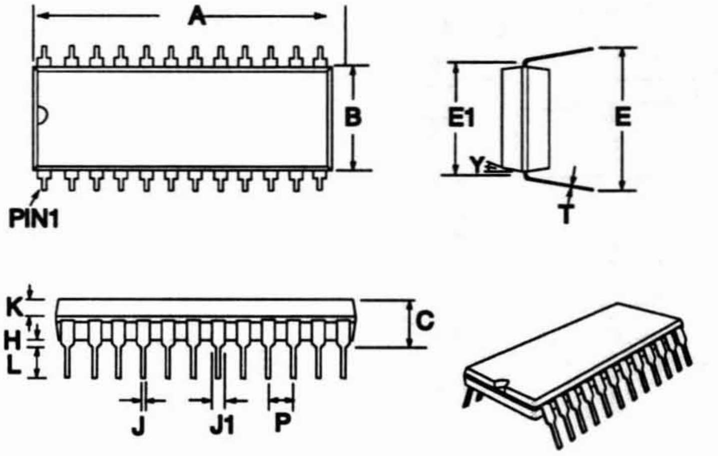


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PLCC Mechanical Outline: Order as part no. MX165CLH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin PDIP Mechanical Outline: Order as part no. MX165CP

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

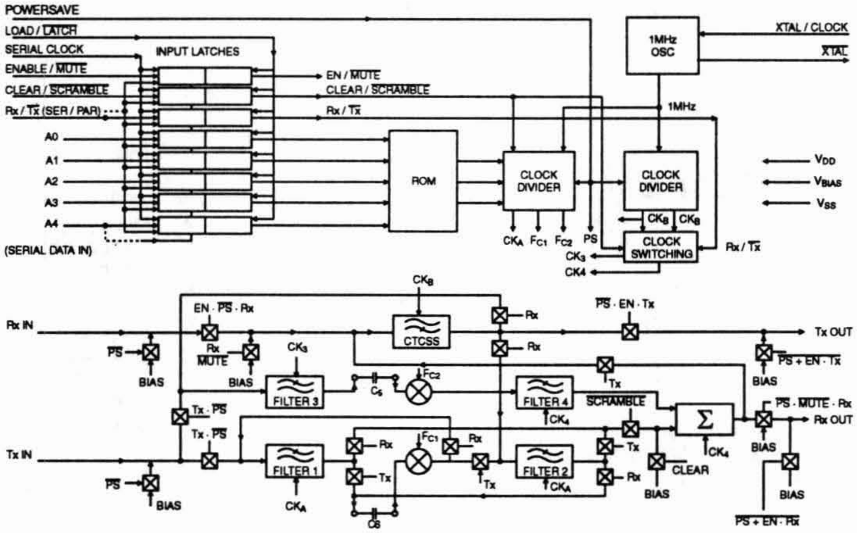
MX214/224 Variable Split Band Inverter

Features

- **CTCSS Highpass Filter**
- **Good Recovered Audio Quality**
- **Fixed and Rolling Code Modes**
- **Serial (MX214) and Parallel (MX224) Loading Options**
- **32 Programmable Split Points**
- **Half-Duplex Capability**

Applications

- **Mobile Radio Voice Security**
- **Cellular Telephone Voice Security**


POWERSAVE
LOAD / $\overline{\text{LATCH}}$
SERIAL CLOCK
ENABLE / $\overline{\text{MUTE}}$
CLEAR / $\overline{\text{SCRAMBLE}}$
Rx / $\overline{\text{Tx}}$ (SER / PAR)
A0
A1
A2
A3
A4
(SERIAL DATA IN)
INPUT LATCHES
EN / $\overline{\text{MUTE}}$
CLEAR / $\overline{\text{SCRAMBLE}}$
Rx / $\overline{\text{Tx}}$
ROM
CLOCK DIVIDER
CLOCK DIVIDER
1MHz OSC
1MHz
XTAL / CLOCK
$\overline{\text{XTAL}}$
V_{DD}
V_{BIAS}
V_{SS}
CK_B
CK_B
CLOCK SWITCHING
Rx / $\overline{\text{Tx}}$
CK_A
F_{C1}
F_{C2}
PS
CK_3
CK4
CK_B
EN · $\overline{\text{PS}}$ · Rx
Rx IN
$\overline{\text{PS}}$
BIAS
Rx
$\overline{\text{MUTE}}$
BIAS
CK_3
CTCSS
Rx
Rx
$\overline{\text{PS}}$ · EN · Tx
Tx OUT
$\overline{\overline{\text{PS}} + \text{EN} \cdot \text{Tx}}$
BIAS
FILTER 3
C_5
F_{C2}
Tx
FILTER 4
CK_4
$\overline{\text{SCRAMBLE}}$
Σ
CK_4
$\overline{\text{PS}}$ · $\overline{\text{MUTE}}$ · Rx
Rx OUT
BIAS
Tx · $\overline{\text{PS}}$
Tx · $\overline{\text{PS}}$
Tx IN
$\overline{\text{PS}}$
BIAS
FILTER 1
CK_A
Rx
Tx
F_{C1}
Rx
Tx
FILTER 2
CK_A
Tx
Rx
CLEAR
BIAS
BIAS
C6
$\overline{\overline{\text{PS}} + \text{EN} \cdot \text{Rx}}$

The MX214/224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/224 ICs include a highpass filter that rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier generation MX204 VSB Inverter.

The MX214/224 splits the voiceband (300-2700Hz) into upper and lower subbands, and inverts each subband about itself. The 'split point' (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000Hz range. In the 'fixed code' mode, a single point is used. Fixed mode operation nets approximately 4 mutually exclusive secure channels.

In 'rolling code' mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip ' Mute' function is useful when implementing rolling code continuous synchronization schemes. 'Powersave' and 'Clear/Scramble' controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1MHz reference oscillator driven by a 1MHz crystal or clock pulse input.

The MX214 and the MX224 operate from a single 5.0V supply and available in the following packages: 22-pin CDIP (MX214J/MX224J), 22-pin PDIP (MX214P/MX224P), and 24-pin PLCC (MX214LH/MX224LH).

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MX-COM, Inc. reserves the right to change specifications at any time without notice.

1. Block Diagram

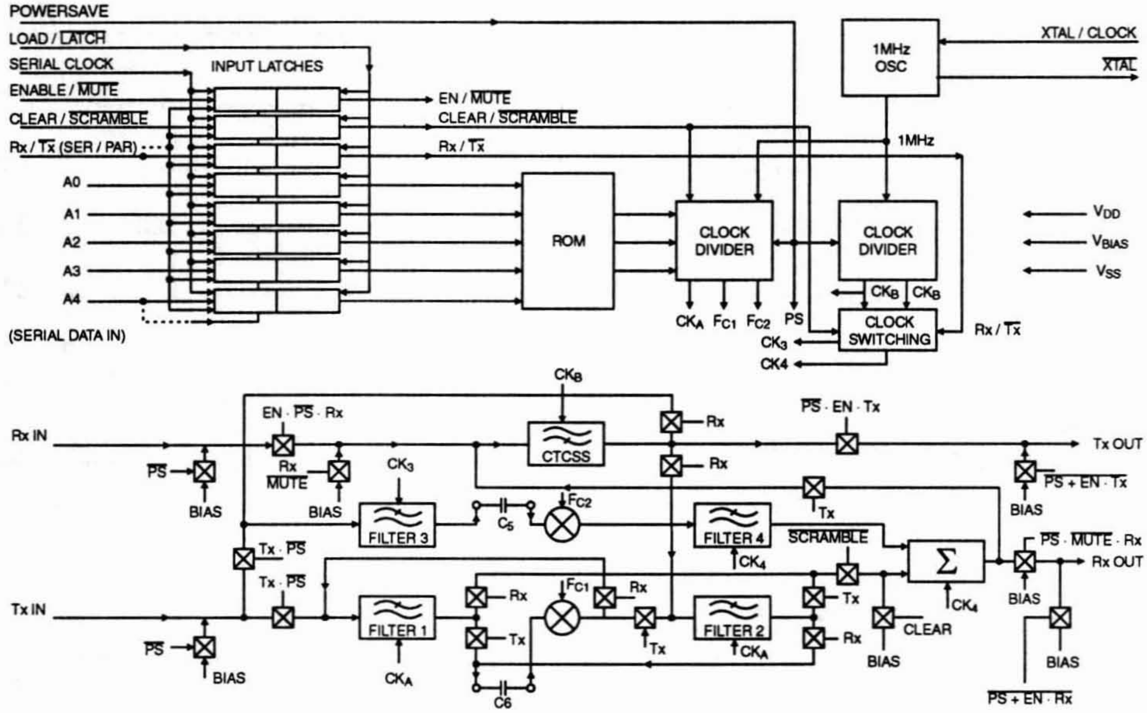

POWERSAVE
LOAD / $\overline{\text{LATCH}}$
SERIAL CLOCK
ENABLE / $\overline{\text{MUTE}}$
CLEAR / $\overline{\text{SCRAMBLE}}$
Rx / $\overline{\text{Tx}}$ (SER / PAR)
A0
A1
A2
A3
A4
(SERIAL DATA IN)
INPUT LATCHES
EN / $\overline{\text{MUTE}}$
CLEAR / $\overline{\text{SCRAMBLE}}$
Rx / $\overline{\text{Tx}}$
ROM
CLOCK DIVIDER
CLOCK DIVIDER
1MHz OSC
1MHz
XTAL / CLOCK
$\overline{\text{XTAL}}$
CK_A F_{C1} F_{C2} PS
CK_B CK_B
CLOCK SWITCHING
CK_3
CK4
Rx / $\overline{\text{Tx}}$
V_{DD}
V_{BIAS}
V_{SS}
CK_B
Rx IN
EN · $\overline{\text{PS}}$ · Rx
Rx $\overline{\text{MUTE}}$
$\overline{\text{PS}}$
BIAS
BIAS
CK_3
FILTER 3
C_5
F_{C2}
CTCSS
Rx
Rx
$\overline{\text{PS}}$ · EN · Tx
Tx OUT
$\overline{\text{PS}}$ + EN · $\overline{\text{Tx}}$
BIAS
Tx
FILTER 4
$\overline{\text{SCRAMBLE}}$
CK_4
Σ
CK_4
$\overline{\text{PS}}$ · $\overline{\text{MUTE}}$ · Rx
Rx OUT
BIAS
Tx · $\overline{\text{PS}}$
Tx · $\overline{\text{PS}}$
Tx IN
$\overline{\text{PS}}$
BIAS
FILTER 1
CK_A
Rx
Tx
F_{C1}
Rx
Tx
C6
FILTER 2
CK_A
Tx
Rx
CLEAR
BIAS
BIAS
$\overline{\text{PS}}$ + EN · $\overline{\text{Rx}}$

Figure 1: Block Diagram

2. Signal List

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
7	1	1	1	Xtal/Clock	Input to the clock oscillator inverter. A 1MHz crystal input or externally derived 1MHz clock is injected here.
8	2	2	2	$\overline{\text{Xtal}}$	Output of the clock oscillator inverter.
9	3			Serial Data Input	This pin is used to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and in input in the following sequence: MUTE, CLEAR, Rx/$\overline{\text{Tx}}$, A0, A1, A2, A3, A4. The Load/$\overline{\text{Latch}}$ is operated on the completion. Reference the timing diagram in Figure 7.
		3 – A4 4 – A3 5 – A2 6 – A1 7 – A0	3 – A4 4 – A3 5 – A2 6 – A1 7 – A0	Programming Inputs	In parallel mode, these five digital inputs define the split point frequency. Each of the 5 input pins has a 1MΩ internal pull-up resistor. See table 2 for programming information.
		8	8	Rx/$\overline{\text{Tx}}$	This digital input selects the Receive and Transmit paths and configures upperband and lowerband filter bandwidths while setting the CTCSS highpass filter position on the signal path. See Table 1 and Figure 5 and figure 6. 1MΩ internal pull-up resistor (Rx).
13	8			Parallel/$\overline{\text{Serial}}$	This pin must be connected to V_{SS} for serial loading. Internal 1MΩ pull-up resistor.
		9	9	Clear/Scramble	This digital input puts the device into 'Clear' or 'Scramble' mode by controlling the application of carrier frequency to the Upper and Lower band balanced modulators. In 'Scramble' mode, the balanced modulator carrier frequency values are selected by the split point address A0-A4. See Table 2. In 'Clear' mode, the carriers are disabled and the balanced modulators are bypassed internally, i.e. the lower band signal is not added to the output signal. 1MHz internal pull-up resistor (Clear).
		10	10	Enable/Mute	This digital function is used to disable the Receive or the Transmit signal paths for rolling code synchronization while maintaining bias conditions. Synchronization data can be transmitted during the Mute periods, as is done in the MX1204 VSB Scrambler Module. 1MΩ Internal pull-up resistor (Enable)
14	10			Serial Clock Input	This is the externally applied data clock frequency used to shift input data along in devices wired in the Serial-loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram Figure 7. 1MΩ Internal pull-up resistor.

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
15	11	11	11	Load/$\overline{\text{Latch}}$	This pin controls the loading of the 8 digital function inputs (ENABLE, CLEAR, A0-A4) into the internal register. When this pin is at a logic '1', all eight inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel, Load/$\overline{\text{Latch}}$ must be kept at logic '0' while a new function is loaded, then strobed 0-1-0 to latch the inputs in. For serial loading, the serial data should be loaded with the Load/$\overline{\text{Latch}}$ at logic '0' and then the Load/$\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. Internal 1MΩ pull-up resistor (Load). See Figure 7.
16	12	12	12	Powersave	This digital input is used to place the MX214/224 into Powersave mode where all parts of the device except the 1MHz oscillator are shut down. All signal input and output lines are made open circuit, free of all bias. This allows signal paths to be routed externally around the device, while reducing current consumption. A logic '0' at this input enables the device to work normally as shown in Table 1. Internal 1MΩ pull-up resistor.
17	13	13	13	V_{SS}	Negative supply (GND)
18	14	14	14	Internal connection	This pin is internally connected. Leave open circuit.
19	15	15	15	Rx Output	This is the processed received audio signal output. This pin is held at a DC 'bias' voltage for all functions except Powersave. This buffered output is driven by the summing circuit in the Rx mode. Signal paths and bias levels are detailed in Table 1 and Figure 6.
20	16	16	16	Tx Output	This is the processed audio output for the transmission channel. This pin is held at a DC 'bias' voltage for all functions except Powersave. This summed and buffered signal is passed through the CTCSS high pass Filter to the output pin in the Tx Mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	V_{BIAS}	Normally at $V_{DD}/2$, this pin requires an external decoupling capacitor (C7) to V_{SS}.
22	18	18	18	Rx Input	This is the analog received signal input. This pin is held at a DC 'bias' voltage by a 300kΩ on-chip bias resistor, which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C3. See figure 2. This input is routed through the CTCSS High Pass Filter in Rx mode to remove subaudio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	Highband Filter Output	The output of the Input Filter of the Upperband limit. The Rx/$\overline{\text{Tx}}$ functions sets the lowpass filter at 3400Hz or 2700Hz respectively. This output must be connected to the Highband Balanced modulator input via capacitor C5. See figure 2.

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
2	20	20	20	Highband Balanced Modulator Input	The input to the Balanced Modulator of the Upperband limit. This input must be connected to the Highband Filter Output via capacitor C5. See figure 2.
3	21	21	21	Lowband Balanced Modulator Input	The input to the Balanced Modulator of the Lowerband limit. This input must be connected to the Lowband Filter Output via capacitor C6. See figure 2.
4	22	22	22	Tx input	This analog 'Clear' audio input for the VSB Scrambler. This pin is held at a DC 'bias' voltage by a 300kΩ on-chip bias resistor, which is selected for all functions except powersave. In must be connected to external circuitry by capacitor C4. See figure2. This input, in Tx mode, is connected to Upper and Lowerband input filters. Signal paths and bias levels are detailed in Table 1 and figure 5.
5	23	23	23	Lowband Filter Output	The output of the Input filter of the lowerband limit. The Rx/$\overline{\text{Tx}}$ function determines which filter is used (Filter 1 or 2). See figure 5 and figure 6. This output must be connected to the Lowband balanced modulator input via capacitor C6. See figure 6.
6	24	24	24	V_{DD}	A single 5.0V supply is required.
10, 11, 12			4, 5, 6, 7, 9	N/C	No Connection

Table 1: Signal List

	Rx/$\overline{\text{Tx}}$ = 1	Rx/$\overline{\text{Tx}}$ = 0	MUTE = 0	POWERSAVE
Rx Path	Enabled	Disabled	Disabled	Disabled
Rx Out Level	Bias	Bias	Bias	High Impedance
Tx Path	Disabled	Enabled	Disabled	Disabled
Tx Out Level	Bias	Bias	Bias	High impedance

Table 2: Functions Influencing Signal Paths

3. External Components

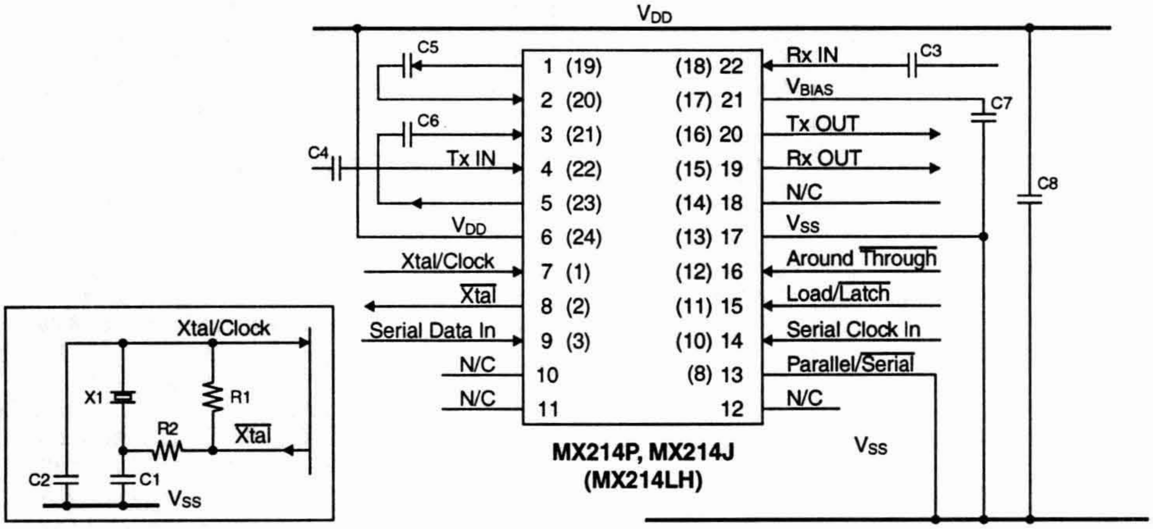

VDD
C5
C6
C4
Tx IN
VDD
Xtal/Clock
Xtal
Serial Data In
N/C
N/C
1 (19)
2 (20)
3 (21)
4 (22)
5 (23)
6 (24)
7 (1)
8 (2)
9 (3)
10
11
(18) 22
(17) 21
(16) 20
(15) 19
(14) 18
(13) 17
(12) 16
(11) 15
(10) 14
(8) 13
12
Rx IN
C3
VBIAS
C7
Tx OUT
Rx OUT
N/C
C8
VSS
Around/Through
Load/Latch
Serial Clock In
Parallel/Serial
N/C
VSS
MX214P, MX214J
(MX214LH)
Xtal/Clock
X1
R1
R2
Xtal
C2
C1
VSS

Figure 2: Recommended External Components 'MX214 Serial Loading'

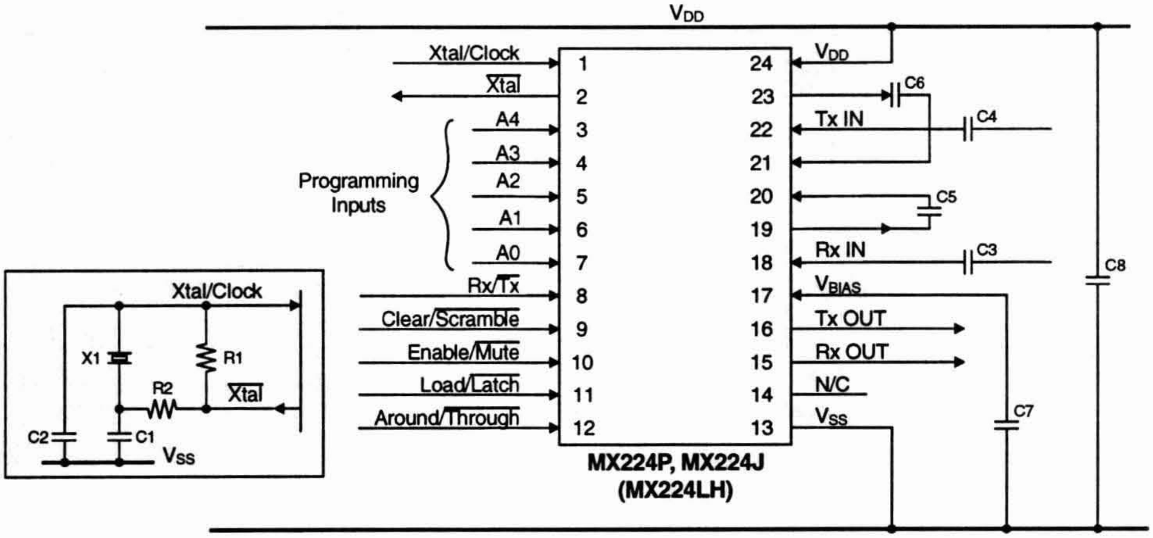

VDD
Xtal/Clock
Xtal
A4
A3
A2
A1
A0
Programming Inputs
Rx/Tx
Clear/Scramble
Enable/Mute
Load/Latch
Around/Through
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
C6
Tx IN
C4
C5
Rx IN
C3
VBIAS
C8
Tx OUT
Rx OUT
N/C
VSS
C7
MX224P, MX224J
(MX224LH)
Xtal/Clock
X1
R1
R2
Xtal
C2
C1
VSS

Figure 3: Recommended External Components 'MX224 Parallel Loading'

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
R2		Selectable	
C1		33pF	±20%
C2		68pF	±20%
C3		15nF	±20%
C4		15nF	±20%
C5	1	1.0µF	±20%
C6	1	1.0µF	±20%
C7		1.0µF	±20%
C8		1.0µF	±20%
X1	2	1MHz	

Table 3: Recommended External Components

Notes:

1. C5 and C6 are coupling capacitors between filter outputs and balanced modulator inputs.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX214/224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/224 ICs include a highpass filter that rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier generation MX204 VSB Inverter.

The MX214/224 splits the voiceband (300-2700Hz) into upper and lower subbands, and inverts each subband about itself. The 'split point' (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000Hz range. In the 'fixed code' mode, a single point is used. Fixed mode operation nets approximately 4 mutually exclusive secure channels.

In 'rolling code' mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip ' Mute' function is useful when implementing rolling code continuous synchronization schemes. 'Powersave' and 'Clear/Scramble' controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1MHz reference oscillator driven by a 1MHz crystal or clock pulse input.

5. Application

The MX214 represents both the MX214 and the MX224 throughout this section.

Recommended external components are shown in Figure 2 and Figure 3. In 'Scramble' mode, split point frequencies are selected and set in accordance with the ROM address code present at the inputs A0-A4. See Table 2. In 'Clear' mode, both upper and Lowerband filter limits are used (see Figure 5 and figure 6), the carrier frequencies are turned off, and the balanced modulators are bypassed internally. The Lowband audio is removed from the output signal prior to summing.

ROM Address A4-A0	Split Point Hz	Low Band Carrier, Hz f_{C1}	High Band Carrier, Hz f_{C2}	ROM Address A4-A0	Split Point Hz	Low Band Carrier, Hz f_{C1}	High Band Carrier, Hz f_{C2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 4: ROM Address Programming

The MUTE function disables the MX214/224's audio outputs to allow periodic transmission of synchronization data. A logic '0' at this input isolates the device while leaving the audio input and output ins at bias level (See Table 1). When the MX21/224 is in Powersave mode, audio signals may be hardwired around the device since the input and output pins are open circuit. See Table 1.

5.1 Audio Quality

Figure below shows the recommended basic audio system layout using pre- and de-emphasis circuitry to maintain good recovered speech quality. The Transmit mode, ***Do Not*** pre-emphasize the audio output of the MX214. In the Receive mode, de-emphasis should be used after the MX214.

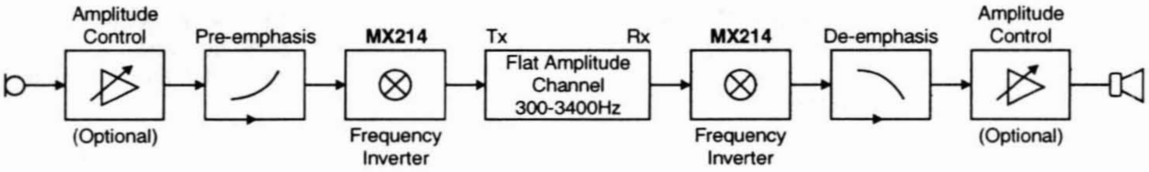


Figure 4: Recommended Basic Communication Audio System Layout

Figure ? shows the recommended basic audio system layout if it is necessary to install the MX214 within a radio having pre- and de-emphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

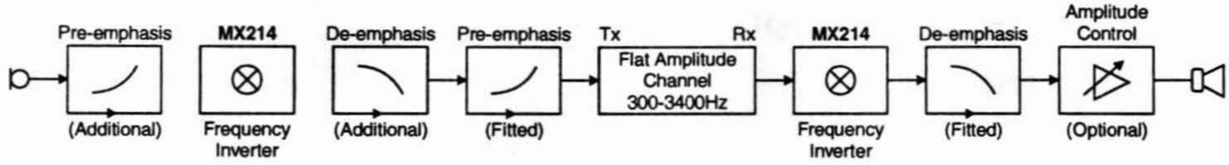

Pre-emphasis
MX214
De-emphasis
Pre-emphasis
Tx
Rx
MX214
De-emphasis
Amplitude Control
Flat Amplitude Channel 300-3400Hz
(Additional)
Frequency Inverter
(Additional)
(Fitted)
Frequency Inverter
(Fitted)
(Optional)

Figure 5: Recommended Basic Radio Communication Audio System Layout.

During the Transmit function the low pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

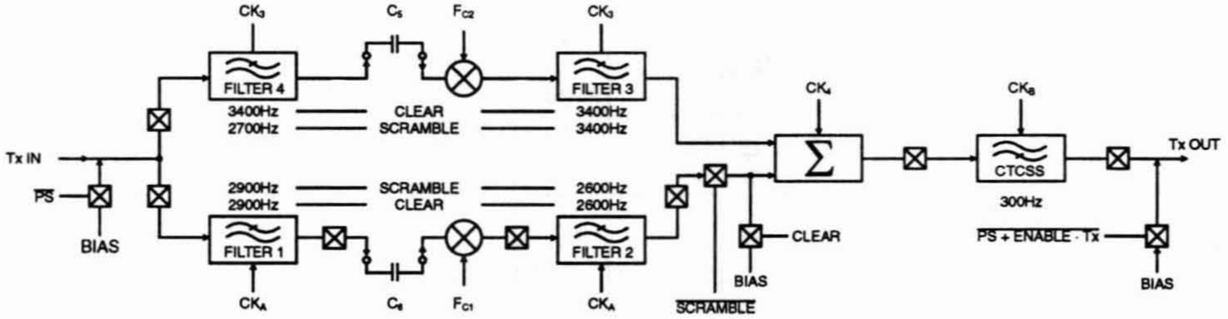

CK3
C5
FC2
CK3
FILTER 4
FILTER 3
3400Hz
2700Hz
CLEAR
SCRAMBLE
3400Hz
3400Hz
CK4
CK8
Tx IN
PS
BIAS
2900Hz
2900Hz
SCRAMBLE
CLEAR
2600Hz
2600Hz
CTCSS
300Hz
Tx OUT
FILTER 1
FILTER 2
CLEAR
PS + ENABLE · Tx
BIAS
BIAS
CKA
C6
FC1
CKA
SCRAMBLE

Figure 6: Basic Tx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

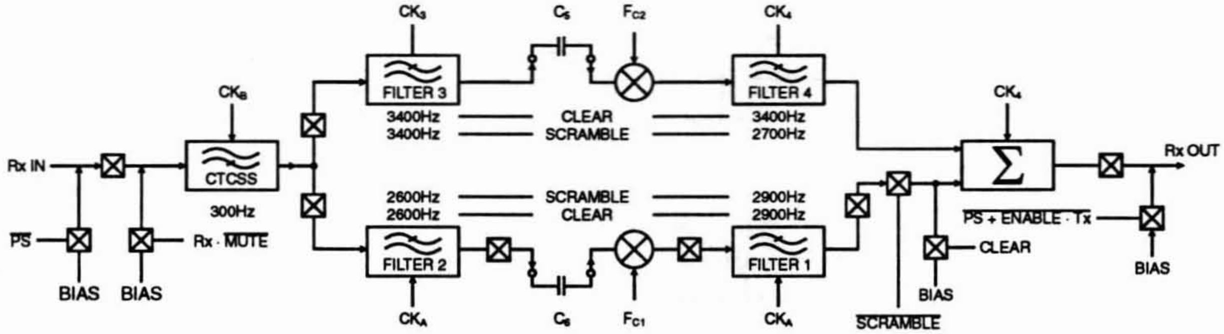

CK3
C5
FC2
CK4
CK8
FILTER 3
FILTER 4
3400Hz
3400Hz
CLEAR
SCRAMBLE
3400Hz
2700Hz
CK4
Rx IN
CTCSS
300Hz
Rx OUT
2600Hz
2600Hz
SCRAMBLE
CLEAR
2900Hz
2900Hz
PS + ENABLE · Tx
PS
Rx · MUTE
FILTER 2
FILTER 1
CLEAR
BIAS
BIAS
BIAS
BIAS
CKA
C6
FC1
CKA
SCRAMBLE

Figure 7: Basic Rx Path

6. Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
P/LH Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
J Package					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			1.0		MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB ref. = 775mV$_{RMS}$, Xtal/Clock Frequency = 1.0MHz

	Notes	Min.	Typ.	Max.	Units
Static Values					
Voltage		4.5	5.0	5.5	V
Current					
Enabled			8		mA
Powersave			1.2		mA
Analog Input Impedances					
Tx/Rx Input (Enabled)			100		kΩ
Tx/Rx Input (Powersave)		1			MΩ
Balanced Modulator			40		kΩ
Analog Output Impedances					
Rx Output (Tx Mode)			100		kΩ
Rx Output (Rx Mode)				2	kΩ
Rx Output (Powersave)		1			MΩ
Tx Output (Tx Mode)				2	kΩ
Tx Output (Rx Mode)			100		kΩ
Tx Output (Powersave)		1			MΩ
Input LPF				1	kΩ
Digital Values					
Digital Input Impedance		100			kΩ
Dynamic Values					
Input Logic '1'		3.5			V
Input logic '0'				1.5	V
Xtal/Clock Frequency			1		MHz
Analog Input Level		-18		6	dB
Carrier Breakthrough	1		-55		dB
Baseband Breakthrough	1, 2, 3		-33		dB
Filter Clock Breakthrough	1, 2, 3		-50		dB
Output Noise	1, 4		-45		dB
Passband Characteristics					
Clear Mode	7				
Passband Gain			0		dB
Output Lower 3dB Point (Rx or Tx)			300		Hz
Output Upper 3dB Point (Rx or Tx)			3400		Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6		0		dB
Received Signal Lower 3dB Point			400		Hz
Received Signal Upper 3dB Point			2700		Hz
Transmitted Signal Lower 3dB Point			300		Hz
Transmitted Signal Upper 3dB Point			3400		Hz

	Notes	Min.	Typ.	Max.	Units
CTCSS (Highpass Filter)					
-3dB Point			300		Hz
Passband gain			0		dB
Stopband Attenuation at f < 250Hz			40		dB

Operating Characteristics Notes:

1. Measured at the output of a single device.
2. Tx Mode.
3. Rx Mode.
4. With input AC short-circuited to V_{SS}.
5. Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400Hz and measured relative to the input signal at the transmitting device.
6. Excluding split point ±150Hz.
7. Measured at the Rx or Tx output pin of a single source.

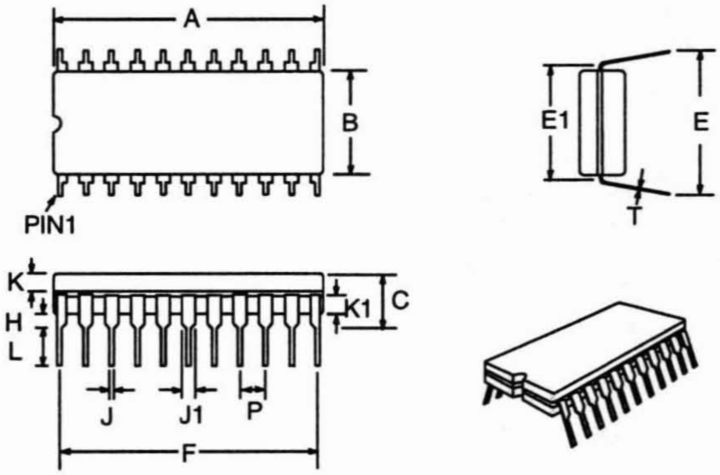
6.1.4 Timing

Timing Figure ?		Notes	Min.	Typ.	Max.	Units
Serial Mode						
t_{SMS}	Serial Mode Enable Set-Up		250			ns
t_{PWH}	Serial Clock ‘High’ Pulse Width		250			ns
t_{PWL}	Serial Clock ‘Low’ Pulse Width		250			ns
t_{DS}	Data Set Up Time		150			ns
t_{DHS}	Data Hold Time		50			ns
t_{LL}	Load/$\overline{\text{Latch}}$ Set Up Time		250			ns
t_{LLW}	Load/$\overline{\text{Latch}}$ Pulse Width		150			ns
Parallel Mode						
t_{LLW}	Load/$\overline{\text{Latch}}$ Pulse Width		150			ns
t_{DSP}	Data Set Up Time		150			ns
t_{DHP}	Data Hold Time		20			ns

Table 5: Serial and Parallel Timing

Figure 8: Loading Timing Diagram

6.2 Packages

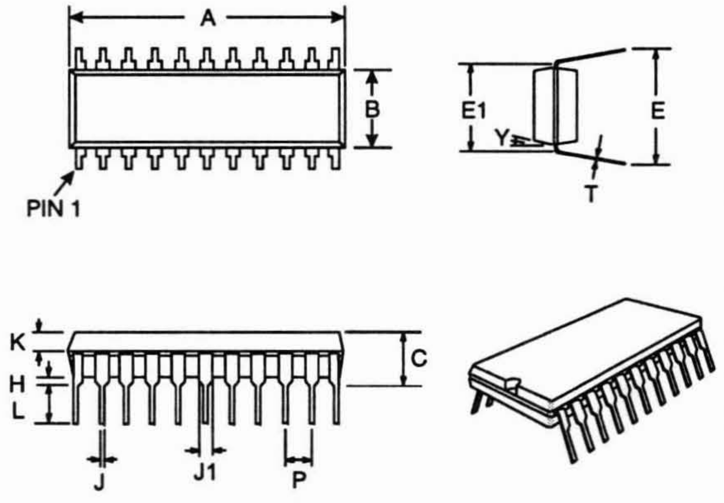


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 22-pin CDIP Mechanical Outline: ***Order as part no. MX214J or MX224J***

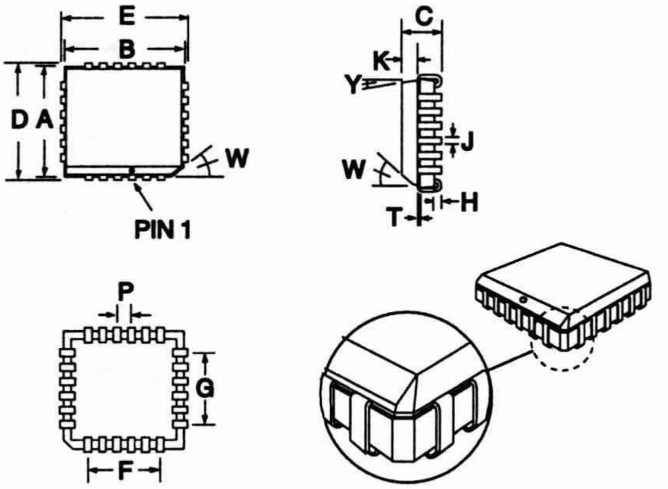


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 22-pin PDIP Mechanical Outline: ***Order as part no. MX214P or MX224P***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PLCC Mechanical Outline: ***Order as part no. MX214LH or MX224LH***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

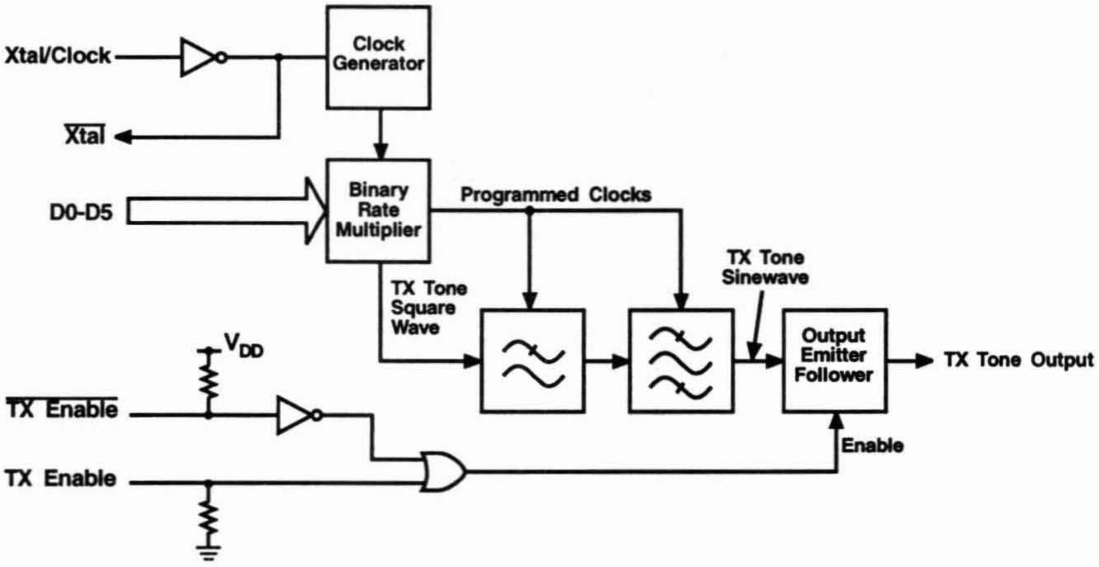
MX315A CTCSS Encoder

Features

- Field Programmable Tone Encoder
- 40 CTCSS Frequencies
- Crystal-Controlled Frequency Stability
- Low Distortion Sinewave Output
- Few External Components Required
- CMOS Low Power Requirements

Applications

- Mobile Radio Base Stations & Repeater Stations
- Mobile Radios
- Hand-Held Radios
- Industrial Controls
- Intercom Systems
- Door-Entry Systems


Xtal/Clock
Clock Generator
$\overline{\text{Xtal}}$
D0-D5
Binary Rate Multiplier
Programmed Clocks
TX Tone Sinewave
TX Tone Square Wave
V_{DD}
Output Emitter Follower
TX Tone Output
$\overline{\text{TX Enable}}$
TX Enable
Enable

The MX315A is a monolithic CMOS tone encoder for sub-audible tone squelch systems, which provides three additional frequencies over the earlier MX315A. These frequencies are 69.3, 97.4 and 206.5Hz. The tone frequencies are derived from an input reference frequency. An on-chip inverter is provided to drive an external crystal circuit.

Tone selection is achieved through six programming inputs and two control inputs (which allow either a logic "1" or "0" to enable the device). A low distortion sinewave is generated at the TX Tone Output when the MX315A is enabled. The emitter follower output stage can source 1mW directly into a 600Ω load (0dBm).

The MX315A is available in the following package styles: 16-pin SOIC (MX315ADW), 14-pin PDIP (MX315AP) and 14-pin CDIP (MX315AJ).

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

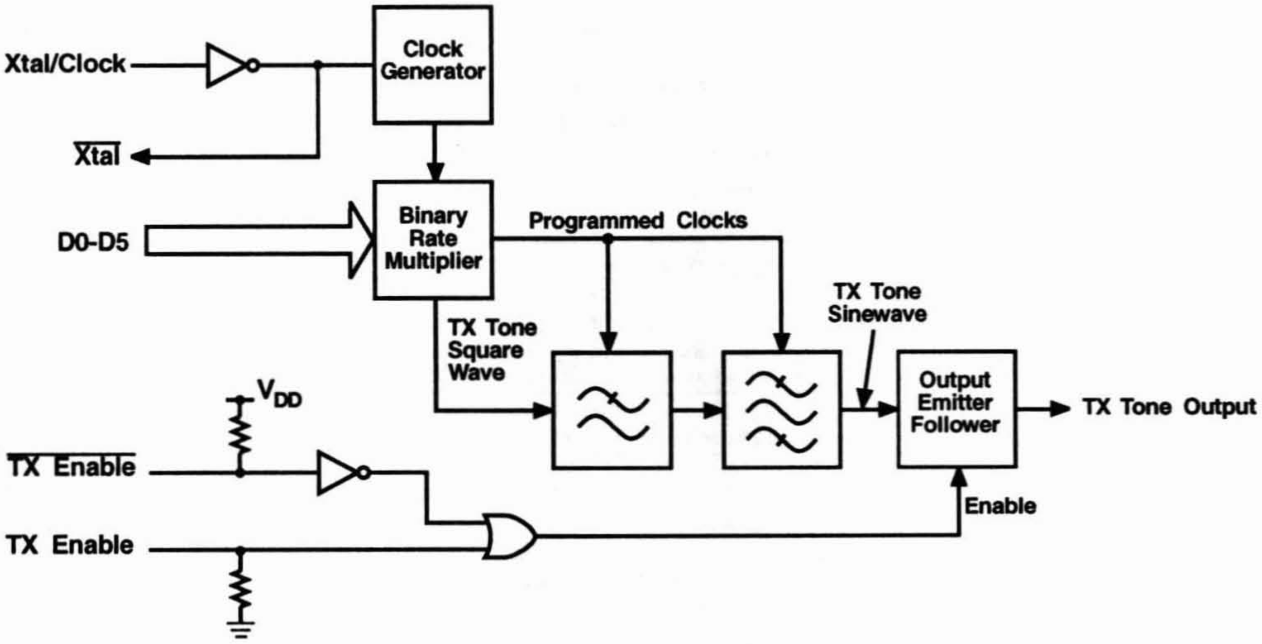

Xtal/Clock
Xtal
Clock Generator
D0-D5
Binary Rate Multiplier
Programmed Clocks
TX Tone Square Wave
TX Tone Sinewave
Output Emitter Follower
TX Tone Output
V_{DD}
$\overline{\text{TX Enable}}$
TX Enable
Enable

Figure 1: Device Block Diagram

2. Signal List

Pin No.		Name	Description
J,P	DW		
1	1	D3	D0-D5 are tone select inputs with internal pull-up resistors. The logic combination at these inputs determines the encoded CTCSS tone. See Table 1. The input sequence is not latched and may be changed at any time. A logic "1" will be programmed if the input is open circuit, allowing the use of SPST switches.
2	2	D2	
3	3	D1	
4	4	D0	
5	5	D4	
6	6	D5	
7	7	V_{SS}	Negative Supply Voltage.
8	8	Xtal/Clock In	This is the input to the CMOS inverter. It can be used in conjunction with the Xtal output to form the active element in a crystal oscillator circuit. Alternatively, a logic level 1MHz frequency can be injected at this pin. However, the supply voltage should never be applied without the input clock signal.
9	9	$\overline{\text{Xtal}}$ Output	This is the output of the CMOS inverter. When used as a crystal oscillator, track lengths and loading of this pin should be minimized.
10	10	Internal Connection	Do not use
	11	N/C	
	12	N/C	
11	13	TX Tone Output	This is the tone output pin. It includes a low impedance emitter follower stage for sourcing sinusoidal tone. The tone is generated about a DC level of approximately 1/2 V_{DD}. The pin is high impedance when not encoding.
12	14	$\overline{\text{TX Enable}}$ Input	This logic input has an internal pull-up resistor. A logic "0" at this pin enables the MX315A.
13	15	TX Enable Input	This logic input has an internal pull-down resistor. A logic "1" at this pin enables the MX315A.
14	16	V_{DD}	Positive Supply Voltage.

Table 1: Signal List

3. External Components

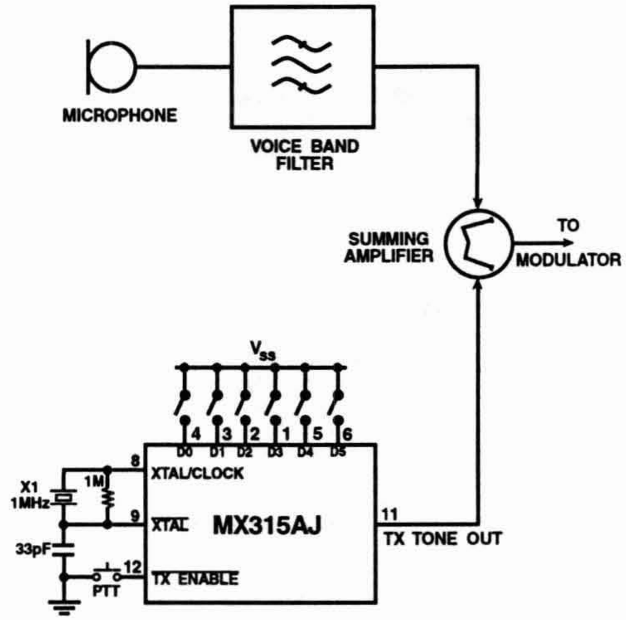

MICROPHONE
VOICE BAND FILTER
SUMMING AMPLIFIER
TO MODULATOR
V_{SS}
4
3
2
1
5
6
D0
D1
D2
D3
D4
D5
8
XTAL/CLOCK
X1
1MHz
1M
9
XTAL
MX315AJ
11
TX TONE OUT
33pF
12
TX ENABLE
PTT

Figure 2: External Components

R1	Note 1	1M	±20%
C1		33pF	±20%
X1	Note 2, 3	1MHz	±0.19%

Table 2: Recommended External Components

Notes:

1. The 1MΩ resistor is used to bias the internal CMOS inverter into its linear mode. A tolerance of ±20% is acceptable.
2. "X1" is a parallel resonant crystal. A reference frequency of 1 MHz ±0.19% is required to maintain a tone accuracy within 0.5%.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. Application

The MX315A is dedicated to Continuous Tone-controlled Squelch Systems (CTCSS) in radio applications. However, it can be used wherever encoding of low-frequency tones is required, such as intercoms, door-entry systems and various industrial applications.

The performance of a CTCSS system can be degraded if speech frequencies in the signaling spectrum are not removed prior to transmission. This can be accomplished by filtering the microphone signals to attenuate frequencies below 250 Hz. Figure 2 illustrates the addition of TX Tone Output to the filtered microphone signals prior to modulation. Figure 3 illustrates the TX Tone Output sequence and a typical spectral analysis.

Where two or more circuits are required to use a single oscillator (i.e. repeater applications), the signal at $\overline{\text{Xtal}}$ can be used to drive one additional Xtal/Clock input. Any further circuits can be driven from the buffered $\overline{\text{Xtal}}$ output of the second device.

The program code can be set on the D0-D5 inputs by hardwired logic levels or SPST switches to V_{SS}, as illustrated in Figure 2 (allowing the internal pull-up resistors to program a logic "1").

The MX315A provides both a $\overline{\text{TX Enable}}$ input and a TX Enable input. Either input can be used to enable the tone output, with the unused pin left open circuit (internal resistors establish a valid logic level and prevent damage). Any configuration of PTT switch or TX signal can therefore be interfaced.

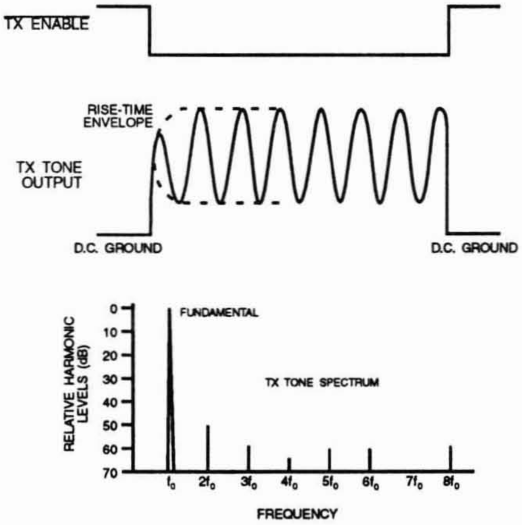


Figure 3: Tone Encoding Sequence and Spectral Response

4.1 Interfacing and Electromagnetic Capability

The MX315A requires a clock of 1MHz, which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 1MHz or its harmonics.

A decoupling capacitor can be used to reduce ripple on the power supply. This will reduce the level of superimposed noise on the supply caused by internal switching transients (particularly at 1MHz and f_0).

4.2 CTCSS Programming

Tone			Programming Inputs						
Nominal Frequency (Hz)	MX315A Freq. (Hz)	Δfo (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	67.06	+.10	1	1	1	1	1	1	3F
69.3	69.37	+.10	1	1	1	0	0	1	39
71.9	71.84	-.08	0	1	1	1	1	1	1F
74.4	74.33	-.10	1	1	1	1	1	0	3E
77.0	76.99	-.02	0	0	1	1	1	1	0F
79.7	79.65	-.06	1	1	1	1	0	1	3D
82.5	82.50	0.0	0	1	1	1	1	0	1E
85.4	85.34	-0.7	1	1	1	1	0	0	3C
88.5	88.62	+.14	0	0	1	1	1	0	0E
91.5	91.38	-.13	1	1	1	0	1	1	3B
94.8	94.88	+.08	0	1	1	1	0	1	1D
97.4	97.46	+.06	1	1	1	0	1	0	3A
100.0	99.87	-.13	0	0	1	1	0	1	0D
103.5	103.39	-.11	0	1	1	1	0	0	1C
107.2	107.17	-.03	0	0	1	1	0	0	0C
110.9	110.85	-.04	0	1	1	0	1	1	1B
114.8	114.80	0.0	0	0	1	0	1	1	0B
118.8	118.60	-.17	0	1	1	0	1	0	1A
123.0	123.12	+.10	0	0	1	0	1	0	0A
127.3	127.50	+.16	0	1	1	0	0	1	19
131.8	131.67	-.10	0	0	1	0	0	1	09
136.5	136.69	+.14	0	1	1	0	0	0	18
141.3	141.48	+.13	0	0	1	0	0	0	08
146.2	145.96	-.16	0	1	0	1	1	1	17
151.4	151.45	+.03	0	0	0	1	1	1	07
156.7	156.59	-.07	0	1	0	1	1	0	16
162.2	162.10	-.06	0	0	0	1	1	0	06
167.9	168.01	+.07	0	1	0	1	0	1	15
173.8	173.43	-.21	0	0	0	1	0	1	05
179.9	180.21	+.17	0	1	0	1	0	0	14
186.2	186.46	+.14	0	0	0	1	0	0	04
192.8	193.16	+.19	0	1	0	0	1	1	13
203.5	202.88	-.31	0	0	0	0	1	1	03
206.5	206.78	+.14	1	1	1	0	0	0	38
210.7	210.84	+.07	0	1	0	0	1	0	12
218.1	217.96	-.07	0	0	0	0	1	0	02
225.7	225.58	-.05	0	1	0	0	0	1	11
233.6	233.75	+.07	0	0	0	0	0	1	01
241.8	242.54	+.31	0	1	0	0	0	0	10
250.3	250.06	+.10	0	0	0	0	0	0	00
Test	4032	0.0	1	1	0	0	1	1	*33

* - or any invalid address

Table 3: CTCSS Tones

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0	V
J / P /DW Packages			
Total Allowable Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature	-30	+85	°C
Storage Temperature	-55	+125	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
V_{DD}		4.5	5.0	5.5	V
Operating Temperature		-30		85	°C
Clock	Note 1		1		MHz

Operating Limits Note:

1. "X1" is a parallel resonant crystal. A reference frequency of 1 MHz ±0.19% is required to maintain a tone accuracy within 0.5%.

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V , T_{AMB} = 25°C, Xtal Frequency = 1MHz

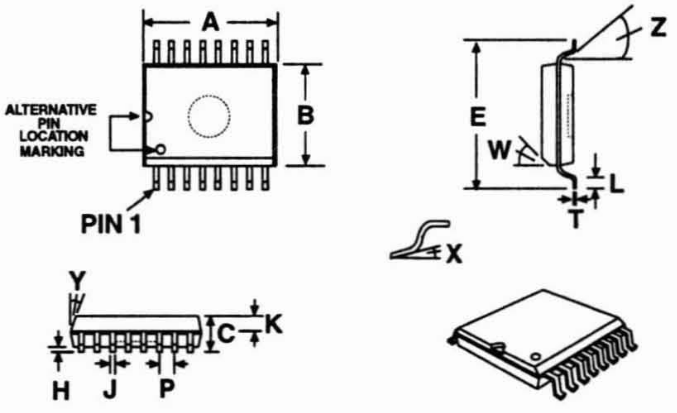
	Notes	Min.	Typ.	Max	Units
Supply Current (operating)			1.5	4.5	mA
Input Impedance	1		500		kΩ
Input Impedance	2		10		MΩ
Logic Input "1"		3.5			V
Logic Input "0"				1.5	V
TX Output EMF	3	550	775		mV_{RMS}
TX Risetime			1		ms
TX Tone Output Load Current				5	mA
TX Distortion	3		2	5	%
Variation in Output Level Between Tones	3		0.1		dB

Operating Characteristics Notes:

1. Refers to D0, D1, D2, D3, D4, D5, TX Enable and $\overline{\text{TX Enable}}$ inputs
2. Refers to Xtal/Clock input

3. Any program tone and $R_L = 600\Omega$, $C_L = 15pF$. THD measurements are taken in the 0-6 kHz bandwidth.

5.2 Packaging

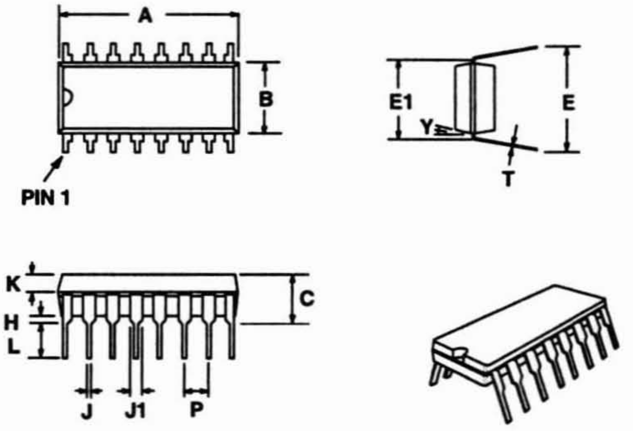


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 4: 16-pin SOIC Mechanical Outline: Order as part no. MX315ADW

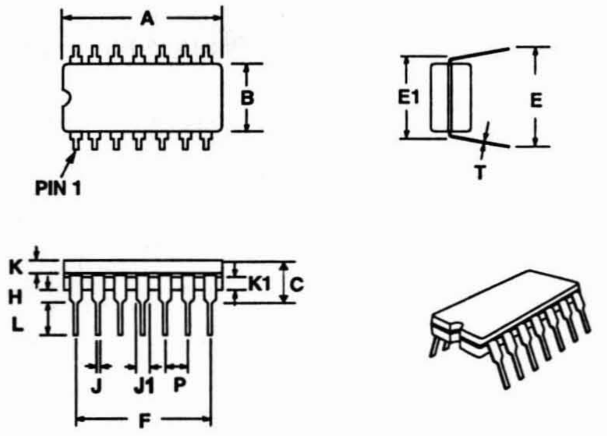


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin PDIP Mechanical Outline: Order as part no. MX315AP



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.754 (19.15)		0.766 (19.46)
B	0.240 (6.10)		0.288 (7.32)
C	0.165 (4.19)		0.230 (5.84)
E	0.360 (9.14)		0.420 (10.67)
E1	0.305 (7.75)		0.315 (8.00)
F		0.600 (15.24)	
H		0.015 (0.38)	
J		0.018 (0.46)	
J1		0.060 (1.52)	
K	0.053 (1.35)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T		0.010 (0.254)	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin CDIP Mechanical Outline: Order as part no. MX315AJ

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX375

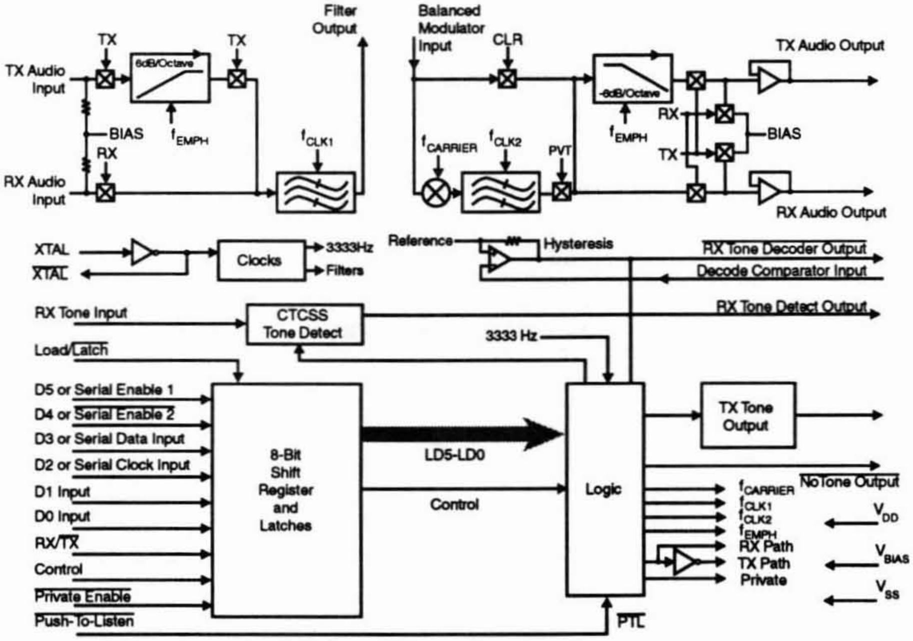
Pvt SQUELCH™ CTCSS Encoder/Decoder

Features

- PRIVATE/CLEAR CAPABILITY
- ON-CHIP TX AUDIO PRE/DEEMPHASIS
- ALTERNATIVE TO STANDARD CTCSS "PARTY LINE"
- POWERSAVE OPTION

Applications

- MOBILE RADIOS
- COMMUNITY REPEATERS
- TELEPHONE/RADIO INTERCONNECT SYSTEMS


TX Audio Input
TX
6dB/Octave
TX
Filter Output
BIAS
RX
f_{EMPH}
f_{CLK1}
RX Audio Input
Balanced Modulator Input
CLR
$f_{CARRIER}$
f_{CLK2}
PVT
-6dB/Octave
f_{EMPH}
RX
TX
BIAS
TX Audio Output
RX Audio Output
XTAL
XTAL
Clocks
3333Hz
Filters
Reference
Hysteresis
RX Tone Decoder Output
Decode Comparator Input
RX Tone Input
CTCSS Tone Detect
RX Tone Detect Output
3333 Hz
Load/Latch
D5 or Serial Enable 1
D4 or Serial Enable 2
D3 or Serial Data Input
D2 or Serial Clock Input
D1 Input
D0 Input
RX/TX
Control
Private Enable
Push-To-Listen
8-Bit Shift Register and Latches
LD5-LD0
Control
Logic
TX Tone Output
NoTone Output
$f_{CARRIER}$
f_{CLK1}
f_{CLK2}
f_{EMPH}
RX Path
TX Path
Private
V_{DD}
V_{BIAS}
V_{SS}
PTL

The MX375 is a CMOS LSI microcircuit which combines CTCSS Encode/Decode operation with voice band frequency inversion. Frequency inversion is achieved by modulating the input audio with a 3333 Hz carrier frequency. Higher voice band frequencies are translated downward, and lower frequencies upward, resulting in a "mirror image" voice transmission. *Pvt*SQUELCH™ combines CTCSS with inverted speech to prevent users from understanding each other's communications unless the transmissions are accompanied by the group's assigned tone. Its net effect is to eliminate casual eavesdropping and give mobile radio users a certain degree of privacy at a minimal price. Up to 38 *Pvt*SQUELCH user groups (one per CTCSS tone) can share a single radio channel. With *Pvt*SQUELCH, competing businesses can share a radio channel without compromising communications security.

Device features: 1) serial or parallel tone programming capability (serial or parallel offered on MX375J, P & LH8), 2) the ability to operate under NOTONE conditions, 3) on-chip Tx and Rx audio filtering, 4) pin-selectable Private/Clear operation, and 5) pre/deemphasis filters in the Tx path, for optimal recovered audio quality.

A low-cost 4 MHz crystal/clock and a single 5V supply are required for operation. The MX375 is available in the following package styles: 28-pin PDIP (MX375P), 28-pin CDIP (MX375J) 28-pin PLCC (MX375LH8), and 24-pin PLCC (MX375LH).

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1. Block Diagram

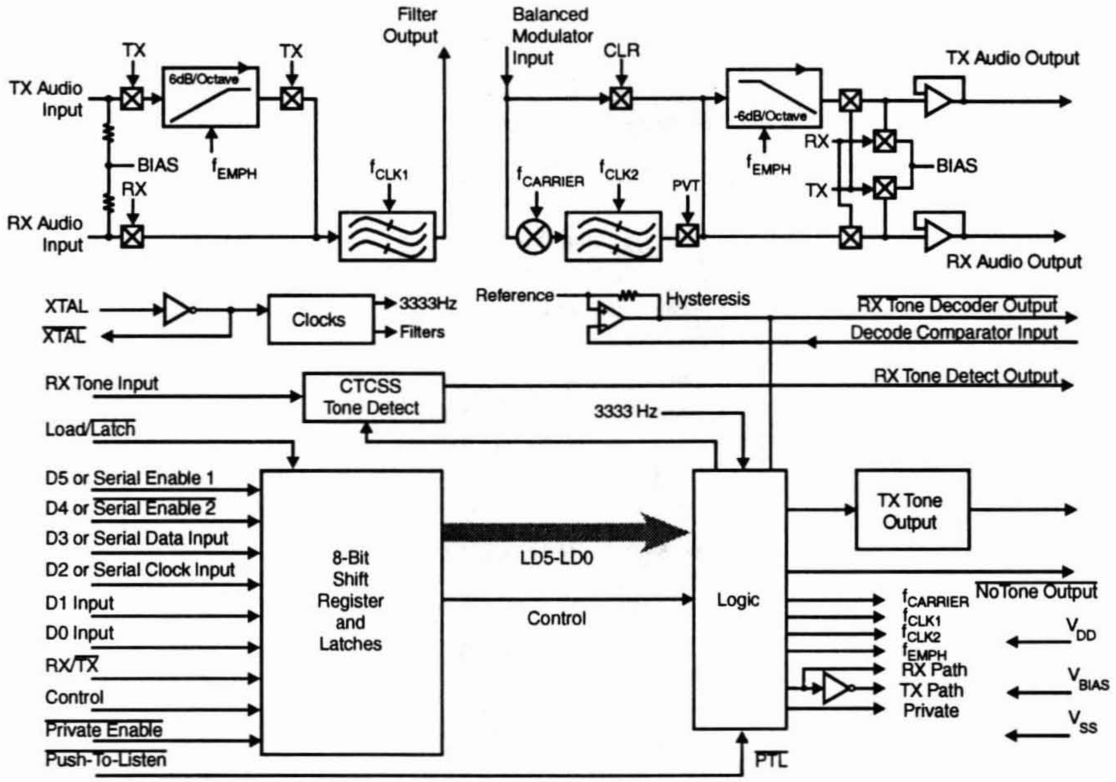

TX Audio Input
TX
6dB/Octave
TX
Filter Output
Balanced Modulator Input
CLR
TX Audio Output
-6dB/Octave
BIAS
f_{EMPH}
f_{CLK1}
$f_{CARRIER}$
f_{CLK2}
PVT
f_{EMPH}
RX
TX
BIAS
RX
RX Audio Input
RX Audio Output
XTAL
$\overline{XTAL}$
Clocks
3333Hz
Filters
Reference
Hysteresis
$\overline{RX Tone Decoder Output}$
Decode Comparator Input
RX Tone Input
CTCSS Tone Detect
RX Tone Detect Output
3333 Hz
Load/$\overline{Latch}$
D5 or $\overline{Serial Enable 1}$
D4 or $\overline{Serial Enable 2}$
D3 or Serial Data Input
D2 or Serial Clock Input
D1 Input
D0 Input
RX/$\overline{TX}$
Control
$\overline{Private Enable}$
$\overline{Push-To-Listen}$
8-Bit Shift Register and Latches
LD5-LD0
Control
Logic
TX Tone Output
$\overline{NoTone Output}$
$f_{CARRIER}$
f_{CLK1}
f_{CLK2}
f_{EMPH}
RX Path
TX Path
Private
V_{DD}
V_{BIAS}
V_{SS}
$\overline{PTL}$

Figure 1: Device Block Diagram

2. Signal List

Pin No.		Name	Type	Description
LH	J,P,LH8			
1	28	V_{DD}	power	5V supply pin.
2	1	XTAL/CLOCK	input	This is the input to the clock oscillator inverter. An external 4 MHz Xtal or clock input should be applied to this pin.
3	2	$\overline{\text{XTAL}}$	output	This is the 4 MHz output of the clock oscillator inverter.
4	3	LOAD / $\overline{\text{LATCH}}$	input	This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$, and D0-D5, as detailed in Table 5. Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{PrivateEnable}}$ inputs can be addressed separately by setting the Load/$\overline{\text{Latch}}$ and Control inputs as shown in Table 5. 1 MΩ pullup.
5-7		D4-D2	input	Programming Inputs (Serial Mode Only): These are the $\overline{\text{RX}}$/TX tone programming and function inputs which enable the serial programming mode. With Load/$\overline{\text{Latch}}$ at logic "0" serial data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input "0 - 1 - 0" (See Figure 5). Pin 5 (D4) = $\overline{\text{Serial Enable2}}$ Pin 6 (D3) = Serial Data Input Pin 7 (D2) = Serial Clock Input
	4-9	D5-D0	input	Parallel Programming Inputs: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which select the CTCSS tone (See Table 4). *For both Serial and Parallel Modes:* In RX, a NOTONE program enables RX Audio Output and forces the RX Tone Decode Output to a logic "0". In TX, a NOTONE program generates a constant V_{BIAS}-0.7V condition at the TX Tone Output pin. Each input has a 1 MΩ pullup resistor.
8	10	$\overline{\text{RX TONE}}$ $\overline{\text{DECODE}}$	output	The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX, this output is held at logic "1".
9	11	DECODE COMPARATOR	input	The voltage level at this pin is compared internally with a fixed reference level. A greater input level compared to the reference will result in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C10, R2, R3, and D1 (see Figure 2).
10	12	RX TONE DETECT	output	In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C10, R2, R3, and D1 (see Figure 2).
N/A	13	NOTONE	output	This pin outputs a logic "0" when a Notone CTCSS code has been programmed in RX. It is typically used to enable carrier squelch circuits under Notone RX conditions.
11	14	V_{SS}	power	The negative supply pin (ground).
12	15	TX TONE OUTPUT	output	The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 4); if NOTONE is programmed, the output is at Vbias-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.

Pin No.		Name	Type	Description
LH	J,P,LH8			
13	16	V_{BIAS}		This pin is set internally to $V_{DD}/2$. It must be externally decoupled using a capacitor (C7) to V_{SS}. See Figure 2.
14	17	FILTER OUTPUT	output	This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C4. See Figure 2.
15	18	BALANCED MODULATOR INPUT	input	This is the input to the balanced modulator. Must be A.C. coupled to the Filter Output via capacitor C4. See Figure 2.
16	19	RX AUDIO OUTPUT	output	Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in TX.
17	20	TX AUDIO OUTPUT	output	Outputs the transmitted audio in TX. In RX, this pin is held at V_{BIAS}.
18	21	RX AUDIO INPUT	input	The audio input for the RX mode. Input signals should be AC coupled via external capacitor C6. See Figure 2
19	22	TX AUDIO INPUT	input	This is the TX Audio voice input. Signals should be AC coupled via external capacitor C11. See Figure 2
20	23	$\overline{\text{PTL}}$	input	The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 5).
21	24	CONTROL		This input, together with Load/$\overline{\text{Latch}}$, selects the operational mode of the RX/$\overline{\text{TX}}$ and $\overline{\text{PrivateEnable}}$ functions. See Table 5
22	25	RX/$\overline{\text{TX}}$	input	This input selects the RX or TX mode (RX = 1, TX = 0). This can be loaded in Serial or Parallel modes as described in Table 5
23	26	$\overline{\text{PRIVATE}}$ $\overline{\text{ENABLE}}$		This input selects either Private or Clear mode (Clear = 1, Private = 0), and can be loaded by Serial or Parallel modes as described in Table 5. This input has an internal 1 MΩ pullup resistor.
24	27	RX TONE INPUT	input	This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C5.

Note: The MX375LH package is available in serial mode only.

Table 1: Signal List

3. External Components

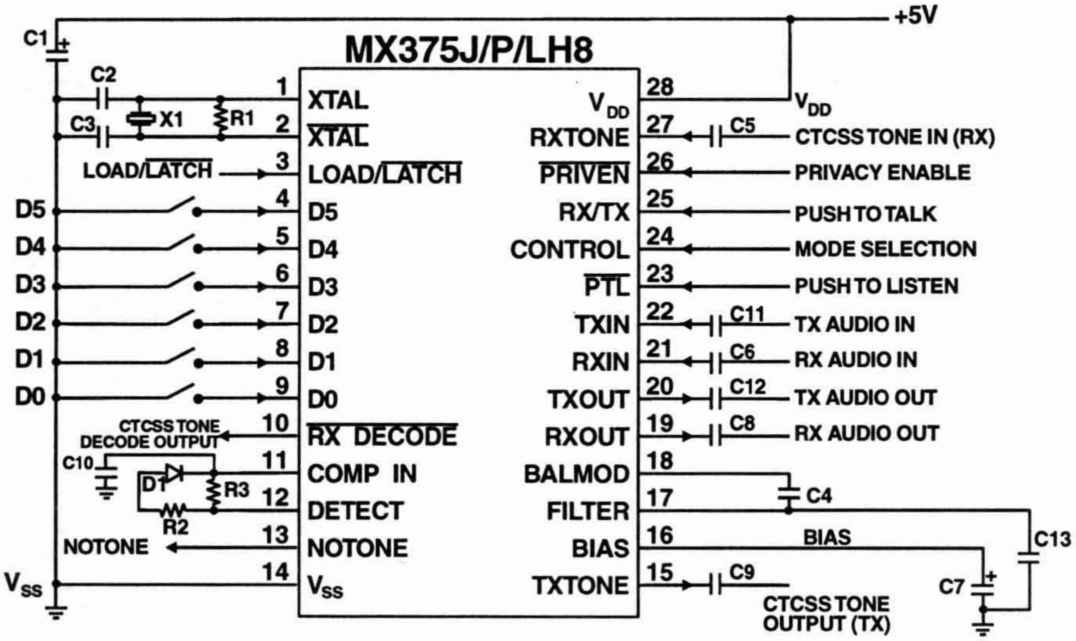

+5V
MX375J/P/LH8
C1
C2
C3
X1
R1
1 XTAL
2 XTAL
3 LOAD/LATCH
LOAD/LATCH
D5 4 D5
D4 5 D4
D3 6 D3
D2 7 D2
D1 8 D1
D0 9 D0
CTCSS TONE DECODE OUTPUT 10 RX DECODE
C10 11 COMP IN
D1
R3
R2 12 DETECT
NOTONE 13 NOTONE
V_{SS} 14 V_{SS}
28 V_{DD} — V_{DD}
27 RXTONE — C5 — CTCSS TONE IN (RX)
26 PRIVEN — PRIVACY ENABLE
25 RX/TX — PUSH TO TALK
24 CONTROL — MODE SELECTION
23 PTL — PUSH TO LISTEN
22 TXIN — C11 — TX AUDIO IN
21 RXIN — C6 — RX AUDIO IN
20 TXOUT — C12 — TX AUDIO OUT
19 RXOUT — C8 — RX AUDIO OUT
18 BALMOD
C4
17 FILTER
16 BIAS — BIAS
C13
15 TXTONE — C9 — CTCSS TONE OUTPUT (TX)
C7

Figure 2: Recommended External Components

R1		1MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
X1	Note 1, 2	4MHz	
C1		1.0µF	±20%
C2		33pF	±20%
C3		33pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±20%

C6		0.1µF	±20%
C7		1.0µF	±20%
C8		0.1µF	±20%
C9		0.1µF	±20%
C10		0.1µF	±20%
C11		0.1µF	±20%
C12		0.1µF	±20%
C13		0.001µF	±20%
D1		small signal	

Table 2: Recommended External Components

Recommended External Components Note:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. XTAL - At cut, fundamental, parallel resonant 20pF load capacitance, 0.05% tolerance

4. General Description

4.1.1 Pre- and De-emphasis

Pre- and De-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

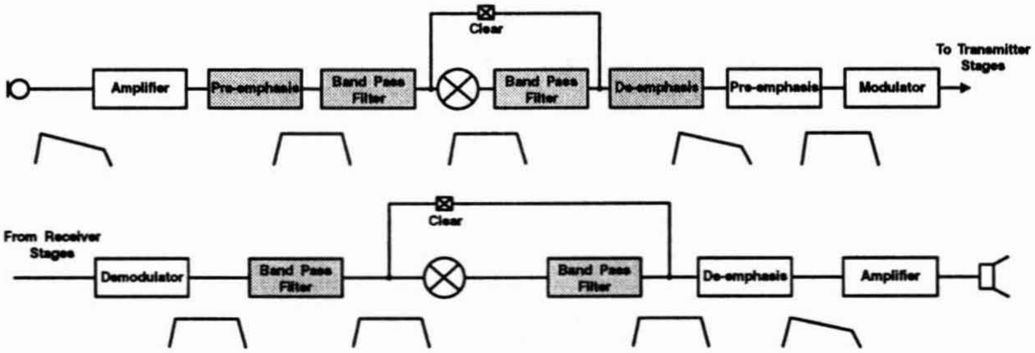

Clear
To Transmitter Stages
Amplifier
Pre-emphasis
Band Pass Filter
Band Pass Filter
De-emphasis
Pre-emphasis
Modulator
Clear
From Receiver Stages
Demodulator
Band Pass Filter
Band Pass Filter
De-emphasis
Amplifier

Figure 3: Transmit and Receive Paths

4.1.2 Functions and Outputs

D0-D5	Notone	RX/TX	PRIVATE ENABLE	PTL	RX TONE DETECT	RX TONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
Tone	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
Tone	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
Notone	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
Notone	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
Tone	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
Tone	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
Notone	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
Notone	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

Table 3: Functions and Outputs

Note:

1. Algebraic functions:
   RX Path On = RX × (PTL + RX Tone Decoder)
   Clear Path = Notone + Private Enable + (PTL × RX × RX Tone Decoder)
   Notone (D0 - D5) = 000011
   Carrier Frequency = 3333Hz During inverted Path (TX or RX)
2. The Pre- and De-emphasis circuits remain in the transmit path in both the Clear and Invert Modes.
3. Power remains applied to the CTCSS tone decoder at all times.
4. During clear operation the carrier frequency is turned off to reduce spurious emissions.

5. Application

5.1.1 CTCSS Programming

Nominal Frequency(Hz)	Frequency(Hz)	ΔF_0 (%)	Program Inputs					
			D5	D4	D3	D2	D1	D0
67.0	67.05	+0.07	1	1	1	1	1	1
71.9	71.9	0	0	1	1	1	1	1
74.4	74.35	-0.07	1	1	1	1	1	0
77.0	76.96	-0.5	0	0	1	1	1	1
79.7	79.77	+0.09	1	1	1	1	0	1
82.5	82.59	+0.1	0	1	1	1	1	0
85.4	85.38	-0.2	1	1	1	1	0	0
88.5	88.61	+0.13	0	0	1	1	1	0
91.5	91.58	+0.09	1	1	1	0	1	1
94.8	94.76	-0.04	0	1	1	1	0	1
97.4	97.29	-0.11	1	1	1	0	1	0
100.0	99.96	-0.04	0	0	1	1	0	1
103.5	103.43	-0.07	0	1	1	1	0	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	0	1	1	0	1	1
114.8	114.64	-0.14	0	0	1	0	1	1
118.8	118.8	0	0	1	1	0	1	0
123.0	122.8	-0.17	0	0	1	0	1	0
127.3	127.08	-0.17	0	1	1	0	0	1
131.8	131.67	-0.10	0	0	1	0	0	1
136.5	136.61	+0.08	0	1	1	0	0	0
141.3	141.32	+0.02	0	0	1	0	0	0
146.2	146.37	+0.12	0	1	0	1	1	1
151.4	151.09	-0.2	0	0	0	1	1	1
156.7	156.88	+0.11	0	1	0	1	1	0
162.2	162.31	+0.07	0	0	0	1	1	0
167.9	168.14	+0.14	0	1	0	1	0	1
173.8	173.48	-0.19	0	0	0	1	0	1
179.9	180.15	+0.14	0	1	0	1	0	0
186.2	186.29	+0.05	0	0	0	1	0	0
192.8	192.86	+0.03	0	1	0	0	1	1
203.5	203.65	+0.07	0	0	0	0	1	1
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	0	0	0	1	0
225.7	226.12	+0.18	0	1	0	0	0	1
233.6	234.19	+0.25	0	0	0	0	0	1
241.8	241.08	-0.30	0	1	0	0	0	0
250.3	250.28	-0.01	0	0	0	0	0	0
Notone			1	1	0	0	0	0

Table 4: CTCSS Programming

(A) Explanation of Load/Latch function in Serial and Parallel Modes		
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Result**
Parallel	1	Transparent, the data acts directly
Parallel	1 - 0	Latches present data in
Parallel	0	No further changes except to allow serial mode selection
Serial (data loading)	0	No change while serial data train is loaded
Serial (data loaded)	0 - 1 - 0	Loaded serial data is latched

(B) Explanation of Control Input			
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Control**	**RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$**
Parallel	0	0	Latched
Parallel	1	0	Transparent
Parallel	X	1	Transparent
Serial	0 - 1 - 0	0	Serial Load
Serial	X	1	Transparent

Table 5: Load/$\overline{\text{Latch}}$ and Control Input Function

Notes:

1. "0 - 1 - 0" is a strobe pulse as shown in Figure 4 and Figure 5.
2. "X" denotes any logical state.

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Typ.	Max.	Units
Supply Voltage	-0.3		7.0	V
Input Voltage at any pin	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
J / P / LH / LH8 Packages				
Total Device Dissipation at T_{AMB} 25°C			800	mW
Derating above 25°C			10	mW/°C above 25°C
Operating Temperature	-40°		85°	C
Storage Temperature	-55°		125°	C

Table 6: Absolute Maximum Ratings

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal/Clock Frequency			4.0		MHz

Table 7: Operating Limits

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C, XTAL = 4.0MHz, Audio level)dB ref. = 300mV_{RMS}, Composite input signal = 0dB, 1 kHz tone in, -12dB (6kHz band limited) Gaussian white noise with a -20dB CTCSS tone.

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX (Private)				15.0	mA
TX (Operating)				12.0	mA
RX (Operating)				7.0	mA
Analog Input Impedance			0.5		MΩ
Analog Output Impedance			0.5		kΩ
Tone Input Impedance			0.5		MΩ
Input Logic "1"		3.5			V
Input Logic "0"				1.5	V
Output Logic "1" (I=-0.1mA)		4.0			V
Output Logic "0" (I=-0.1mA)				1.0	V
Dynamic Values					
Decoder					
Input Signal Level	1,4	-20			dB
Response Time	1,4,6			250	ms
Deresponse Time	1,4,6			250	ms
Selectivity	4	±0.5		±3.0	%f_0
Encoder					
Tone Output Level (775mV_{RMS} ref.)		-3.0	0	3.0	dB
Tone Frequency Accuracy		-0.3		0.3	%f_0
Tone Harmonic Distortion			2.0	5.0	%
Tone Output Load Current	2			5.0	mA
Output Level Variation between Tones	9	-1.0		1.0	dB
Risetime (to 90% nominal level)					
(f_0>100 Hz)	5		15		ms
(f_0<100 Hz)	5		45		ms

	Notes	Min.	Typ.	Max	Units
RX Clear					
Total Harmonic Distortion	3		2	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3	-1	0	1	dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
RX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough	3		-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3000Hz)	3		-	4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)			-60		dB
TX Clear					
Total Harmonic Distortion	3		3	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3		0		dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
TX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough			-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3033Hz)	3,8			4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)	8		-60		dB

Table 8: Operating Characteristics

Operating Characteristics Notes:

1. These values are obtained using the external integrating components given in Figure 2.
2. An emitter follower output
3. With an input signal of 1 kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with R_L=600 Ω, C_L=15pF, including any response to a phase reversal instruction.
6. f_0 > 100 Hz, (for 100Hz > f_0 > 67Hz: t = [100/f_0(Hz)] x 250ms).
7. Input ac short-circuit, audio path enabled.
8. Due to frequency inversion, these figures reflect the difference from the ideal response.
9. Reference 156.7 Hz (MX175 and MX275).

6.2 Timing Information

6.2.1 Serial Loading

	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Table 9: Serial Loading Timing Information

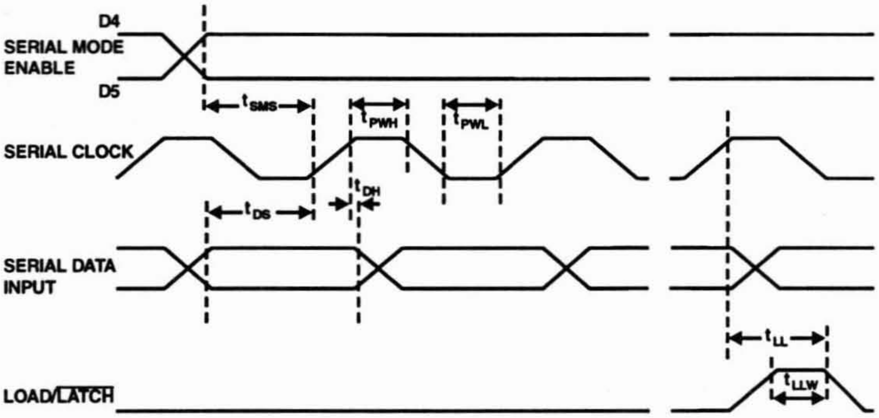

D4
SERIAL MODE ENABLE
D5
t_{SMS}
t_{PWH}
t_{PWL}
SERIAL CLOCK
t_{DH}
t_{DS}
SERIAL DATA INPUT
t_{LL}
t_{LLW}
LOAD/$\overline{\text{LATCH}}$

Figure 4: Serial Loading Timing

6.2.2 Parallel Loading

	Min.	Typ.	Max.	Unit
Data Valid Time (t_{VP})	200			ns
Load Time (t_L)	150			ns
Fall Time (t_F)			50	ns
Data Hold Time (t_H)	50			ns

Table 10: Parallel Loading Timing Information

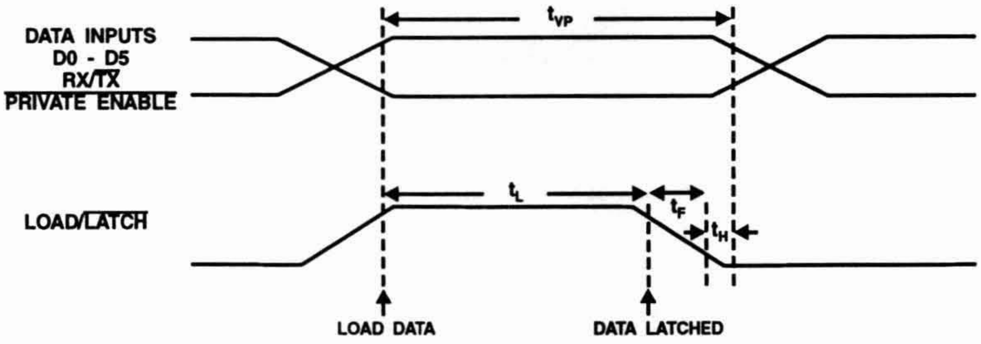
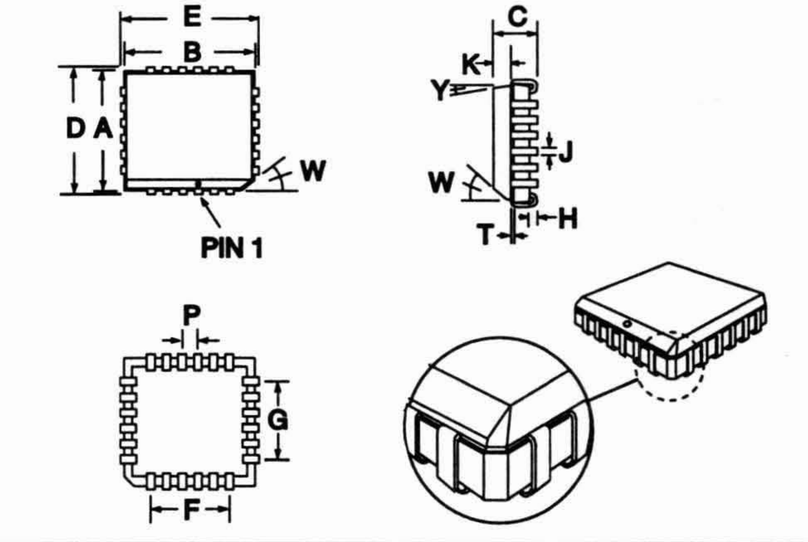

tVP
DATA INPUTS
D0 - D5
RX/TX
PRIVATE ENABLE
tL
tF
tH
LOAD/LATCH
LOAD DATA
DATA LATCHED

Figure 5: Parallel Load Timing

6.3 Packaging

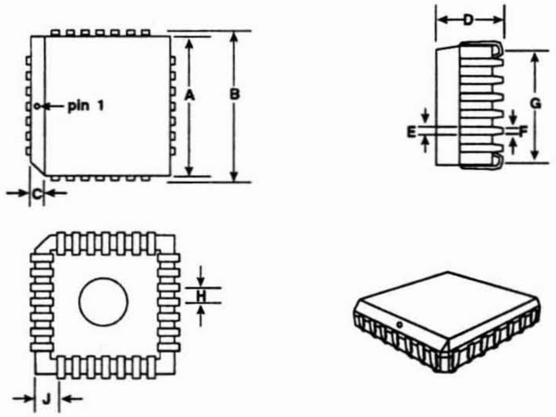

E
B
D
A
W
PIN 1
C
K
Y
J
W
T
H
P
G
F

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin PLCC Mechanical Outline: ***Order as part no. MX375LH***

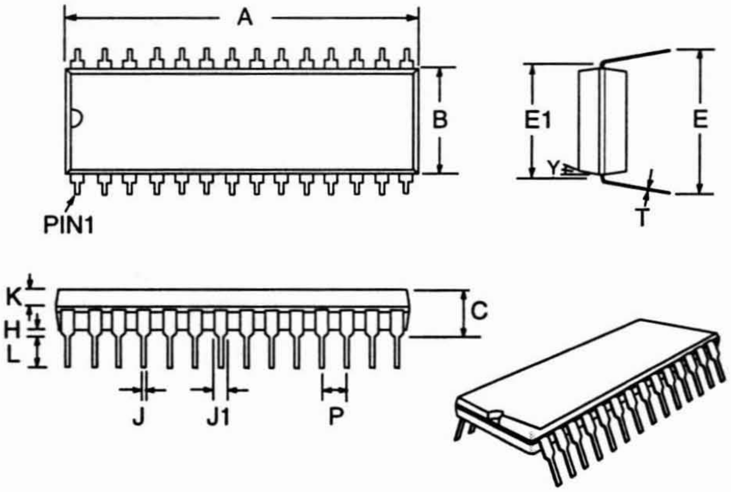


Package Tolerances

DIM.	MIN.	MAX.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 28-pin PLCC Mechanical Outline: ***Order as part no. MX375LH8***

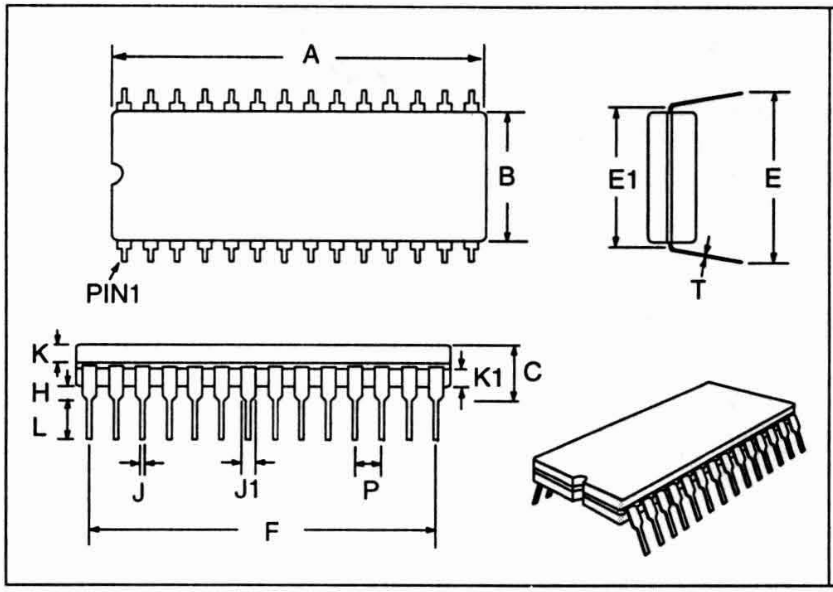


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.44)		1.47 (37.20)
B	0.530 (13.41)		0.555 (14.04)
C	0.160 (4.05)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.013 (0.33)		0.021 (0.53)
J1		0.060 (1.52)	
K	0.066 (1.67)		0.074 (1.88)
L	0.125 (3.16)		0.160 (4.05)
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 28-pin PDIP Mechanical Outline: ***Order as part no. MX375P***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.58)		1.460 (37.08)
B	0.510 (12.94)		0.530 (13.45)
C	0.165 (4.19)		0.230 (5.84)
E	0.640 (16.26)		0.715 (18.14)
E1	0.608 (15.43)		0.618 (15.70)
F		1.300 (33.02)	
H	0.015 (0.38)		0.050 (1.27)
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0090 (0.228)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 28-pin CDIP Mechanical Outline: ***Order as part no. MX375J***

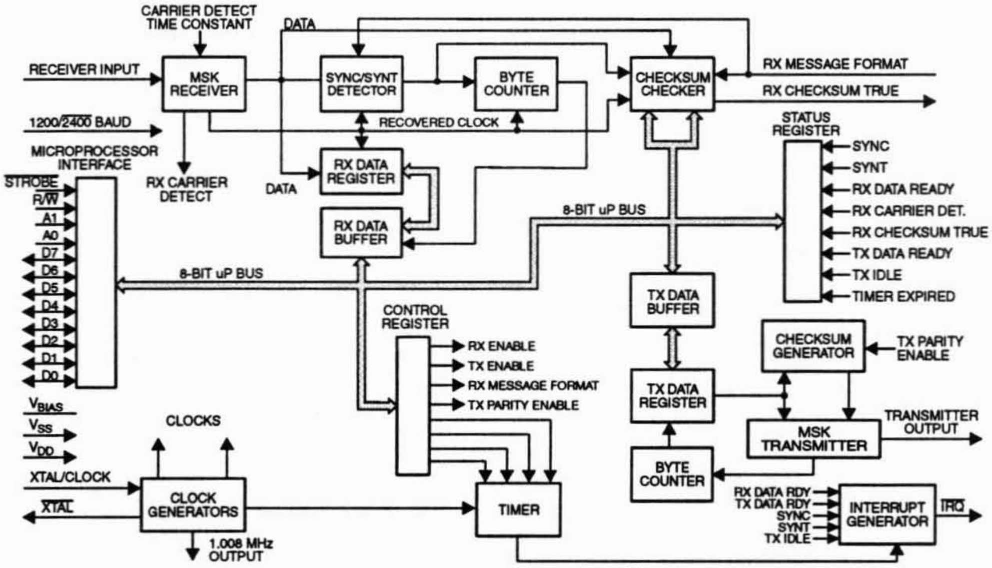
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

# MX429A 1200/2400bps MSK Modem
for Trunked Radio Systems

Features

- Band III & General Purpose Trunked Radio Apps
- Full-Duplex 1200 and 2400 Baud Operation
- Error Check Word Generation and Checking
- Preamble Generation
- µProcessor Compatible Interface
- Frame SYNC and SYNT Detection
- Low Power Consumption
- General Purpose Timer


CARRIER DETECT TIME CONSTANT
DATA
RECEIVER INPUT
MSK RECEIVER
SYNC/SYNT DETECTOR
BYTE COUNTER
CHECKSUM CHECKER
RX MESSAGE FORMAT
RX CHECKSUM TRUE
1200/2400 BAUD
RECOVERED CLOCK
STATUS REGISTER
MICROPROCESSOR INTERFACE
RX CARRIER DETECT
DATA
RX DATA REGISTER
RX DATA BUFFER
8-BIT uP BUS
SYNC
SYNT
RX DATA READY
RX CARRIER DET.
RX CHECKSUM TRUE
TX DATA READY
TX IDLE
TIMER EXPIRED
STROBE
R/W
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
8-BIT uP BUS
TX DATA BUFFER
CONTROL REGISTER
RX ENABLE
TX ENABLE
RX MESSAGE FORMAT
TX PARITY ENABLE
CHECKSUM GENERATOR
TX PARITY ENABLE
TX DATA REGISTER
MSK TRANSMITTER
TRANSMITTER OUTPUT
V_BIAS
V_SS
V_DD
CLOCKS
XTAL/CLOCK
XTAL
CLOCK GENERATORS
TIMER
BYTE COUNTER
RX DATA RDY
TX DATA RDY
SYNC
SYNT
TX IDLE
INTERRUPT GENERATOR
IRQ
1.008 MHz OUTPUT

The MX429A is a single-chip CMOS 1200 and 2400 baud MSK modem, designed primarily for use in Trunked Radio Systems but may also be employed in other general purpose radio or line data communication applications. The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The MX429A is full duplex at 1200 and 2400 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits. Preamble may be generated by the device in transmit. The 16-bit SYNC or SYNT words are detected in receive. An error check word is automatically generated in transmit and error checking is performed in the receive mode. An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides both 4.032MHz and 1.008MHz outputs and performs all modem timings.

The MX429A requires a single 5-volt power supply, has a powersave facility, and is available in the following package styles: 24-pin CDIP (MX429AJ), 24-pin PDIP (MX429AP), and 24-pin PLCC (MX429ALH).

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1 Block Diagram

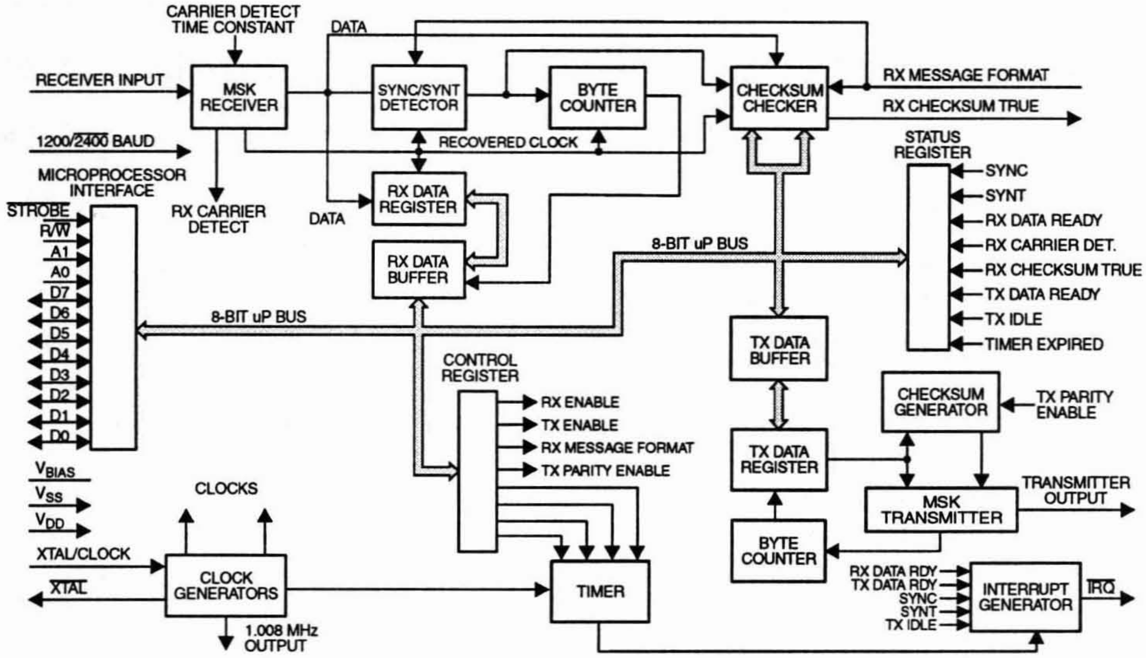
CARRIER DETECT TIME CONSTANT
DATA
RECEIVER INPUT
MSK RECEIVER
SYNC/SYNT DETECTOR
BYTE COUNTER
CHECKSUM CHECKER
RX MESSAGE FORMAT
RX CHECKSUM TRUE
1200/2400 BAUD
RECOVERED CLOCK
STATUS REGISTER
MICROPROCESSOR INTERFACE
STROBE
R/W
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
RX CARRIER DETECT
DATA
RX DATA REGISTER
RX DATA BUFFER
8-BIT uP BUS
8-BIT uP BUS
SYNC
SYNT
RX DATA READY
RX CARRIER DET.
RX CHECKSUM TRUE
TX DATA READY
TX IDLE
TIMER EXPIRED
TX DATA BUFFER
CONTROL REGISTER
RX ENABLE
TX ENABLE
RX MESSAGE FORMAT
TX PARITY ENABLE
CHECKSUM GENERATOR
TX PARITY ENABLE
TX DATA REGISTER
MSK TRANSMITTER
TRANSMITTER OUTPUT
V_{BIAS}
V_{SS}
V_{DD}
CLOCKS
XTAL/CLOCK
XTAL
CLOCK GENERATORS
1.008 MHz OUTPUT
TIMER
BYTE COUNTER
RX DATA RDY
TX DATA RDY
SYNC
SYNT
TX IDLE
INTERRUPT GENERATOR
IRQ

Figure 1: Block Diagram

2 Signal List

Pin No.		Signal		Description
J/P	LH	Name	Type	
1	1	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by a capacitor, see Figure 2.
2	2	Transmit Output	Output	The 1200 baud, 1200Hz/1800Hz and 2400 baud, 1200Hz/2400Hz MSK Tx output. When not enabled by the Control Register (D0) its output impedance is set high.
3	4	Receiver Input	Input	The 1200/2400 baud received MSK signal input. The 1200Hz/1800Hz, 1200Hz/2400Hz audio to this pin must be ac coupled via a capacitor, see Figure 2.
5	5	V_{DD}	Power	Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by a capacitor, see Figure 2.
6	6	Carrier Detect Time Constant:		The on-chip Carrier Detect function requires external component(s) on this pin. See Figure 2for recommended component(s).
7	7	Xtal/Clock		The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here, see Figure 2.
8	8	$\overline{\text{XTAL}}$		The output of the 4.032 MHz clock oscillator.

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Pin No.		Signal		Description
J/P	LH	Name	Type	
9	9	D0		Microprocessor Data Interface These 8 lines are used by the device to communicate with a microprocessor with the $R/\overline{W}$, A0 and A1 inputs determining register selection.
10	10	D1		
11	11	D2		
12	12	D3		
13	13	D4		
14	14	D5		
15	15	D6		
16	16	D7		
17	17	A0		Register Selection: These inputs, with the $R/\overline{W}$ input, select the required register to the data bus as shown in Table 2
18	18	A1		
19	19	$\overline{\text{STROBE}}$		Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating the high order address bits with a Read/Write clock. The MX429A is selected when this pin is a logic '0'.
20	20	$R/\overline{W}$		Used in conjunction with A1 and A0 to determine which internal registers are connected to the data interface pins (D0 to D7) during Strobe.
21	21	$\overline{\text{IRQ}}$		Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kW pullup to V_{DD}). The conditions that cause the interrupts are indicated at the Status Register and are as follows: Timer Expired, Rx Data Ready, Tx Data Ready, Tx Idle, Rx SYNC Detect, Rx SYNT Detect
22	24	$1200/\overline{2400}$ Baud Select		A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one and a half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor.
23	22	V_{SS}	Power	Negative Supply (GND)
24	23	Clock/4		A 1.008 MHz (X1 ÷ 4) clock is available at this output for external circuit use, note the source impedance and source current limits.
4	3			Leave this pin open-circuit

Table 1: Signal List

Register	$R/\overline{W}$	A0	A1
Control	0	1	1
Status	1	1	1
Rx Data	1	0	1
Tx Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

Table 2: Register Selection

3 External Components

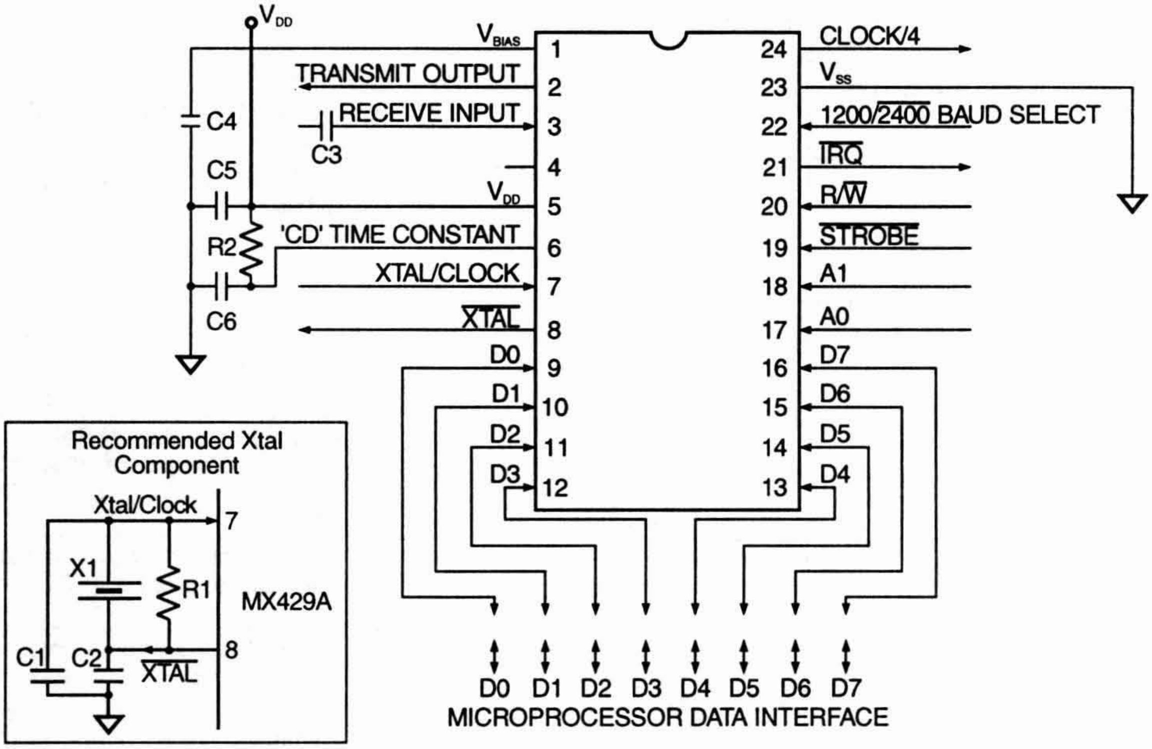

V_DD
V_BIAS
TRANSMIT OUTPUT
RECEIVE INPUT
C3
C4
C5
V_DD
R2
'CD' TIME CONSTANT
XTAL/CLOCK
C6
XTAL
D0
D1
D2
D3
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
CLOCK/4
V_SS
1200/2400 BAUD SELECT
IRQ
R/W
STROBE
A1
A0
D7
D6
D5
D4
Recommended Xtal Component
Xtal/Clock
7
X1
R1
MX429A
C1
C2
8
XTAL
D0 D1 D2 D3 D4 D5 D6 D7
MICROPROCESSOR DATA INTERFACE

Figure 2: Recommended External Components

R1		1MΩ	±10%
R2		1MΩ	±10%
C1		33pF	±20%
C2		33pF	±20%
C3		0.1µF	±20%

C4		1.0µF	±20%
C5		1.0µF	±20%
C6		1.0µF	±20%
X1	Note 1	4.032MHz	

Table 3: Recommended External Components

Notes:

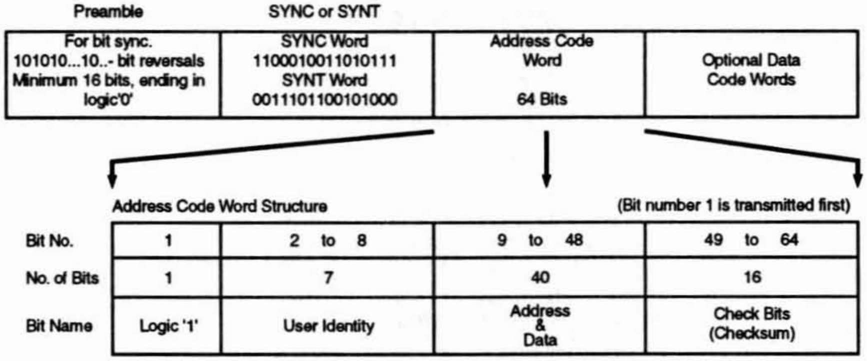
1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of VDD, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4 General Description

4.1 Modems in Mobile Data Signaling

4.1.1 Digital Code Format

The MPT 1327 Signaling Standard for Trunked LMR Systems protocol is used by the MX429 for communication between a Trunking System Controller (TSC) and users' radio units. These data stream formats are summarized in Figure 3.



Preamble	SYNC or SYNT		
For bit sync. 101010...10..- bit reversals Minimum 16 bits, ending in logic'0'	SYNC Word 1100010011010111 SYNT Word 0011101100101000	Address Code Word 64 Bits	Optional Data Code Words

Address Code Word Structure (Bit number 1 is transmitted first)

Bit No.	1	2 to 8	9 to 48	49 to 64
No. of Bits	1	7	40	16
Bit Name	Logic '1'	User Identity	Address & Data	Check Bits (Checksum)

Figure 3: Tx and Rx Data Stream

4.1.2 Operation

The MX429A can be used for Full-Duplex operation with the host microprocessor only having to operate on the data while the modem (MX429A) handles all other signaling routines and requirements.

In the Tx mode the MX429A will :

1. Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
2. Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
3. Accept from the host, and transmit, 6 bytes of data (Address Code Word):
   A. Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes.
   B. Upon a software command, disable internal checksum generation and allow continuous data transmission.
4. Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the Rx mode the MX429A will:

1. Detect and achieve bit synchronization within 16 bits.
2. Search for and detect the 16-bit 'SYNC'/'SYNT' word.
3. Output all received data after 'SYNC/SYNT,' in byte form.
4. Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.

Note: In Rx, a software command is used to determine whether a 'SYNC'/'SYNT' word is required after every 8 (6 data + 2 checksum) received bytes, or "data" is received continually.
Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

4.1.3 Non MPT Application – Full-Duplex

The functions described in this section, to allow the MX429A modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

Tx: When enabled the device transmits a "101010......10" preamble until data for transmission is loaded by the host microprocessor. Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages). Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

Rx: When enabled requires the 16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

4.1.4 Control Register (A1 = 1, A0 = 1, R/$\overline{\text{W}}$ = 0, Write Only)

The Control Register, when selected, directs the modem's operation as described in Table 4

Bit	Description	Function
Bit 0 D0	TX Enable	**Set**: D0 enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.........10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. **Clear**: The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.
Bit 1 D1	Tx Parity Enable	**Set**: D1 indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. **Clear**: No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written".
Bit 2 D2	Rx Enable	**Set**: D2 enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. **Clear**: The receiver is disabled and all interrupts caused by the receiver are inhibited.
Bit 3 D3	Rx Message Format	**Set**: D3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. **Clear**: The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received.
Bit 4 D4	Timer LSB	Reference Table 5
Bit 5 D5	Timer	
Bit 6 D6	Timer	
Bit 7 D7	Timer MSB	If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.
Tx Enable		If using the internal Tx preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occasionally produce a Tx Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either: a. Detecting that the timer interrupt status bit is not set and that it is not appropriate to load Tx data at this time. b. Not using the timer. i.e. immediately after Tx Enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.

Table 4: Control Register

D7	D6	D5	D4	Reset counter and disable timer interrupts				
0	0	0	0	Count and interrupt every				
0	0	0	1	"	"	"	8	bits
0	0	1	0	"	"	"	16	bits
0	0	1	1	"	"	"	24	bits
0	1	0	0	"	"	"	32	bits
0	1	0	1	"	"	"	40	bits
0	1	1	0	"	"	"	48	bits
0	1	1	1	"	"	"	56	bits
1	0	0	0	"	"	"	64	bits
1	0	0	1	"	"	"	72	bits
1	0	1	0	"	"	"	80	bits
1	0	1	1	"	"	"	88	bits
1	1	0	0	"	"	"	96	bits
1	1	0	1	"	"	"	104	bits
1	1	1	0	"	"	"	112	bits
1	1	1	1	"	"	"	120	bits

Table 5: Timer Control Bits

4.1.5 Status Register (A1 = 1, A0 = 1, R/$\overline{W}$ = 1, Read Only)

When an interrupt is generated, the $\overline{IRQ}$ Output goes low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function
Bit 0 D0	Rx Data Ready	**D0**: when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. **Set** when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared**: (i). by a read of the Status Register followed by a read of the Rx Data Buffer (ii). by Rx Enable going Low.
Bit 1 D1	Rx Checksum True	**D1**: when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit (D0) is set for the second byte of the received checksum, does not cause an interrupt. **Set**: by a correct comparison between the received and generated checksums. **Cleared**: (i). by a read of the Status Register followed by a read of the Rx Data Buffer (ii). by Rx Enable going Low.
Bit 2 D2	Rx Carrier Detect	**D2**: is a "Real Time" indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When MSK tones are present at the receiver input this bit goes High, for no MSK input this bit goes Low. When the Rx Enable bit (D2– Control Register) is Low Rx Carrier Detect will go Low.
Bit 3 D3	Tx Data Ready	D3: when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. **Set**: (i). when the contents of the Tx Data Buffer are transferred to the Tx Data Register (ii). when the Tx Enable is set (No interrupt is generated in this case. **Bit Cleared**: (i). by a read of the Status Register followed by a write to the Tx Data Buffer (ii). by Tx Enable going Low. **Interrupt Cleared**: (i). by a read of the Status Register (ii). by Tx Enable going Low.

Bit	Description	Function
Bit 4 D4	Tx Idle	**D4**: causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set**: one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D1). **Bit Cleared**: (i). by a write to the Tx Data Buffer (ii). by Tx Enable going Low. **Interrupt Cleared**: (i). by a read of the Status Register (ii). by Tx Enable going Low.
Bit 5 D5	Timer Interrupt	**D4**: causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set**: one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D1). **Bit Cleared**: (i). by a write to the Tx Data Buffer (ii). by Tx Enable going Low **Interrupt Cleared**: (i). by a read of the Status Register (ii). by Tx Enable going Low.
Bit 6 D6	Rx SYNC Detect *	**D6**: when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. **Set**: on receipt of the 16th bit of a 'SYNC' word. **Bit and Interrupt Cleared**: (i). by a read of the Status Register (ii). by Rx Enable going Low.
Bit 7 D7	Rx SYNT Detect *	**D7**: when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000) has been detected in the received bit stream. **Set**: on receipt of the 16th bit of a 'SYNT' word. **Bit and Interrupt Cleared**: (i). by a read of the Status Register (ii). by Rx Enable going Low.

* SYNC and SYNT Detection is disabled while the checksum checker is running.

Table 6: Status Register

4.1.6 Rx Data Buffer (A1 = 1, A0 = 0, R/$\overline{W}$ = 1, Read Only)

These 8 bits are the last byte of data received with bit 7 being received first. Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.

D0 LSB	D1	D2	D3	D4	D5	D6	D7 MSB

4.1.7 Tx Data Buffer (A1 = 1, A0 = 0, R/$\overline{W}$ = 0, Write Only)

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals. If the Tx Parity Enable bit (Control Register D1) is set, a 2–byte checksum will be inserted and transmitted by the modem after every 6 transmitted "message" bytes.

D0 LSB	D1	D2	D3	D4	D5	D6	D7 MSB

4.2 Syndrome Word

This 16-bit word (both Low and High bytes) may be used to correct errors. Bits S1 to S15 are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of " received message." For a correct message all 15 bits (S1 to S15) will be zero. The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register D0) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

4.2.1 Syndrome Low Byte (A1 = 0, A0 = 0, R/$\overline{W}$ = 1, Read Only)

D0	D1	D2	D3	D4	D5	D6	D7
S1	S2	S3	S4	S5	S6	S7	S8

4.2.2 Syndrome High Byte (A1 = 0, A0 = 1, R/$\overline{W}$ = 1, Read Only)

D0	D1	D2	D3	D4	D5	D6	D7
S9	S10	S11	S12	S13	S14	S15	Parity Error

D7: This is a "Parity Error Bit". Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Therefore a correctly received message all 16 bits of the Syndrome Word
(S1 to S15 and Parity Error) will be zero.

4.3 Carrier Detect Time Constant

The value of the Carrier Detect capacitor, C5, determines the carrier detect time constant. A long time constant (larger value C5) results in improved noise immunity but increased response time. C5 may be varied to optimize noise immunity/response time.

1. With R2 = 1MΩ and C5 = 1µF as external components for the carrier detect function at 1200 baud only.
2. By using C5 = 0.1µF and removing R2 completely the MX429A will operate at both 1200 and 2400 baud rates.

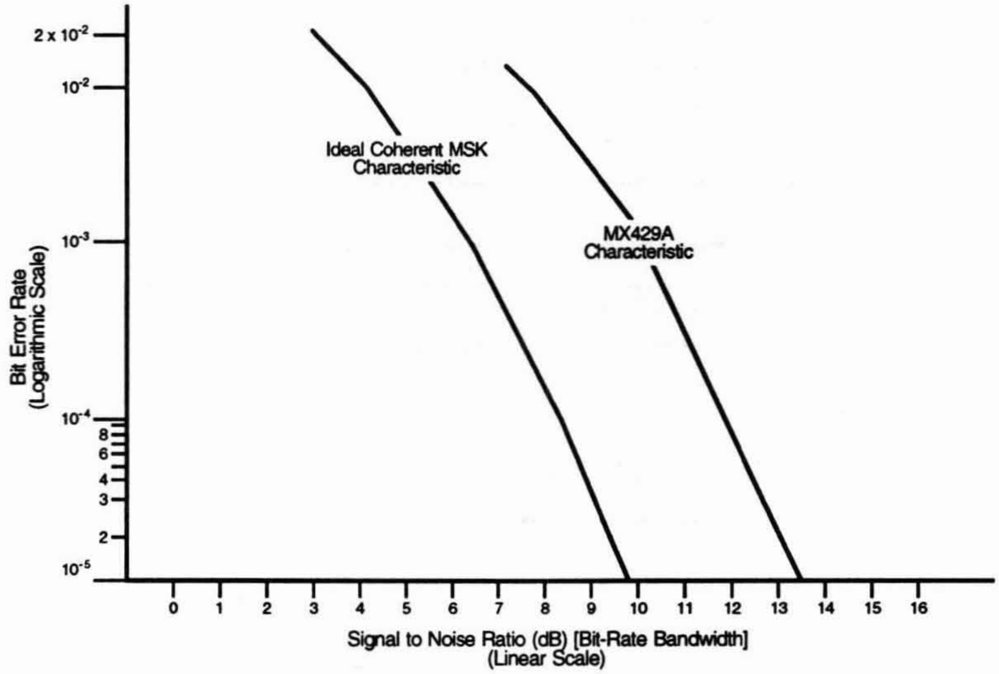


Figure 4: Bit Error Rate vs. Signal to Noise Ratio

5 Application

5.1 Checksum Generation and Checking

Generation – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16–bit word is used as the "Checksum."

Checking – The checksum checker does two things:

It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero. Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64). If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR D1) bit is set.

5.2 Receive Operation

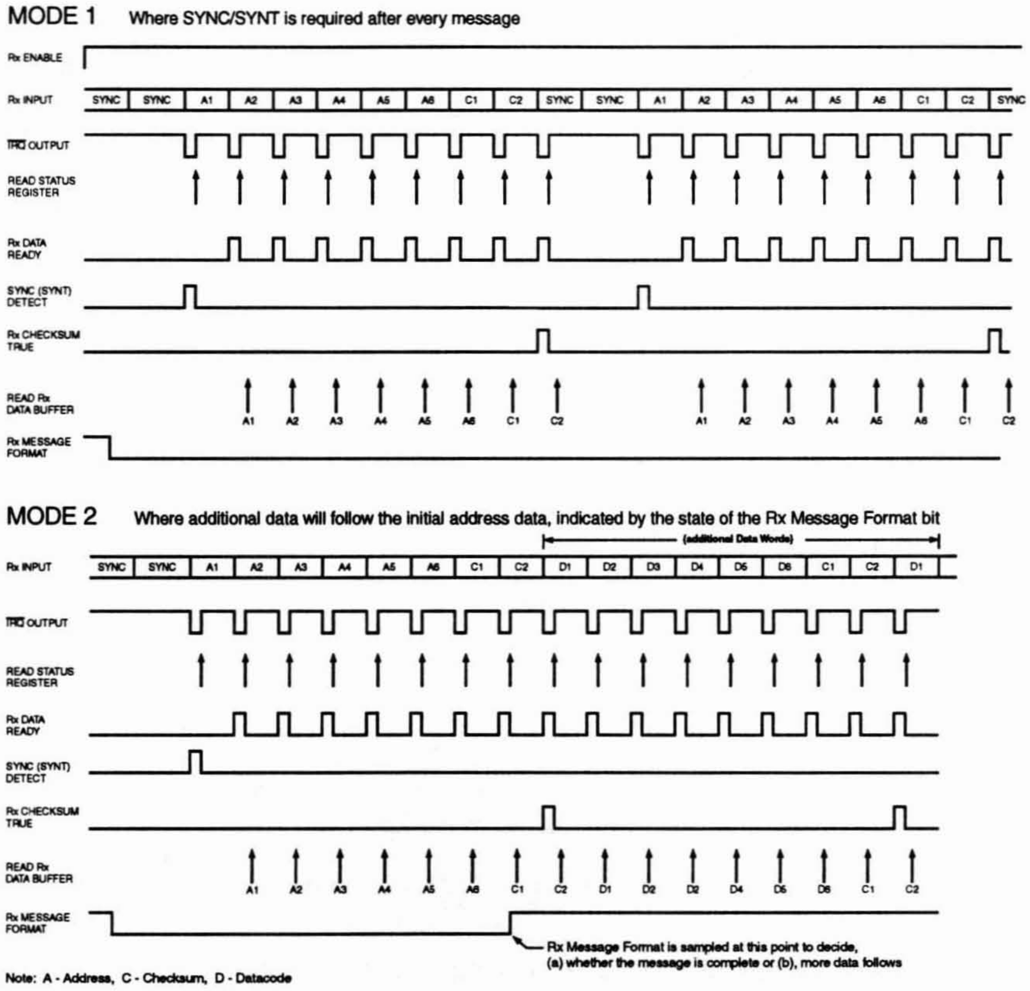
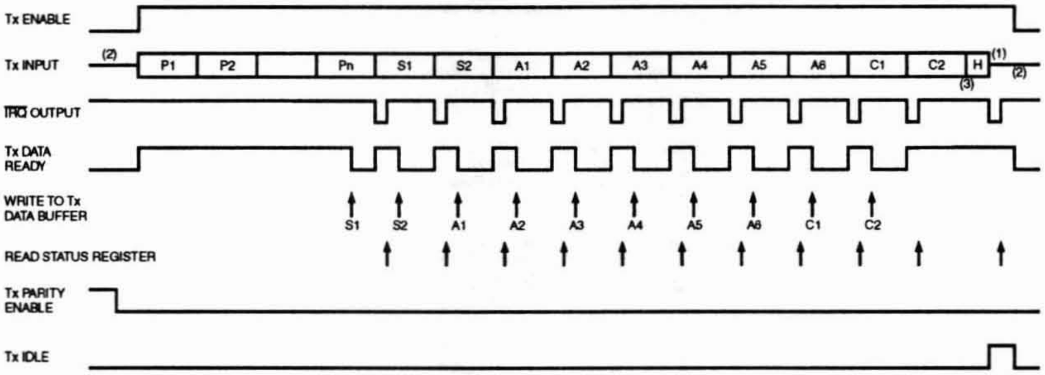

MODE 1 Where SYNC/SYNT is required after every message
Rx ENABLE
Rx INPUT
SYNC SYNC A1 A2 A3 A4 A5 A6 C1 C2 SYNC SYNC A1 A2 A3 A4 A5 A6 C1 C2 SYNC
IRQ OUTPUT
READ STATUS REGISTER
Rx DATA READY
SYNC (SYNT) DETECT
Rx CHECKSUM TRUE
READ Rx DATA BUFFER
A1 A2 A3 A4 A5 A6 C1 C2 A1 A2 A3 A4 A5 A6 C1 C2
Rx MESSAGE FORMAT
MODE 2 Where additional data will follow the initial address data, indicated by the state of the Rx Message Format bit
(additional Data Words)
Rx INPUT
SYNC SYNC A1 A2 A3 A4 A5 A6 C1 C2 D1 D2 D3 D4 D5 D6 C1 C2 D1
IRQ OUTPUT
READ STATUS REGISTER
Rx DATA READY
SYNC (SYNT) DETECT
Rx CHECKSUM TRUE
READ Rx DATA BUFFER
A1 A2 A3 A4 A5 A6 C1 C2 D1 D2 D2 D4 D5 D6 C1 C2
Rx MESSAGE FORMAT
Rx Message Format is sampled at this point to decide, (a) whether the message is complete or (b), more data follows
Note: A - Address, C - Checksum, D - Datacode

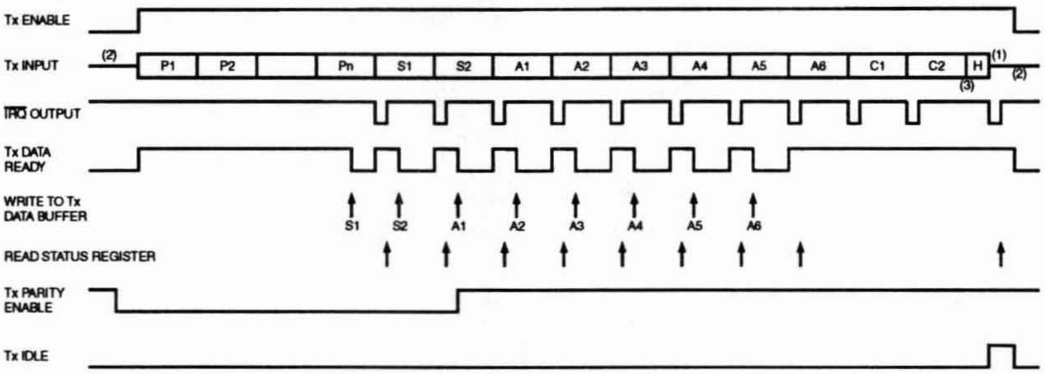
Figure 5: Receive Operation

5.3 Transmit Operation

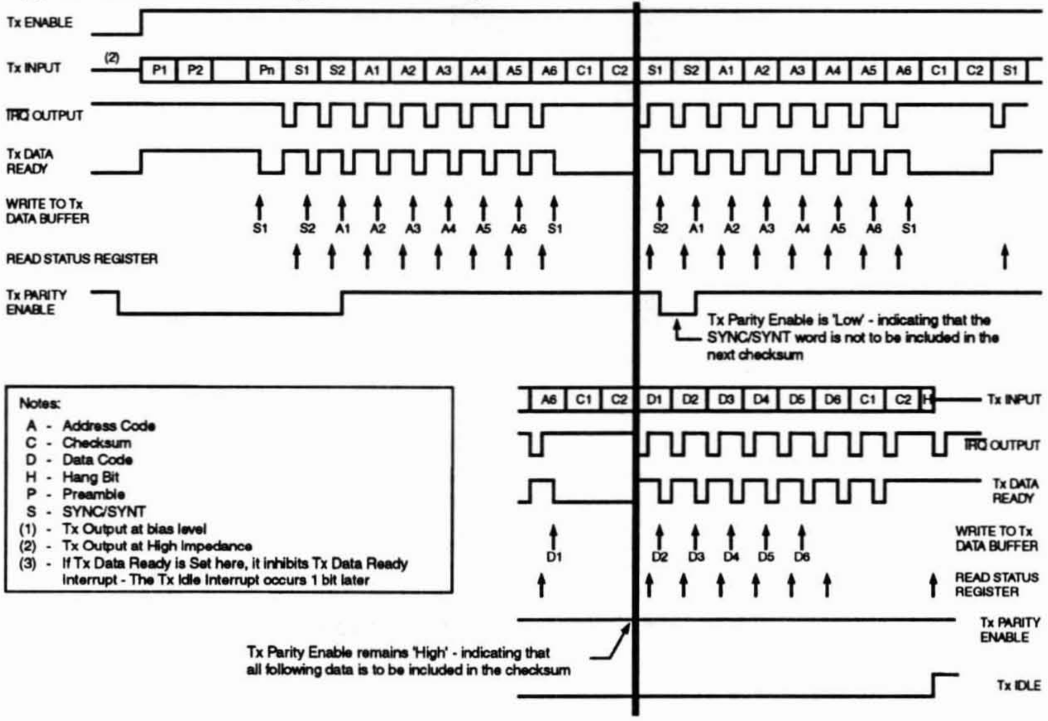
(a) Tx - one message with checksum supplied by host


Tx ENABLE
Tx INPUT
(2)
P1
P2
Pn
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
H
(1)
(2)
(3)
IRQ OUTPUT
Tx DATA READY
WRITE TO Tx DATA BUFFER
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
READ STATUS REGISTER
Tx PARITY ENABLE
Tx IDLE

(b) Tx - one message with checksum generated internally


Tx ENABLE
Tx INPUT
(2)
P1
P2
Pn
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
H
(1)
(2)
(3)
IRQ OUTPUT
Tx DATA READY
WRITE TO Tx DATA BUFFER
S1
S2
A1
A2
A3
A4
A5
A6
READ STATUS REGISTER
Tx PARITY ENABLE
Tx IDLE

(c) Tx - more than one message, with checksum generated internally


Tx ENABLE
Tx INPUT
(2)
P1
P2
Pn
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
S1
IRQ OUTPUT
Tx DATA READY
WRITE TO Tx DATA BUFFER
S1
S2
A1
A2
A3
A4
A5
A6
S1
S2
A1
A2
A3
A4
A5
A6
S1
READ STATUS REGISTER
Tx PARITY ENABLE
A6
C1
C2
D1
D2
D3
D4
D5
D6
C1
C2
H
Tx INPUT
IRQ OUTPUT
Tx DATA READY
WRITE TO Tx DATA BUFFER
D1
D2
D3
D4
D5
D6
READ STATUS REGISTER
Tx PARITY ENABLE
Tx IDLE

Tx Parity Enable is 'Low' - indicating that the SYNC/SYNT word is not to be included in the next checksum

Tx Parity Enable remains 'High' - indicating that all following data is to be included in the checksum

Notes:
- A - Address Code
- C - Checksum
- D - Data Code
- H - Hang Bit
- P - Preamble
- S - SYNC/SYNT
- (1) - Tx Output at bias level
- (2) - Tx Output at High Impedance
- (3) - If Tx Data Ready is Set here, it inhibits Tx Data Ready Interrupt - The Tx Idle Interrupt occurs 1 bit later

Figure 6: Transmit Operation

5.4 Basic Power Up Software

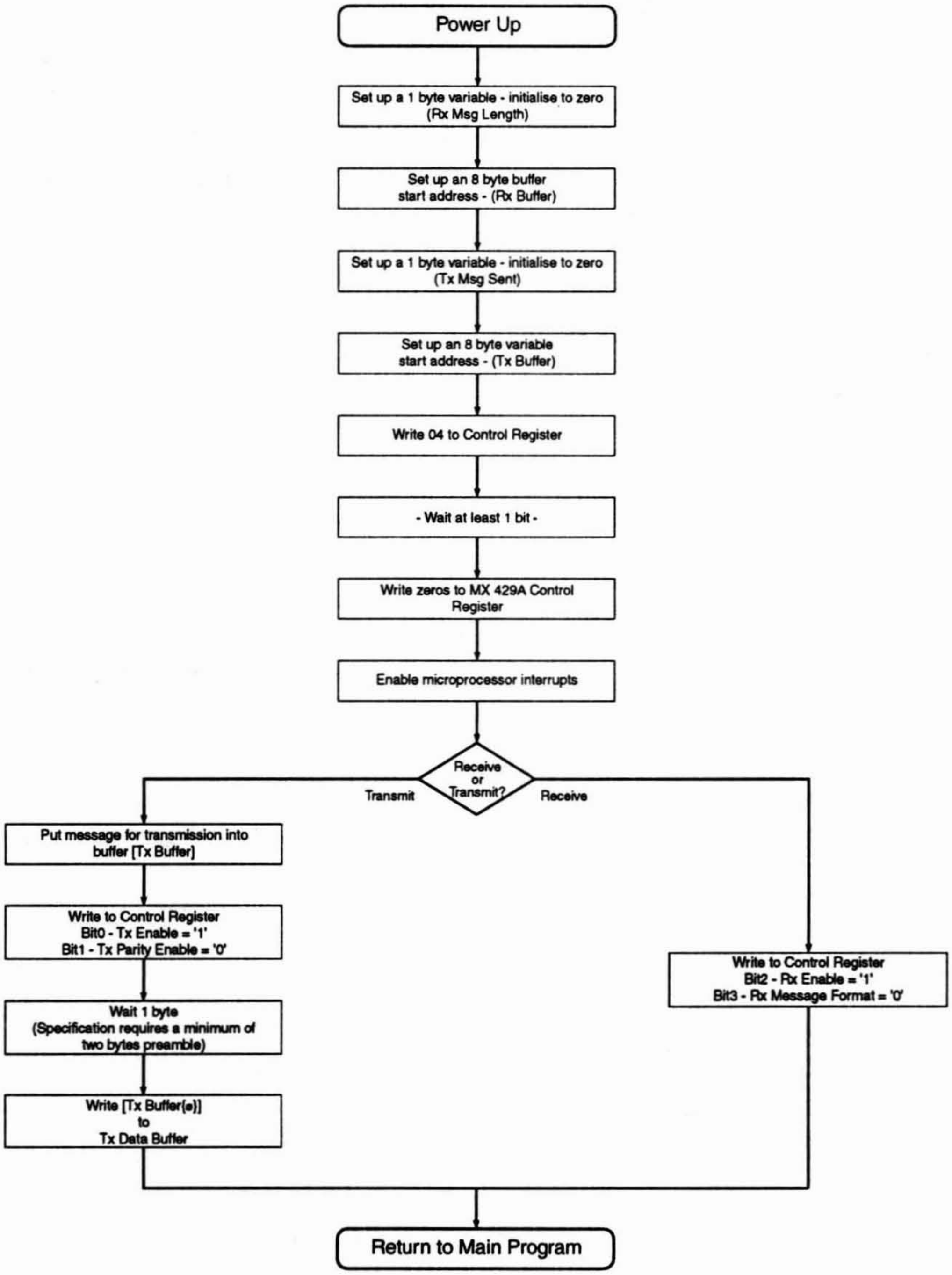

Power Up
Set up a 1 byte variable - initialise to zero (Rx Msg Length)
Set up an 8 byte buffer start address - (Rx Buffer)
Set up a 1 byte variable - initialise to zero (Tx Msg Sent)
Set up an 8 byte variable start address - (Tx Buffer)
Write 04 to Control Register
- Wait at least 1 bit -
Write zeros to MX 429A Control Register
Enable microprocessor interrupts
Receive or Transmit?
Transmit
Receive
Put message for transmission into buffer [Tx Buffer]
Write to Control Register Bit0 - Tx Enable = '1' Bit1 - Tx Parity Enable = '0'
Wait 1 byte (Specification requires a minimum of two bytes preamble)
Write [Tx Buffer(e)] to Tx Data Buffer
Write to Control Register Bit2 - Rx Enable = '1' Bit3 - Rx Message Format = '0'
Return to Main Program

Figure 7: Basic Power-Up Software

5.5 Basic Software Interrupt Flow

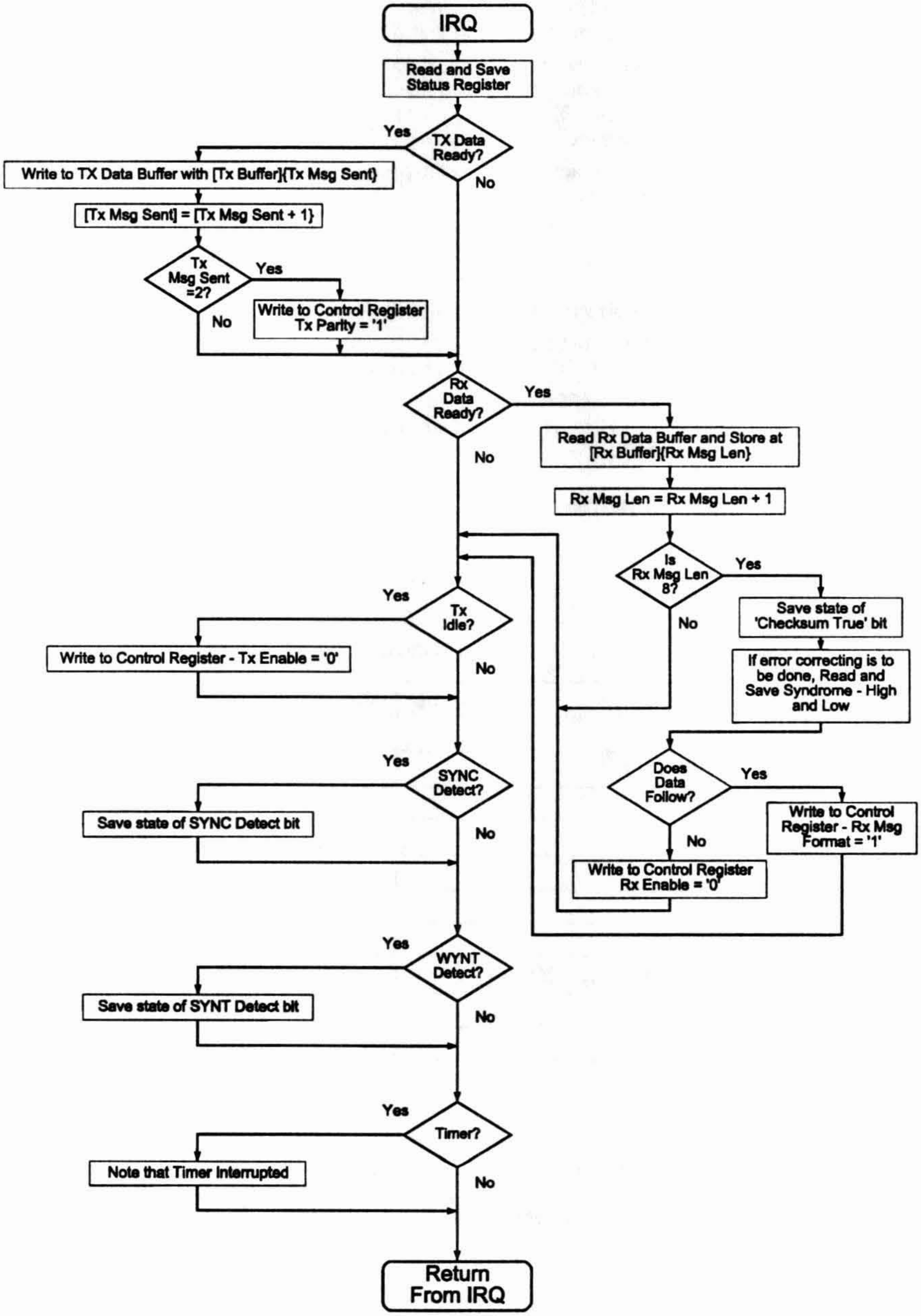

IRQ
Read and Save Status Register
TX Data Ready?
Yes
No
Write to TX Data Buffer with [Tx Buffer]{Tx Msg Sent}
[Tx Msg Sent] = [Tx Msg Sent + 1}
Tx Msg Sent =2?
Yes
No
Write to Control Register Tx Parity = '1'
Rx Data Ready?
Yes
No
Read Rx Data Buffer and Store at [Rx Buffer]{Rx Msg Len}
Rx Msg Len = Rx Msg Len + 1
Is Rx Msg Len 8?
Yes
No
Save state of 'Checksum True' bit
If error correcting is to be done, Read and Save Syndrome - High and Low
Does Data Follow?
Yes
No
Write to Control Register - Rx Msg Format = '1'
Write to Control Register Rx Enable = '0'
Tx Idle?
Yes
No
Write to Control Register - Tx Enable = '0'
SYNC Detect?
Yes
No
Save state of SYNC Detect bit
WYNT Detect?
Yes
No
Save state of SYNT Detect bit
Timer?
Yes
No
Note that Timer Interrupted
Return From IRQ

Figure 8: Basic Software Interrupt Flow

5.6 Bus Interface Timing

It is very important that circuit designs conform to the bus interface timing specification as described in Section 6.1.4. Failure to do so can result in intermittent operation that is difficult to troubleshoot.

For example, if the bus timing is incorrect, the required two step READ Rx data transaction (1: Read Status Register, 2: Read Rx Data Buffer) may fail on step 2. As a result, the MX429A IRQ will not be reset and subsequently expected IRQ's will not occur. This symptom might be incorrectly interpreted as an MX429A functional failure but is, in fact, caused by the circuit design's bus interface timing violation.

Other examples can occur on WRITE transactions that fail to properly clear the IRQ and so prevent subsequently expected IRQ's from occurring.

Circuit designs should be careful to strictly conform to the t_{DHW} specification, the Data Hold Time (Write), as assumed requirements may be incorrect.

5.6.1 Bus interface design migration from MX429 to MX429A

The MX429A bus interface timing requirements precisely match those of its predecessor, the MX429. As a result, properly designed and operated MX429 bus interface circuits are compatible with the MX429A device.

It should be noted that the MX429 and MX429A device may behave ***differently in those designs, which violate the bus timing specification***. However, this is caused by the timing violation rather than an incompatibility between the two devices.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
J / P / LH Package					
Total allowable Power Dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above °C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.032		MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 5.0V$, $T_{AMB} = 25°C$, Xtal/Clock $f_0 = 4.032MHz$
Bit Rate Bandwidth = 1200Hz, Audio Level 0dB ref: = $300mV_{RMS}$

Static Values	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Current Ranges					
Rx and Tx Enabled				7.0	mA
Rx Enabled, Tx Disabled			4.0	6.0	mA
Rx Disabled, Tx Enabled				7.0	mA
Rx and Tx Disabled			1.5	2.5	mA
Dynamic Values					
Modem Internal Delay			1.5		ms
Interface Levels					
Output Logic '1' Source Current	2			120	μA
Output Logic '0' Sink Current	3			360	μA
Three State Output Leakage Current				4.0	μA
D0 – D7 Data In/Out	1				
Logic '1' Level		3.5			V
Logic '0' Level				1.5	V
A1, A0, R/W, STROBE, IRQ	4				
Logic '1' Level		4.0			V
Logic '0' Level				1.0	V
Analog Impedance's					
Rx Input		100			kΩ
Tx Output (Enabled)			10		kΩ
Tx Output (Disabled)			5.0		MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0			MΩ
R_{OUT}	5		30.0		kΩ
Oscillator Gain			25.0		dB
Xtal frequency			4.032		MHz
Receiver					
Signal Input Levels	6	–9.0	–2.0	10.5	dB
Bit Error Rate	7				
@ 12dB Signal/Noise Ratio			7.0		10^{-4}
@ 20dB Signal/Noise Ratio			1.0		10^{-8}
Synchronization @ 12dB Signal/Noise Ratio	8				
Probability of Bit 16 being correct			99.5		%
Carrier Detect Response Time	8		13.0		ms

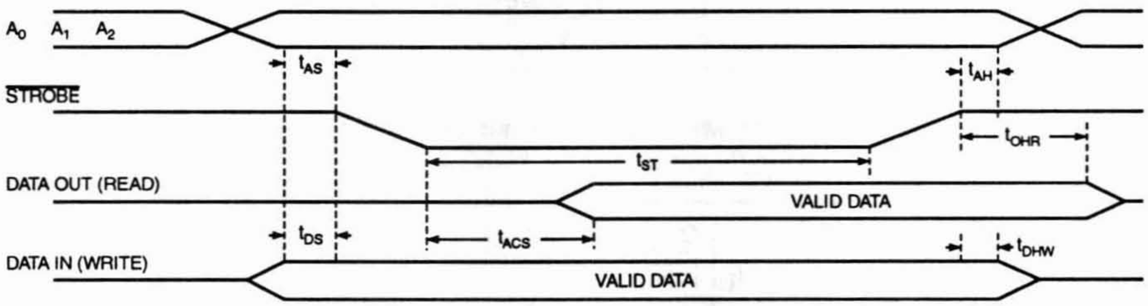
Static Values	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Transmitter					
Output Level			8.25		dB
Output Level Variation	10	-1.0		1.0	dB
Output Distortion			3.0	5.0	%
3rd Harmonic Distortion			2.0	3.0	%
Logic '1' Frequency 1200 baud	9		1200		Hz
2400 baud	9		1200		Hz
Logic '0' Frequency 1200 baud	9		1800		Hz
2400 baud	9		2400		Hz
Isochronous Distortion					
1200Hz – 1800Hz/1200Hz - 2400Hz		25	40	μs	
1800Hz – 1200Hz/2400Hz - 1200Hz		20	40	μs	

Operating Characteristics Notes:

1. With each data line loaded as, C = 50pf and R = $10k\Omega$.
2. V_{OUT} = 4.6V.
3. V_{OUT} = 0.4V
4. Sink/Source currents ≤ 0.1mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 4, Bit Error Rate.
8. This Response Time is measured using a 10101010101.... 01 pattern input signal at a level of 230mV_{RMS} (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.
10. The amplitude difference between the Transmit Output signals (tones) representing a logic '0' a logic '1'.

6.1.4 Timing

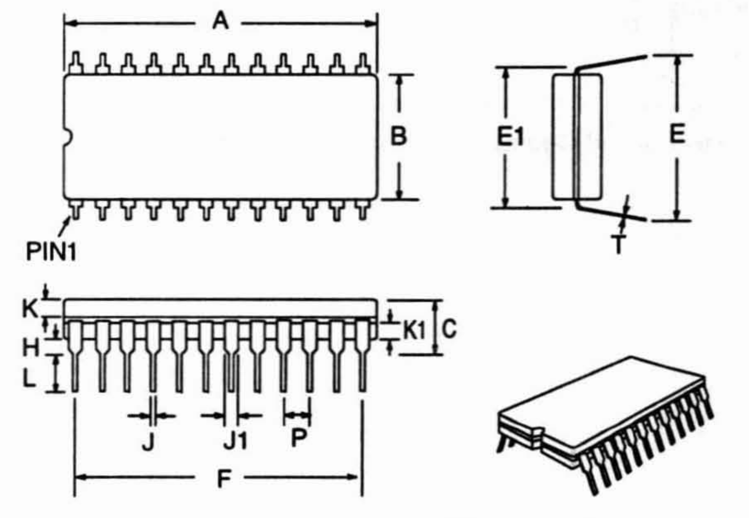
Timing see Figure 9		Min.	Typ.	Max.	Units
(t_{ACS})	Access Time			135	ns
(t_{AH})	Address Hold Time	0			ns
(t_{AS})	Address Set-up Time	0			ns
(t_{DHW})	Data Hold Time (Write)	85			ns
(t_{DS})	Data Set-up Time (Write)	0			ns
(t_{OHR})	Output Hold Time (Read)	15		105	ns
(t_{ST})	Strobe Time	140			ns


A0 A1 A2
tAS
tAH
STROBE
tOHR
tST
DATA OUT (READ)
VALID DATA
tDS
tACS
tDHW
DATA IN (WRITE)
VALID DATA

t_{ACS} - Access Time
t_{AS} - Address Set-Up Time
t_{DS} - Data Set-Up Time
t_{AH} - Address Hold Time
t_{DHW} - Data Hold Time (Write)
t_{OHR} - Output Hold Time (Read)
t_{ST} - Strobe Time

Figure 9: Timing Diagram

6.2 Packaging

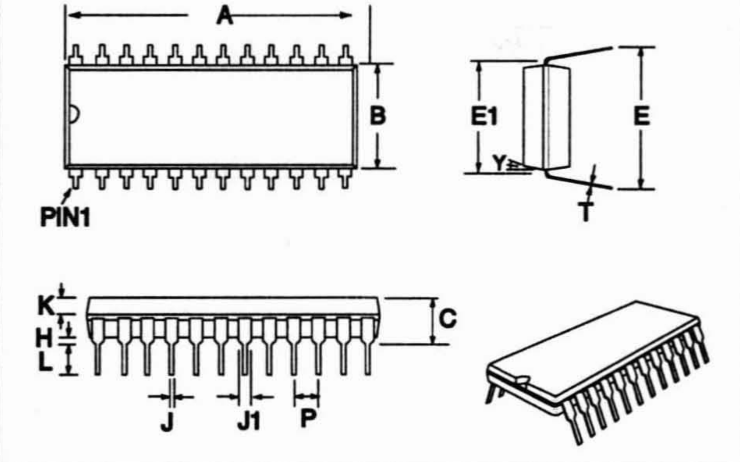

A
B
PIN1
E1
E
T
K
H
L
K1
C
J
J1
P
F

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin CDIP Mechanical Outline: ***order as part no. MX429AJ***

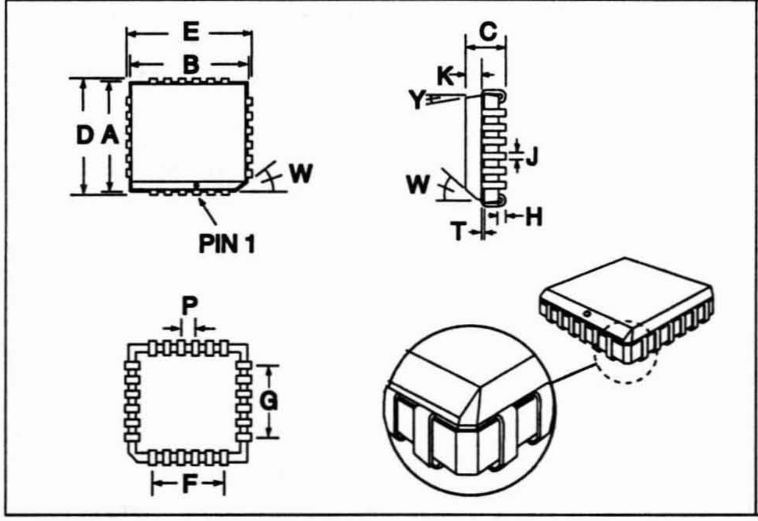


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: *order as part no. MX429AP*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin PLCC Mechanical Outline: *order as part no. MX429ALH*

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX465

LOW VOLTAGE CTCSS ENCODER/DECODER

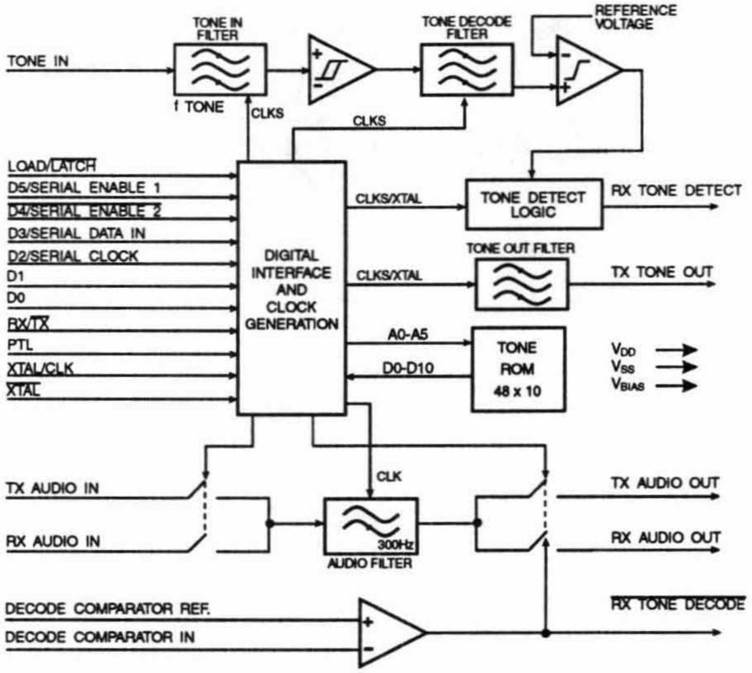
with Tx and Rx Audio Filters

Features

- Meets TIA/EIA-603 Standards
- 47 CTCSS Tones + Notone
- TX/RX Speech Filters
- Improved Sinad
- Serial or Parallel Programming
- Easy µP Interface
- Scanning on any Channel
- Standard 4MHz Xtal (See MX165C for 1MHz)
- Low Voltage 3.3V to 5.0V

Applications

- Mobile Radio Channel Sharing
- Scan Trunking
- Wireless Intercom Traffic Control
- Hookswitch Supervision
- Repeater Control


TONE IN FILTER
TONE DECODE FILTER
REFERENCE VOLTAGE
TONE IN
f TONE
CLKS
CLKS
LOAD/LATCH
D5/SERIAL ENABLE 1
D4/SERIAL ENABLE 2
D3/SERIAL DATA IN
D2/SERIAL CLOCK
D1
D0
RX/TX
PTL
XTAL/CLK
XTAL
DIGITAL INTERFACE AND CLOCK GENERATION
CLKS/XTAL
TONE DETECT LOGIC
RX TONE DETECT
TONE OUT FILTER
CLKS/XTAL
TX TONE OUT
A0-A5
D0-D10
TONE ROM 48 x 10
VDD
VSS
VBIAS
CLK
TX AUDIO IN
RX AUDIO IN
300Hz
AUDIO FILTER
TX AUDIO OUT
RX AUDIO OUT
DECODE COMPARATOR REF.
DECODE COMPARATOR IN
RX TONE DECODE

The MX465 CTCSS Encoder/Decoder is a low voltage, CMOS device that meets TIA/EIA-603 Standards. The MX465 will encode and decode the tones 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz in addition to the 39 standard CTCSS tones, for a total of 47 CTCSS tones + Notone. With the incorporation of the on-chip TX and RX speech filter, the MX465 enhances voice/tone multiplexing by attenuating TX and RX speech 36dB at frequencies below 250Hz while passing signals > 300Hz with only 1dB of ripple. This not only minimizes CTCSS talk-off in the TX mode but also improves Hum and Noise performance in the RX mode.

Available in the following package styles: 24-pin TSSOP (MX465TN), 24-pin SSOP (MX465DS), 24-pin SOIC (MX465DW), 24-pin PLCC (MX465LH), 24-pin PDIP (MX465P), and 24-pin CDIP (MX465J) the MX465 requires a single 3.3V to 5.0V supply and a 4MHz clock or crystal.

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MX-COM, Inc. Reserves the right to change specifications at any time and without notice

1 Block Diagram

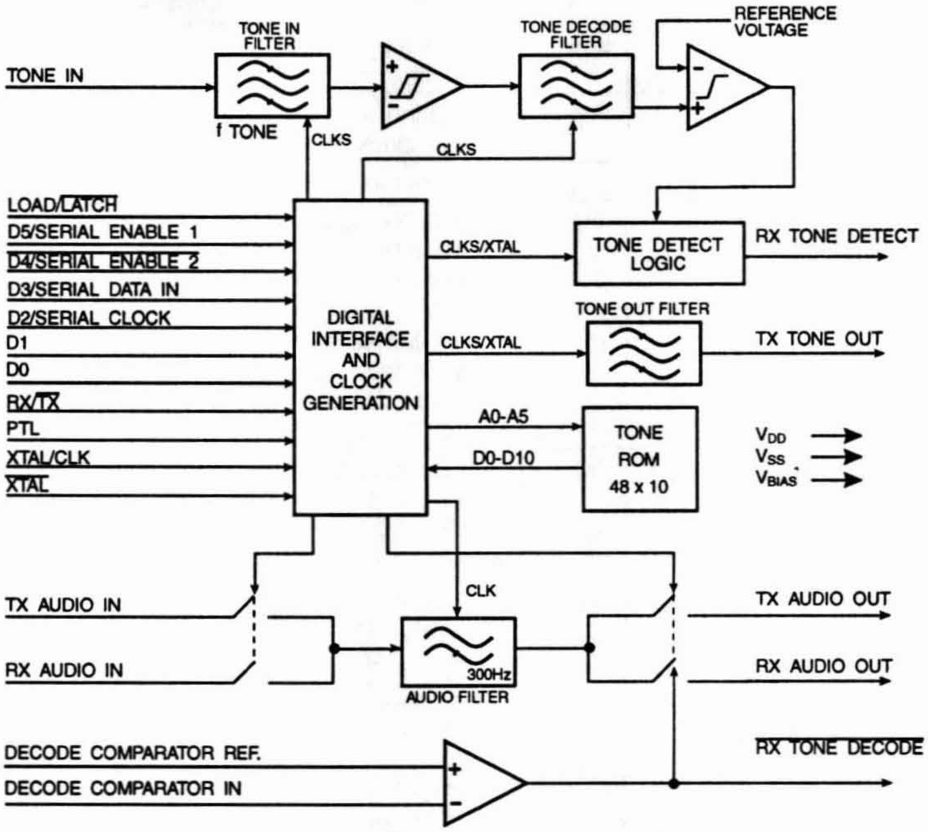

TONE IN FILTER
TONE DECODE FILTER
REFERENCE VOLTAGE
TONE IN
f TONE
CLKS
CLKS
LOAD/LATCH
D5/SERIAL ENABLE 1
D4/SERIAL ENABLE 2
D3/SERIAL DATA IN
D2/SERIAL CLOCK
D1
D0
RX/TX
PTL
XTAL/CLK
XTAL
DIGITAL INTERFACE AND CLOCK GENERATION
CLKS/XTAL
TONE DETECT LOGIC
RX TONE DETECT
TONE OUT FILTER
CLKS/XTAL
TX TONE OUT
A0-A5
D0-D10
TONE ROM 48 x 10
V_{DD}
V_{SS}
V_{BIAS}
CLK
TX AUDIO IN
RX AUDIO IN
300Hz
AUDIO FILTER
TX AUDIO OUT
RX AUDIO OUT
DECODE COMPARATOR REF.
DECODE COMPARATOR IN
RX TONE DECODE

Figure 1 : Block Diagram

2 Signal List

Pin No.	Signal	Type	Description
1	V_{DD}	power	Positive supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
2	XTAL/CLOCK	input	Input to the on-chip inverter used with a 4 MHz Xtal or external clock source.
3	$\overline{\text{XTAL}}$	output	Output of the on-chip inverter (clock output).
4	LOAD/$\overline{\text{LATCH}}$	input	Controls 8 on-chip latches. It is used to latch RX/$\overline{\text{TX}}$, PTL, and D0-D5. A logic 1 applied to this input places the 8 latches in the 'transparent' mode. A logic 0 applied to this input places the 8 latches in the 'latched' mode. In Parallel Mode, data is loaded and latched by a logic 1-0 transition (see Figure 4). In Serial Mode, data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Figure 5). Internally pulled to V_{DD}
5	D5 / SERIAL ENABLE 1	input	Data input D5 (Parallel Mode). A logic 1 applied to this input together with a logic 0 applied to D4/$\overline{\text{SERIAL ENABLE 2}}$ will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
6	D4 / $\overline{\text{SERIAL ENABLE 2}}$	input	Data input D4 (Parallel Mode). A logic 0 applied to this input together with a logic 1 applied to D5 / SERIAL ENABLE 1 will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
7	D3 / SERIAL DATA IN	input	Data input D3 (Parallel Mode). In Serial Mode this pin becomes the serial data input for D5-D0, RX/$\overline{\text{TX}}$ and PTL (see Figure 5). D5 is clocked first and PTL last. Internally pulled to V_{DD}.
8	D2 / SERIAL CLOCK	input	Data input D2 (Parallel Mode). In Serial Mode this pin becomes the SERIAL CLOCK input. Data is clocked on the positive going edge (see Figure 5). Internally pulled to V_{DD}.
9	D1	input	Data input D1 (Parallel Mode). Internally pulled to V_{DD}.
10	D0	input	Data input D0 (Parallel Mode). Internally pulled to V_{DD}.
11	V_{SS}	power	Negative supply.
12	DECODE COMPARATOR REF.	input	Internally biased to $V_{DD}/3$ or 2 $V_{DD}/3$ via 1M resistors depending on the logic state of the $\overline{\text{RX TONE DECODE}}$ pin. $\overline{\text{RX TONE DECODE}}$ = 1 will bias this input 2 $V_{DD}/3$; a logic 0 will bias this input $V_{DD}/3$. This input provides the DECODE COMPARATOR REFERENCE voltage, and the switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.
13	$\overline{\text{RX TONE DECODE}}$	output	Gated output of the decode comparator. This output is used to gate the RX Audio path. A logic 0 on this pin indicates a successful decode and the DECODE COMPARATOR IN pin is more positive than the DECODE COMPARATOR REF. input (see Table 3).
14	DECODE COMPARATOR IN	input	Inverting input of the DECODE COMPARATOR. This pin is normally connected to the integrated output of the RX TONE DETECT line.
15	RX TONE DETECT	output	In RX mode this output will go to logic 1 during a successful decode. It must be externally integrated to control response and deresponse times (see Table 3).

Pin No.	Signal	Type	Description
16	TX TONE OUT	output	The CTCSS sinewave output appears on this pin under control of the $RX/\overline{TX}$ pin. When not transmitting a tone, TX TONE OUT may be biased to $V_{DD}/2$. (see Table 3).
17	$RX/\overline{TX}$	input	RX or TX modes selected in Parallel Mode (see Figure 4). In Serial Mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	PTL	input	In RX mode this pin operates as a 'Push To Listen' function by enabling the RX audio path, thus overriding the tone squelch function (Parallel Mode). In Serial Mode this function is loaded serially. Internal pull-up to V_{DD}
19	RX AUDIO OUT	output	High pass filtered RX AUDIO OUT. This pin outputs audio when $\overline{\text{RX TONE DECODE}}$ = logic 0, PTL = logic 1, or when Notone is programmed (see Table 4). In TX mode this pin is biased to $V_{DD}/2$.
20	TX AUDIO OUT	output	High pass filtered TX AUDIO OUT pin. In TX mode this pin outputs audio present at the TX AUDIO IN pin. In RX mode this pin is biased to $V_{DD}/2$
21	V_{BIAS}	output	Output of an internally generated $V_{DD}/2$ bias level that would normally be externally bypassed to V_{SS} via capacitor C6.
22	TX AUDIO IN	input	In TX mode TX AUDIO IN may be prefiltered, using the TX Audio path, thus helping to avoid talk-off due to intermodulation of speech frequencies with the transmitted CTCSS tone. Internally biased to $V_{DD}/2$.
23	RX AUDIO IN	input	Input to the audio high pass filter in RX mode. Internally biased to $V_{DD}/2$.
24	TONE INPUT	input	Input to the CTCSS tone detector. Internally biased to $V_{DD}/2$.

Table 1: Signal List

3 External Components

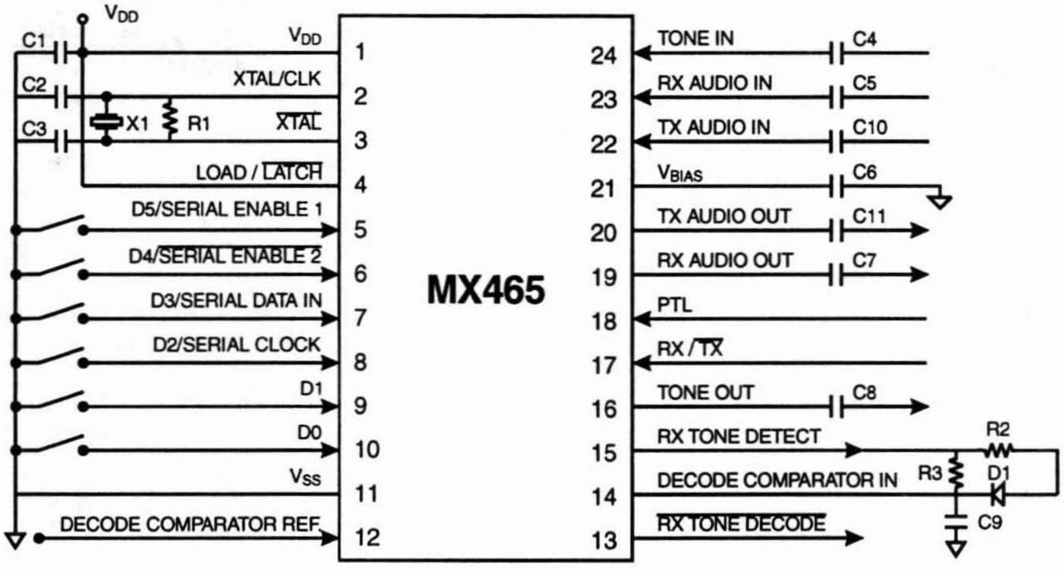

VDD
C1
C2
C3
X1
R1
VDD 1
XTAL/CLK 2
XTAL 3
LOAD / LATCH 4
D5/SERIAL ENABLE 1 5
D4/SERIAL ENABLE 2 6
D3/SERIAL DATA IN 7
D2/SERIAL CLOCK 8
D1 9
D0 10
VSS 11
DECODE COMPARATOR REF 12
MX465
24 TONE IN C4
23 RX AUDIO IN C5
22 TX AUDIO IN C10
21 VBIAS C6
20 TX AUDIO OUT C11
19 RX AUDIO OUT C7
18 PTL
17 RX / TX
16 TONE OUT C8
15 RX TONE DETECT
14 DECODE COMPARATOR IN
13 RX TONE DECODE
R2
R3
D1
C9

Figure 2 : Recommended External Components for Typical Application

R1	Note 1	1.0MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
C1		0.1µF	±20%
C2	Note 1	18pF	±20%
C3	Note 1	33pF	±20%
C4	Note 2	0.1µF	±20%
C5	Note 2	0.1µF	±20%

C6		0.47µF	±20%
C7	Note 2	0.1µF	±20%
C8	Note 2	0.1µF	±20%
C9	Note 2	0.1µF	±20%
C10	Note 2	0.1µF	±20%
C11	Note 2	0.1µF	±20%
D1		small signal	
X1	Note 1	4MHz	100ppm max.

Table 2: External Components

External Components Notes:

1. The values specified for R1, C2, and C3 have been found to be satisfactory when used with a crystal (X1) whose equivalent series resistance is ≤ 1000Ω. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. The 0.1µF value for the DC Blocking capacitors, C4, C5, C7, C8, C9, C10, and C11 is not a requirement. For the capacitors C4, C5, and C10, the input impedance is internal to the device and specified typical as 550kΩ. For the remaining capacitors external circuits will be important in determining the input impedance.

4 General Description

4.1 Description

Voice on shared radio channels are multiplexed with a subaudible CTCSS (Continuous Tone Controlled Subaudible Squelch) tone as a means of directing messages among user groups sharing the same RF frequencies. CTCSS modulates the transmitter with a discrete tone, from 39 standard CTCSS tones in the range (67.0Hz to 250.0Hz) according to TIA/EIA-603. There are an additional eight CTCSS tones not specified in TIA/EIA-603 that the MX465 will encode and decode. They are : 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz, for a total of 47 CTCSS tones plus Notone.

The MX465 also incorporates TX/RX on chip speech filters. In early CTCSS designs, TX speech was not filtered from the CTCSS tone, rather the filtering was dependent upon the host transmitter's pre-emphasis network. At only 6dB/octave, the attenuation of speech components at higher CTCSS tones was only a few dB which resulted in talk-off (low frequency voice components unsquelching the receiver audio).

4.2 I/O Conditions

D0-D5	Tone	No Tone	Tone	Tone	Tone	No Tone
Input Pins Condition						
RX / $\overline{\text{TX}}$	0	0	1	1	1	1
PTL	0	X	0	1	X	X
Decode Comparator In	X	X	0	0	1	X
Output Pins Condition						
RX TONE DETECT	0	0	0	0	1	X
$\overline{\text{RX TONE DECODE}}$	1	1	1	1	0	0
Result / Function						
Tone Transmitter Enabled	Yes	No (Bias)	No (Bias)	No (Bias)	No (Bias)	No (Bias)
TX Audio Path Enabled	Yes	Yes	No	No	No	No
Tone Decode Enabled	No	No	Yes	Yes	Yes	Yes
RX Audio Path Enabled	No (Bias)	No (Bias)	No (Bias)	Yes	Yes	Yes
Notes	1	2	3	4	5	6

Notes:

1. Normal tone transmit condition.
2. Notone programmed in TX mode, tone transmit output set to $V_{DD}/2$. TX audio path enabled.
3. Normal decode standby.
4. Normal decode standby with PTL used to enable audio.
5. Normal decode of correct CTCSS tone condition, PTL has no effect.
6. Notone programmed in RX mode, tone transmit output (Bias). RX audio path enabled.
7. X = don't care

Table 3: Combinations of Input / Output conditions

4.3 Filter Response

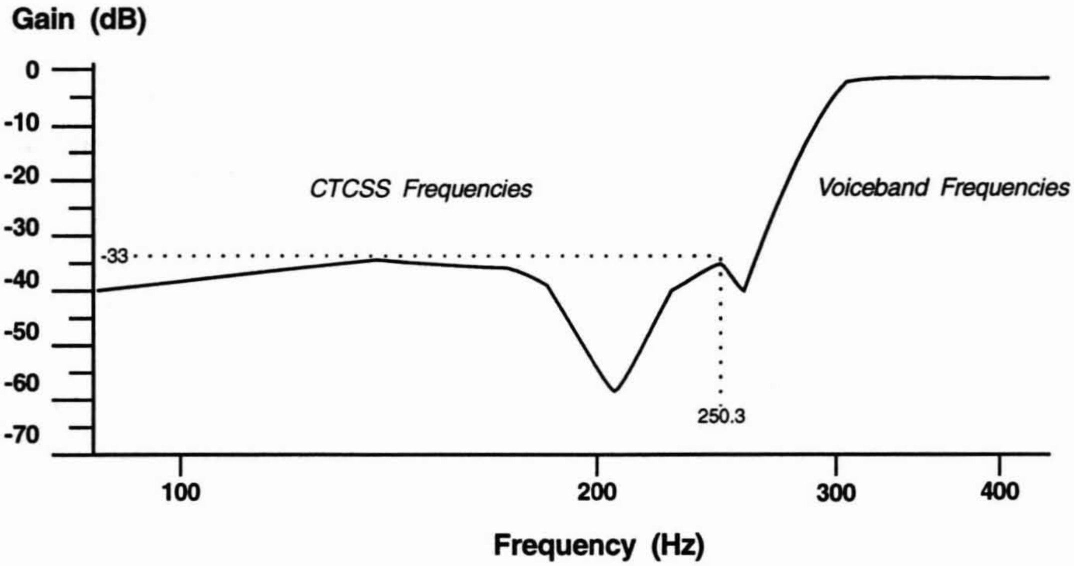


Figure 3 : Voiceband Filter Response

4.4 Serial and Parallel Mode Timing

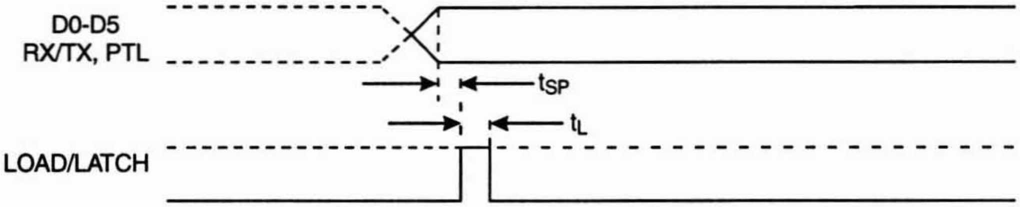
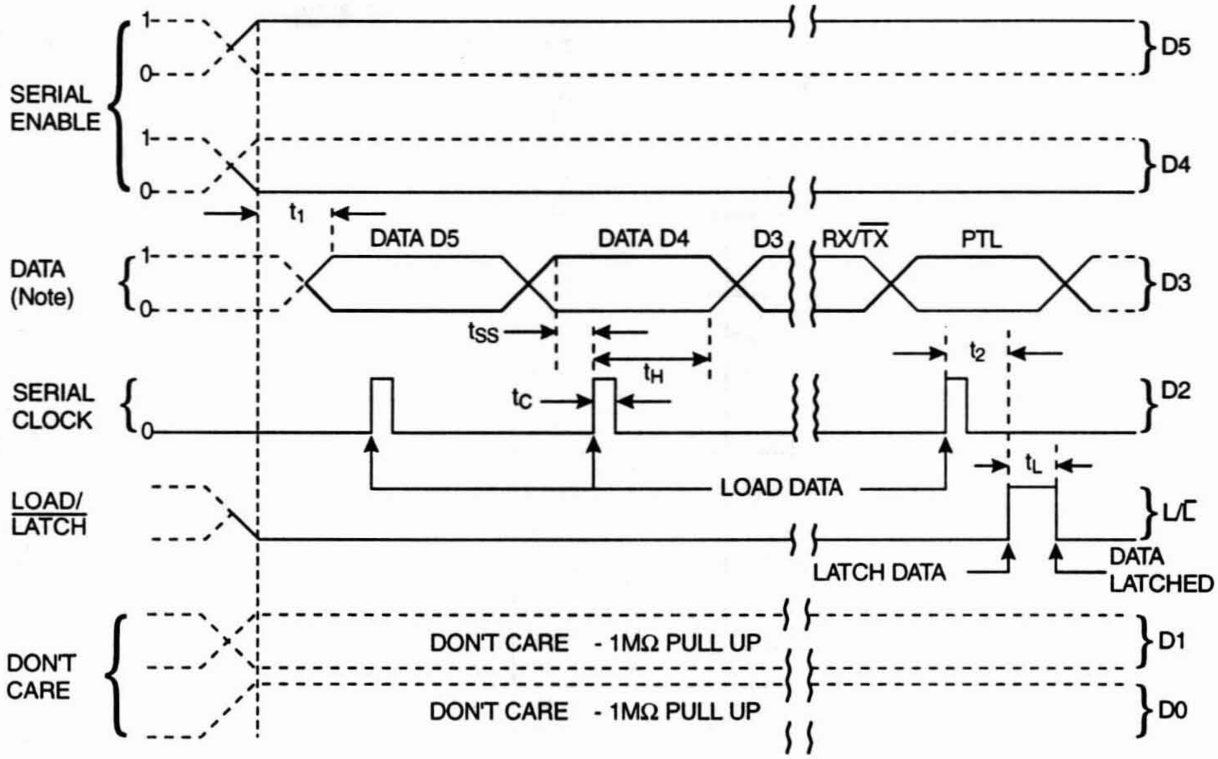

D0-D5
RX/TX, PTL
t_{SP}
t_L
LOAD/LATCH

Figure 4 : Parallel Mode


SERIAL
ENABLE
1
0
D5
D4
t_1
DATA D5
DATA D4
D3
RX/$\overline{TX}$
PTL
DATA
(Note)
D3
t_{SS}
t_H
t_2
SERIAL
CLOCK
t_C
D2
LOAD DATA
t_L
LOAD/
LATCH
L/$\overline{L}$
LATCH DATA
DATA
LATCHED
DON'T
CARE
DON'T CARE - 1MΩ PULL UP
D1
DON'T CARE - 1MΩ PULL UP
D0

Note : Serial bit 1 through bit 8 = D5, D4, D3, D2, D1, D0, RX/TX and PTL respectively. Load bit 1 first, bit 8 last

Figure 5 : Serial Mode

4.5 CTCSS Programming

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX465 Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
	67.0	66.98	-0.029	1	1	1	1	1	1	3F
	69.3	69.32	0.024	1	1	1	0	0	1	39
	71.9	71.901	0.001	0	1	1	1	1	1	1F
	74.4	74.431	0.042	1	1	1	1	1	0	3E
	77.0	76.965	-0.046	0	0	1	1	1	1	0F
	79.7	79.677	-0.029	1	1	1	1	0	1	3D
	82.5	82.483	-0.021	0	1	1	1	1	0	1E
	85.4	85.383	-0.020	1	1	1	1	0	0	3C
	88.5	88.494	-0.007	0	0	1	1	1	0	0E
	91.5	91.456	-0.048	1	1	1	0	1	1	3B
	94.8	94.76	-0.042	0	1	1	1	0	1	1D
	97.4	97.435	-0.036	1	1	1	0	1	0	3A
	100.0	99.96	-0.040	0	0	1	1	0	1	0D
	103.5	103.429	-0.069	0	1	1	1	0	0	1C
	107.2	107.147	-0.05	0	0	1	1	0	0	0C
	110.9	110.954	0.049	0	1	1	0	1	1	1B
	114.8	114.84	0.035	0	0	1	0	1	1	0B
	118.8	118.793	-0.006	0	1	1	0	1	0	1A
	123.0	123.028	0.023	0	0	1	0	1	0	0A
	127.3	127.328	0.022	0	1	1	0	0	1	19
	131.8	131.674	-0.095	0	0	1	0	0	1	09
	136.5	136.612	0.082	0	1	1	0	0	0	18
	141.3	141.323	0.016	0	0	1	0	0	0	08
	146.2	146.044	-0.107	0	1	0	1	1	1	17
	151.4	151.441	0.027	0	0	0	1	1	1	07
	156.7	156.875	0.112	0	1	0	1	1	0	16
•	159.8	159.936	0.085	1	1	0	0	0	1	31
	162.2	162.311	0.069	0	0	0	1	1	0	06
	167.9	167.708	-0.114	0	1	0	1	0	1	15
	173.8	173.936	0.078	0	0	0	1	0	1	05
	179.9	179.654	-0.137	0	1	0	1	0	0	14
•	183.5	183.680	0.098	1	1	0	0	1	0	32
	186.2	186.289	0.048	0	0	0	1	0	0	04
•	189.9	190.069	0.089	1	1	0	0	1	1	33
	192.8	192.864	0.033	0	1	0	0	1	1	13
•	196.6	196.329	-0.138	1	1	0	1	0	0	34
•	199.5	199.312	-0.094	1	1	0	1	0	1	35
	203.5	203.645	0.071	0	0	0	0	1	1	03
•	206.5	206.207	-0.142	1	1	0	1	1	0	36
	210.7	210.848	0.070	0	1	0	0	1	0	12
	218.1	217.853	-0.113	0	0	0	0	1	0	02
	225.7	225.339	-0.160	0	1	0	0	0	1	11

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX465 Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
•	229.1	229.279	0.078	1	1	0	1	1	1	37
	233.6	233.359	-0.103	0	0	0	0	0	1	01
	241.8	241.970	0.070	0	1	0	0	0	0	10
	250.3	250.282	-0.007	0	0	0	0	0	0	00
•	254.1	254.162	0.024	1	1	1	0	0	0	38
	Notone		N/A	1	1	0	0	0	0	30
	Serial input mode		N/A	1	0	Data	Clock	X	X	2X
•	Not specified in the TIA/EIA tone set									

Table 4: CTCSS Tones

5 Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pins	-20	20	mA
TN / DW / LH / DIP Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	**Max.**	**Units**
Supply (V_{DD}-V_{SS})	2.7	5.5	V
Xtal Frequency	4.0	4.0	MHz
Operating Temperature	-40	85	°C

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V / 5.0V at T_{AMB} = 25°C, V_{SS} = 0V,
Xtal Frequency = 4.0 MHz, 100ppm max.
(Over the life of the XTAL the operating range may vary from 100ppm up to 1000ppm)
0dB ref. = 750mV_{RMS} (proportional to V_{DD}; see note 17)

Composite Signal:
1kHz test tone = 300mV_{RMS}, f0 CTCSS tone = 30 mV_{RMS}, 75mV_{RMS} Noise (band limited to 6kHz Gaussian)

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply voltage		2.7	3.3/5.0	5.5	V
Supply current					
V_{DD} = 5.0V			3.7	4.2	mA
V_{DD} = 3.3V			1.3	1.6	mA
Analog input impedance	18	480	550		kΩ
Analog output impedance	18		400	1000	Ω
Digital Input impedance	1,18	25	40		kΩ
Input logic 1	1	70%V_{DD}			V
Input logic 0	1			30%V_{DD}	V
Output Logic 1 source = 0.1mA	2	80%V_{DD}			V
Output Logic 0 sink = 0.1mA	2			20%V_{DD}	V
Dynamic Values					
Speech filter					
Total harmonic distortion	5,8,19		1.0	1.5	%
Output noise level (input AC short circuit, audio switch enabled)	8,18		0.5	1.0	mV_{RMS}
Sinad	8,9	40	50		dB
Spurious emissions	18			- 48	dB
Cutoff frequency			300		Hz
Bandpass ripple	8		1	1.8	dB
Stopband attenuation <250Hz	7,8,19	33	36		dB
Passband gain 1kHz		- 0.5	0	0.5	dB
TX/RX isolation	5		60		dB
Encoder					
Tone output level	12	- 1.0	0	1.0	dB
Tone Frequency Accuracy (f error)		- 0.3		0.3	%f_0
Risetime to 90% nominal output					
f_0>100Hz	4,10		15	75	ms
f_0<100Hz	4,10		45	120	ms
Total Harmonic Distortion	19		1.5	2	%

	Notes	Min.	Typ.	Max.	Units
Decoder					
Pure tone decode threshold	19		7	15	mV_{RMS}
Composite signal decode threshold	3			30	mV_{RMS}
Decode input signal level	16	-20		3.5	dB
Pure tone decode response time	13,14	95	115	140	ms
Pure tone decode deresponse time	13,15	95	130	170	ms
Decode response time	3,6,10			250	ms
Deresponse time	3,10		180	250	ms
Decode selectivity:					
Upper decode band edge	3,11,19,20	$1.005f_0$	$1.015f_0$	$0.995f_{0+1}$	Hz
Lower decode band edge	3,11,19,20	$1.005f_{0-1}$	$0.985f_0$	$0.995f_0$	Hz
Serial / Parallel Inputs					
Parallel Set Up Time (t_{SP})		400			ns
Load / Latch Pulse Width (t_L)		400			ns
Serial Clock Pulse Width (t_C)		400			ns
Serial Data Set-Up Time (t_{SS})		400			ns
Serial Data Hold Time (t_H)		400			ns
Serial Enable Time (t_1)		400			ns
Serial Load / Latch Set-Up Time (t_2)		400			ns
Serial Clock Frequency			1		MHz

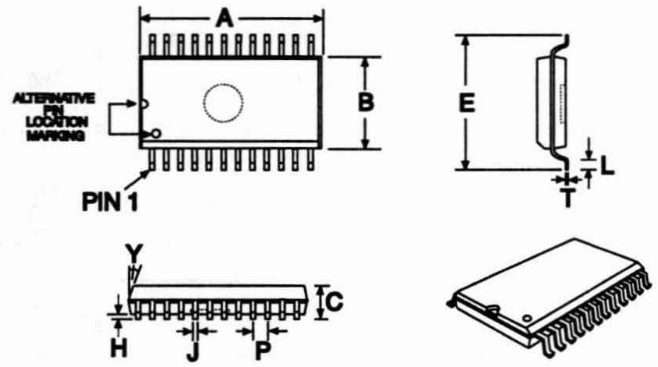
Operating Characteristics Notes:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite signal test condition.
4. Any programming tone and $R_L = 10k\Omega$, $C_L = 15pF$.
5. With an input level of 0dB @1kHz
6. f_0>100Hz (for 100 Hz> f_0>67Hz: t=100/ f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. With an input level of -3.5dB @1kHz
10. Per TIA/EIA-603.
11. Per TIA/EIA-603, device will not decode adjacent TIA/EIA-603 Tones.
12. Tone output level is proportional to V_{DD}.
13. f_0=156.7Hz @ -20dB.
14. Typically 12.5 Tone Cycles + 40ms.
15. Typically 7 Tone Cycles + 90ms.
16. Max composite signal is 3.5dB with:
    Noise (band limited 6kHz Gaussian) = -12dB ref to 1kHz test tone
    f_0 CTCSS tone = -20dB ref to 1kHz test tone
17. For maximum dynamic range, set audio level to 0dB, V_{DD} x150mV_{RMS}, using minimum V_{DD} under which system is intended to work. (e.g. for a 2.7V system, use 0dB equal to 405mV_{RMS}).
18. By characterization only.

19. Batch sampled only
20. For example, if: $f_0 = 100.0Hz$ ($f_{0-1} = 97.4Hz$ $f_{0+1} = 103.5Hz$)

Decode Selectivity	Min	Typ	Max	Unit
Upper Decode Band Edge	100.5	101.5	102.98	Hz
Lower Decode Band Edge	97.89	98.5	99.5	Hz

5.2 Packaging

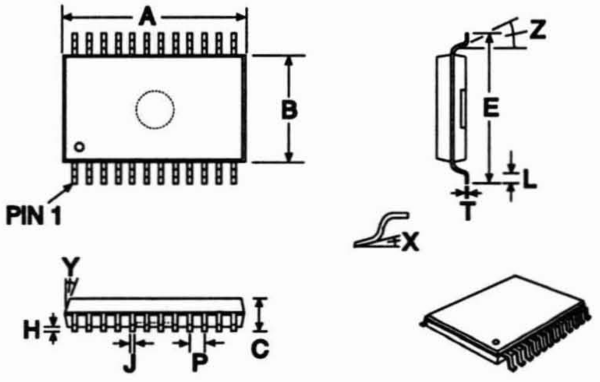


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	---------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin TSSOP Mechanical Outline: Order as part no. MX465TN

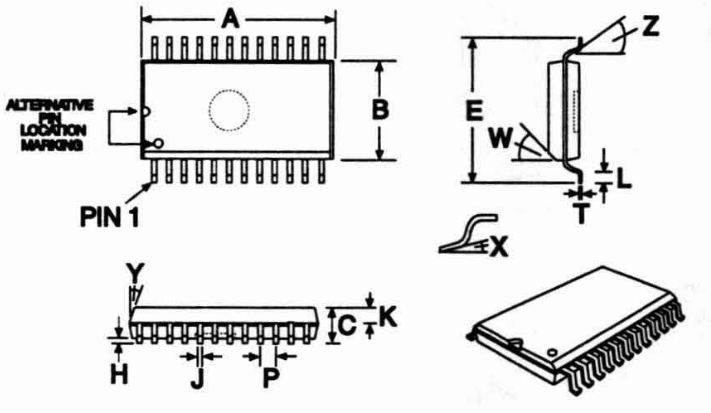


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin-SSOP Mechanical Outline: ***Order as part no. MX465DS***

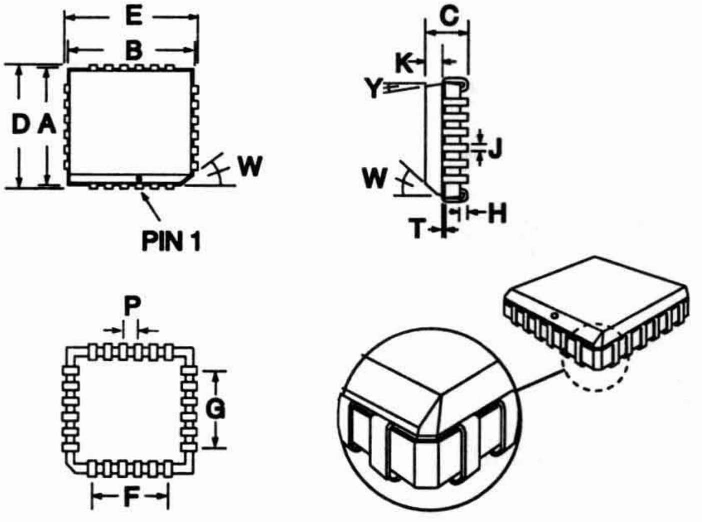


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin SOIC Mechanical Outline: *Order as part no. MX465DW*

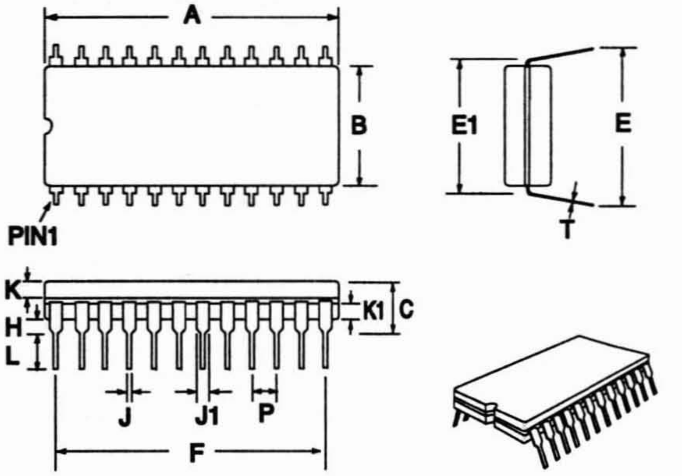


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin PLCC Mechanical Outline: *Order as part no. MX465LH*

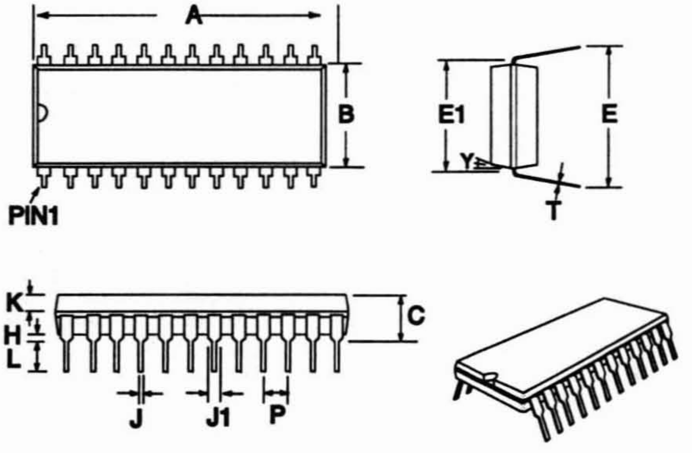


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin-CDIP Mechanical Outline: ***Order as part no. MX465J***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: ***Order as part no. MX465P***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

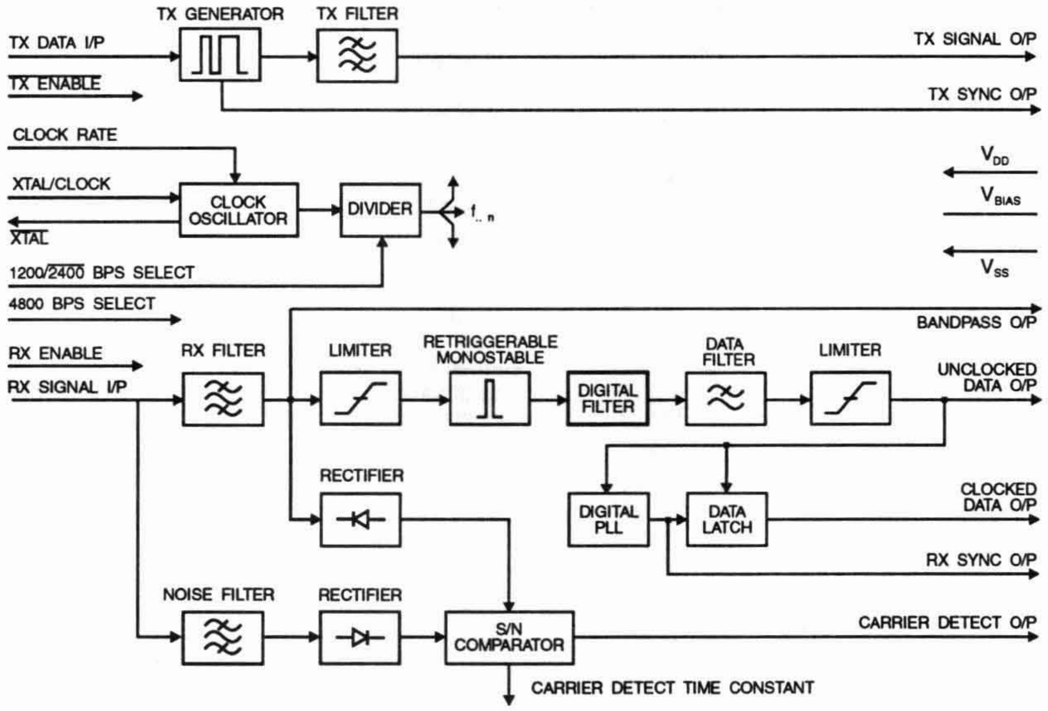
MX469 1200/2400/4800bps MSK Modem

Features

- Selectable Data Rates
  1200/2400/4800bps
- Full-Duplex MSK
- RX and TX Bandpass Filters
- Clock Recovery and
  Carrier Detect Capabilities
- Pin Selected Xtal/Clock Inputs
  1.008MHz or 4.032MHz

Applications

- Radio and General Applications
- Data-Over-Radio
- PMR/Cellular Signaling
- Portable Data Terminals
- Personal/Cordless Telephone


TX GENERATOR
TX FILTER
TX DATA I/P
TX ENABLE
TX SIGNAL O/P
TX SYNC O/P
CLOCK RATE
XTAL/CLOCK
CLOCK OSCILLATOR
DIVIDER
$f_{..n}$
XTAL
1200/2400 BPS SELECT
4800 BPS SELECT
V_{DD}
V_{BIAS}
V_{SS}
BANDPASS O/P
RX ENABLE
RX SIGNAL I/P
RX FILTER
LIMITER
RETRIGGERABLE MONOSTABLE
DIGITAL FILTER
DATA FILTER
LIMITER
UNCLOCKED DATA O/P
RECTIFIER
DIGITAL PLL
DATA LATCH
CLOCKED DATA O/P
RX SYNC O/P
NOISE FILTER
RECTIFIER
S/N COMPARATOR
CARRIER DETECT O/P
CARRIER DETECT TIME CONSTANT

The MX469 is a full-duplex pin-selectable 1200/2400/4800bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800, 1200/2400, and 2400/4800Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. The use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies, and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The MX469 includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins. RX, TX, and Carrier Detect circuits contain bandpass filters to provide high quality signals in their respective paths. The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

The MX469 demonstrates high sensitivity and good bit-error-rate under adverse signal conditions.

This low-power device requires few external components and is available in the following packages: 24-pin SOIC (MX469DW), 22-pin PDIP (MX469P), and 20-pin SOIC (MX469D3).

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MXCOM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

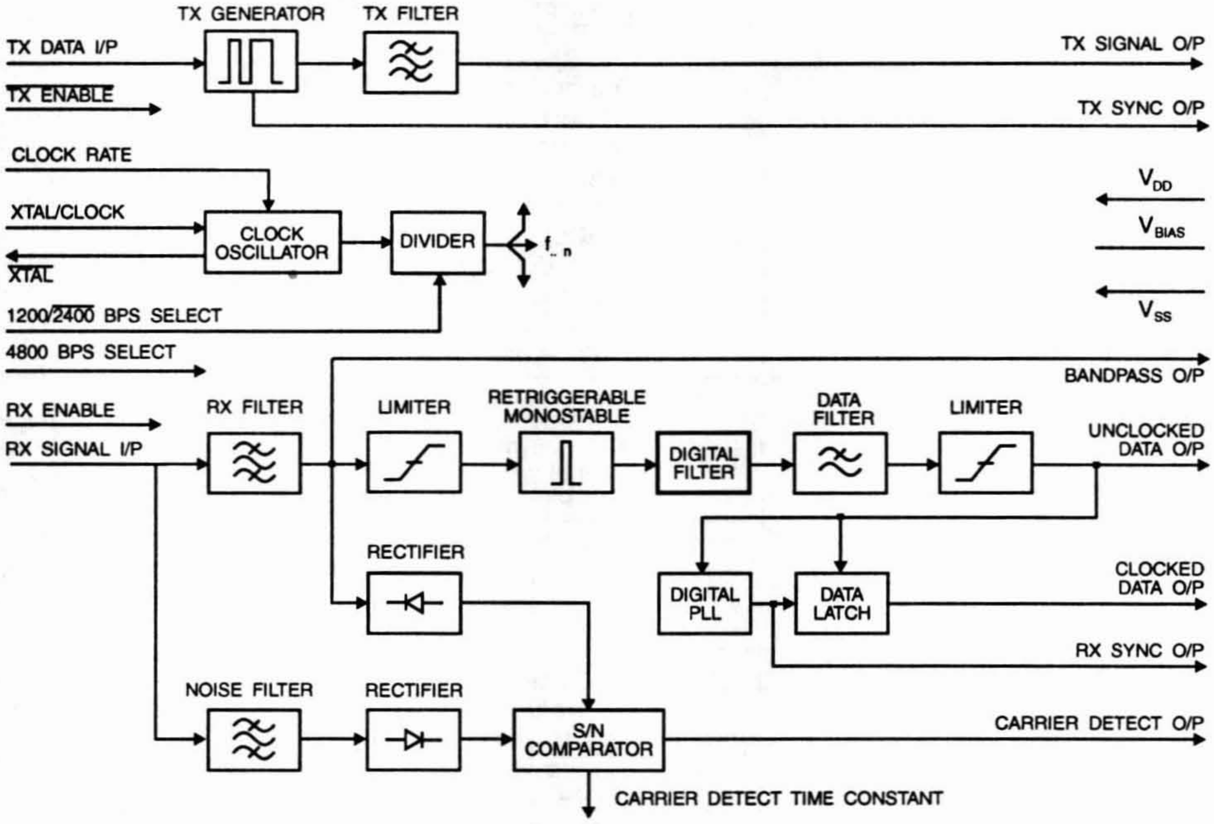

TX GENERATOR
TX FILTER
TX DATA I/P
TX ENABLE
TX SIGNAL O/P
TX SYNC O/P
CLOCK RATE
XTAL/CLOCK
CLOCK OSCILLATOR
DIVIDER
f.. n
XTAL
V_{DD}
V_{BIAS}
V_{SS}
1200/2400 BPS SELECT
4800 BPS SELECT
BANDPASS O/P
RX ENABLE
RX SIGNAL I/P
RX FILTER
LIMITER
RETRIGGERABLE MONOSTABLE
DIGITAL FILTER
DATA FILTER
LIMITER
UNCLOCKED DATA O/P
RECTIFIER
DIGITAL PLL
DATA LATCH
CLOCKED DATA O/P
RX SYNC O/P
NOISE FILTER
RECTIFIER
S/N COMPARATOR
CARRIER DETECT O/P
CARRIER DETECT TIME CONSTANT

Figure 1: Block Diagram

2. Signal List

			Signal	Type	Description
P	DW	D3			
1	1	1	Xtal/Clock	input	The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to Table 3. Operation of any MX•COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) be installed on the power supply (V_{DD}).
2	2	2	$\overline{\text{Xtal}}$	output	Output of the on-chip inverter.
3	3	3	TX Sync	output	A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the MSK signal (See Figure 3).
5	5	4	TX Signal	output	When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) MSK signal (See Figure 3). With the transmitter disabled, this output is set to a high-impedance state.
6	7	5	TX Data	input	Serial logic data to be transmitted is input to this pin.
7	8	6	$\overline{\text{TX Enable}}$	Input	A logic '0' will enable the transmitter (See Figure 3). A logic '1' at this input will put the transmitter into powersave while forcing "TX Sync Out" to a logic '1' and "TX Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
8	9	7	Bandpass	output	The output of the RX Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
9	10	8	RX Enable	Input	The control of the RX function. The control of other outputs is provided in Table 2
10	11	9	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C2). See Figure 2 and RX Enable notes. This bias voltage is maintained under all powersave conditions.
11	12	10	V_{SS}	power	Negative supply (GND).
12	13	11	Unclocked Data	output	The recovered asynchronous serial data output from the receiver.
13	14	12	Clocked Data	output	The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "RX Sync O/P". (See Figure 4 and Figure 6).
14	15	13	Carrier Detect	output	For 1200 and 2400bps operation only. When an MSK signal is being received this output is a logic '1'. The Carrier Detect signal should be ignored during 4800bps operation.
15	16	14	RX Signal	input	The MSK signal input for the receiver. This input should be coupled via a capacitor, C3.

			Signal	**Type**	**Description**
P	**DW**	**D3**			
17	18	15	RX Sync	output	A flywheel squarewave output. This clock will synchronize to incoming RX MSK data. (See Figure 4 and Figure 6).
16	19	16	1200/$\overline{2400}$ BPS Select	input	A logic '1' on this pin selects the 1200bps option; tone frequencies are one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400bps option; tone frequencies are one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pull-up resistor. Operational Data Rate Configurations are illustrated in Table 3
18	20	17	4800 BPS Select	input	A logic '1' on this pin combined with a logic '0' on the 1200/2400 BPS Select pin will select the 4800 option (1MΩ pulldown resistor). Tone frequencies are: one-half cycle of 2400Hz represents a logic '1', one half cycle of 4800Hz represents a logic '0'. This state can only be achieved using a 4.032MHz Xtal input. Operational Data Rate Configurations are illustrated in Table 3
19	21	18	Clock Rate	input	A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
20	23	19	Carrier Detect Time Constant	output	Part of the carrier detect integration function. The value of C4 connected to this pin will affect the carrier detect response time and therefore the noise performance (See Figure 2, Note 3).
22	24	20	V_{DD}	power	Positive supply. A single 5-volt supply is required.
4, 21	4, 6, 17, 22		N/C		No Internal Connection.

Table 1: Signal List

RX Enable	=	RX Function	Clock Data Output	Carrier Detect	Rx Sync Out
1	=	Enabled	Enable	Enabled	Enabled
0	=	Powersave	0	0	1 or 0

Table 2: RX Enable Control Functions

XTAL/CLOCK Frequency	1.008MHz		4.032MHz		
Clock Rate pin	0	0	1	1	1
1200/2400 Select Pin	1	0	1	0	0
4800 Select Pin	0	0	0	0	1
Data Rate (bps)	1200	2400	1200	2400	4800

Table 3: Operational Data Rate Configuration

3. External Components

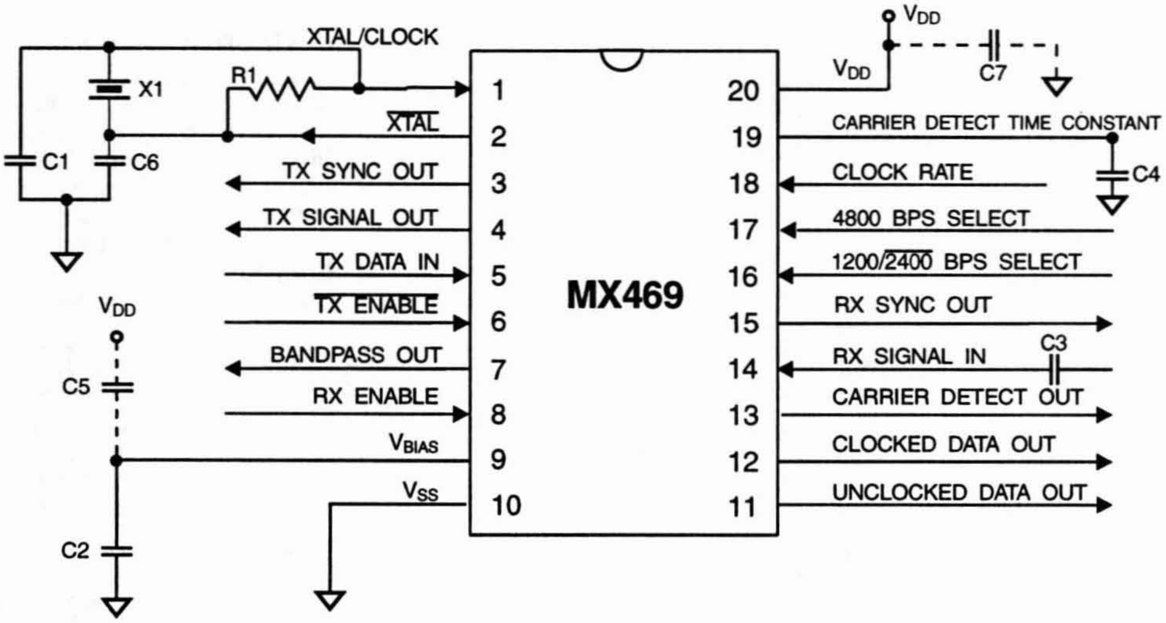

XTAL/CLOCK
X1
R1
XTAL
C1
C6
TX SYNC OUT
TX SIGNAL OUT
TX DATA IN
TX ENABLE
BANDPASS OUT
RX ENABLE
V_{BIAS}
V_{SS}
V_{DD}
C5
C2
MX469
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
V_{DD}
V_{DD}
C7
CARRIER DETECT TIME CONSTANT
CLOCK RATE
C4
4800 BPS SELECT
1200/2400 BPS SELECT
RX SYNC OUT
RX SIGNAL IN
C3
CARRIER DETECT OUT
CLOCKED DATA OUT
UNCLOCKED DATA OUT

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
C1		33pF	±5%
C2		1.0µF	±20%
C3		0.1µF	±20%
C4	Note 1	0.1µF	±10%
C5	Note 2	1.0µF	±25%
C6	Note 3	33pF	±5%
C7	Note 2	1.0µF	±20%
X1	Note 4	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Table 4: Recommended External Components

Notes:

1. The value of C4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
2. Decoupling circuits depend upon whether the input signal is referenced to V_{BIAS} or V_{SS}. Use C5 when the input signal is referenced to V_{BIAS}. Use C7 when the input signal is referenced to V_{SS}. It is not necessary to use both C5 and C7.
3. C6 reduces Xtal voltage overshoot. Reference the MX-COM Xtal Application Note.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Timing

4.1.1 1200bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			416		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		800	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TXD}			1.2		µs
TX Data Rate Period	t_{TDR}			833		µs
RX Data Rate Period	t_{RDR}		800		865	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/clock tolerance.
2. All TX timings are related to the TX Sync Output.

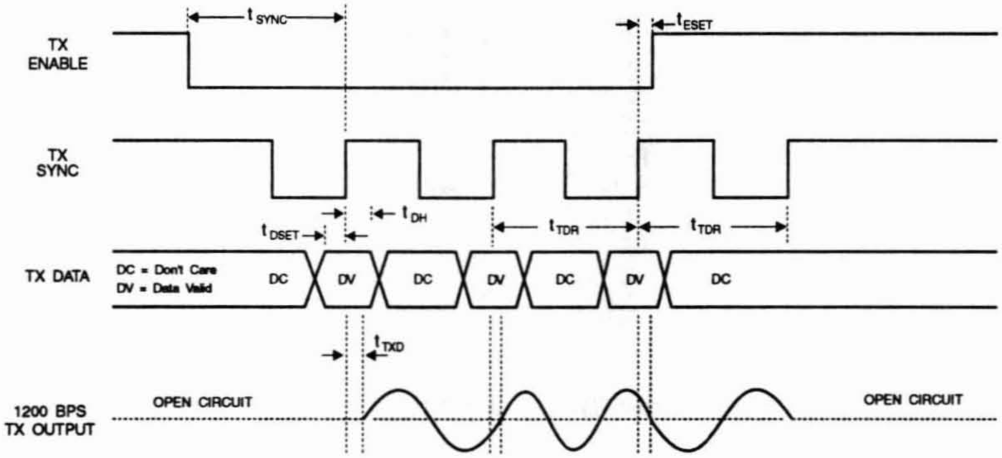

TX ENABLE
t SYNC
t ESET
TX SYNC
t DSET
t DH
t TDR
t TDR
TX DATA
DC = Don't Care
DV = Data Valid
DC
DV
DC
DV
DC
DV
DC
t TXD
OPEN CIRCUIT
OPEN CIRCUIT
1200 BPS TX OUTPUT

Figure 3: Transmitter Timing: 1200bps

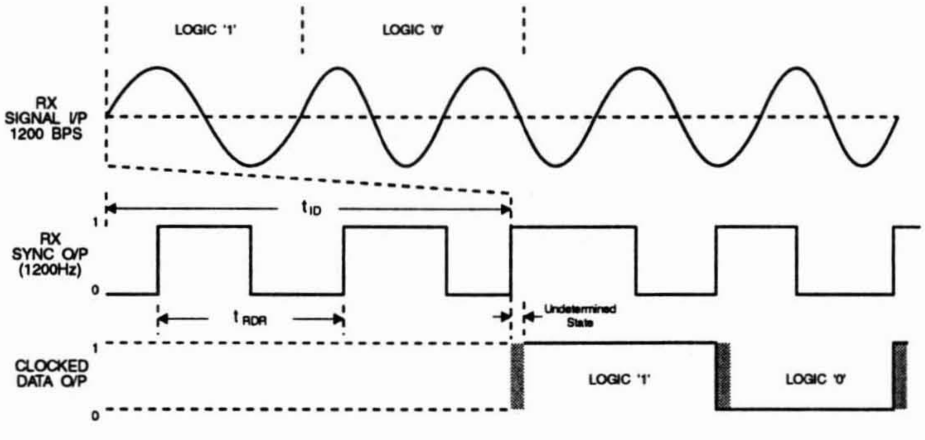

LOGIC '1'
LOGIC '0'
RX SIGNAL I/P 1200 BPS
t ID
1
RX SYNC O/P (1200Hz)
0
t RDR
Undetermined State
1
CLOCKED DATA O/P
0
LOGIC '1'
LOGIC '0'

Figure 4: Receiver Timing Diagram: 1200bps

4.1.2 2400bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			208		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		400	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			416		µs
RX Data Rate Period	t_{RDR}		400		433	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

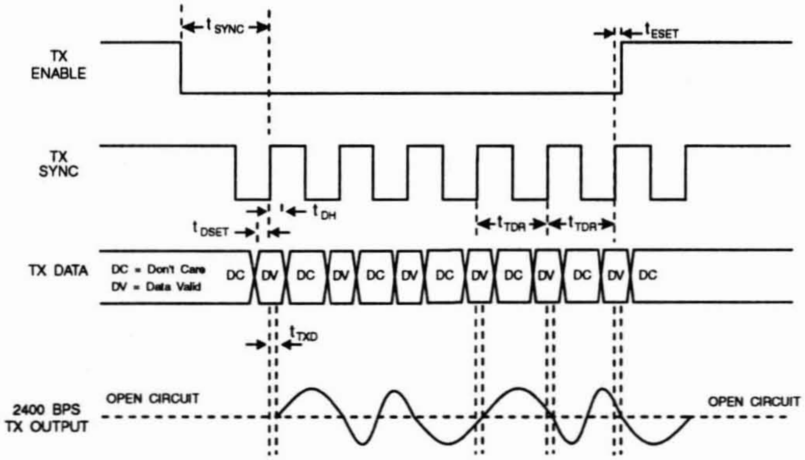

t SYNC
t ESET
TX ENABLE
TX SYNC
t DSET
t DH
t TDR
t TDR
TX DATA
DC = Don't Care
DV = Data Valid
DC
DV
t TXD
2400 BPS TX OUTPUT
OPEN CIRCUIT
OPEN CIRCUIT

Figure 5: Transmitter Timing: 2400bps

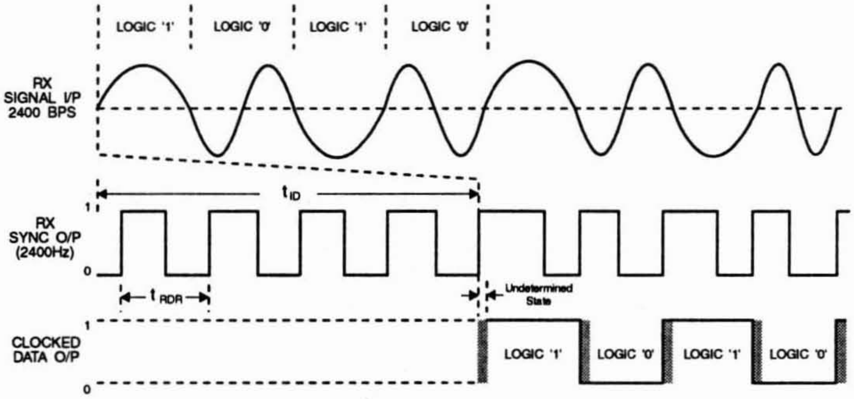

LOGIC '1'
LOGIC '0'
LOGIC '1'
LOGIC '0'
RX SIGNAL I/P 2400 BPS
t ID
RX SYNC O/P (2400Hz)
1
0
t RDR
Undetermined State
CLOCKED DATA O/P
1
0
LOGIC '1'
LOGIC '0'
LOGIC '1'
LOGIC '0'

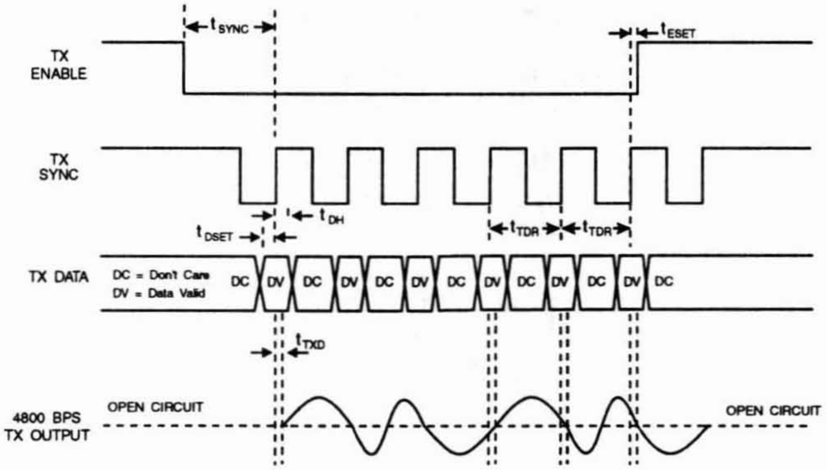
Figure 6: Receiver Timing: 2400bps

4.1.3 4800bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			104		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		200	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			208		µs
RX Data Rate Period	t_{RDR}		200		216	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.0		ms

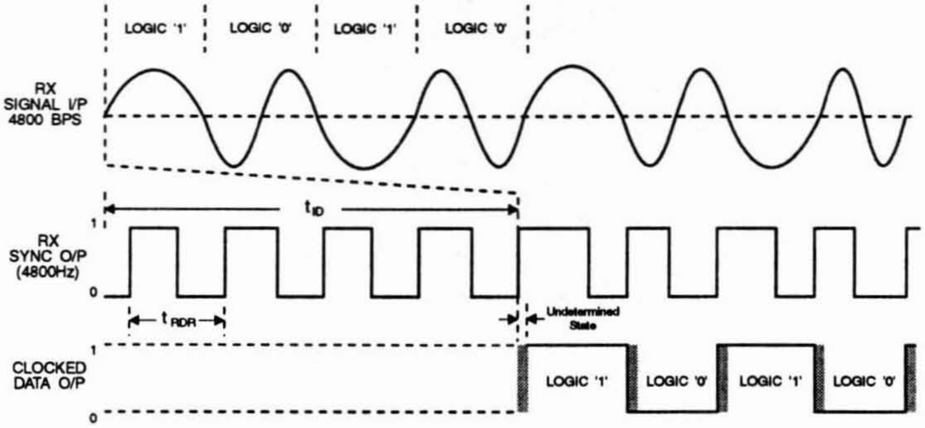
Notes:

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.



t SYNC
t ESET
TX ENABLE
TX SYNC
t DH
t DSET
t TDR
t TDR
TX DATA
DC = Don't Care
DV = Data Valid
DC
DV
t TXD
OPEN CIRCUIT
4800 BPS TX OUTPUT
OPEN CIRCUIT

Figure 7: Transmitter Timing: 4800bps



LOGIC '1'
LOGIC '0'
LOGIC '1'
LOGIC '0'
RX SIGNAL I/P 4800 BPS
t ID
1
RX SYNC O/P (4800Hz)
0
t RDR
Undetermined State
1
CLOCKED DATA O/P
0
LOGIC '1'
LOGIC '0'
LOGIC '1'
LOGIC '0'

Figure 8: Receiver Timing: 4800bps

5. Application

5.1 Synchronous Modem Design Considerations

The MX469 is an easily applied data pump, which can be used with many protocols. Because it is an MSK, or minimum shift keying, modem, it achieves a more noise resistant, higher data rate in a narrower bandwidth than other FSK (frequency shift keying) modems. This characteristic is especially important for wireless applications because it fundamentally determines the bandwidth of RF transmissions, which are strictly limited and controlled by regulatory agencies. Using MSK signaling, the MX469 data modem can achieve a 2400bps data rate within the typical 300-3000 Hz voice band of many common radios.

In order to achieve this advantage, an MSK modem must precisely control the bit rate and timing of the modulated Tx output signal bits. This control is asserted by the MSK modem with a data clock signal, which is output, by the modem to pace the Tx data source (e.g. a microcontroller). The data clock signal, in effect, indicates when the Tx data source should provide the next Tx data bit to the modem. See Figure 9. Because this type of interface involves the use of a modem generated bit clock signal to control the timing of when new Tx data bits must be supplied from the data source, the interface is called synchronous.

Another characteristic of a synchronous modem is that, to receive data, it must first learn the data bit timing of the Rx signal stream before it can accurately demodulate Rx data bits. Accordingly, a synchronous modem undergoes a period of training or synchronization when it first begins to receive a stream of MSK modulated signal. During this initial receive phase, the received signal is evaluated over several bit times as the modem 'locks on' and achieves proper receive synchronization. The training sequence, called a preamble, is a specific data pattern which must be added to the 'front' of a transmit data stream with the start of each new transmission. A specific preamble data pattern (e.g. 16 bits of alternating 0,1,0,1... for the MX469) is used to optimize the training accuracy while minimizing the number of preamble bits required.

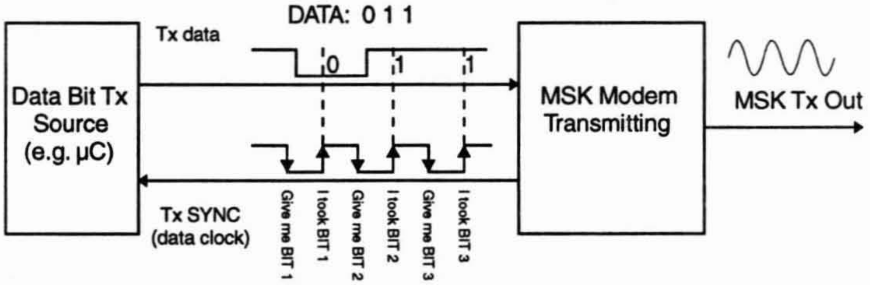


Figure 9: Synchronous Transmit Operation

Non-synchronous or asynchronous interfaces are commonly found in wired applications which do not have the bandwidth efficiency requirements of wireless systems. A well known example is the serial port of a personal computer which can transmit a 1200 bps (or faster) data signal over a single Tx signal without using an additional data clock signal to control the precise rate and timing of data bits being transmitted to a typical telephone line data modem. Popular modem standards such as Bell 202 and v.23 use FSK signaling to pass such asynchronous serial port data signals over telephone systems.

Another aspect of asynchronous interfaces and modems is that they can carry data streams which are not at the exact, nominal data rate. For example, a 1200 bps FSK modem will typically operate properly when supplied with transmit data streams of 1201 bps or 1199 bps.

Because of the differences in synchronous and asynchronous interfaces, they cannot successfully operate if directly connected. In other words, a personal computer's RS232 serial port cannot directly interface to an MSK modem. This is because:

- The asynchronous interface may provide data bits too fast or too slow compared to the precise rate required for MSK signaling (a bit rate, or pacing, incompatibility).
- The timing of each specific data bit presented by an asynchronous interface will not be aligned with the precise bit timing required for MSK signaling (a bit timing incompatibility).

Synchronous and asynchronous interface can be successfully interfaced for applications requiring the advantages of both. This typically involves the use of data buffering and retiming circuits to resolve the timing and pacing issues.

5.2 Bit Error Rate

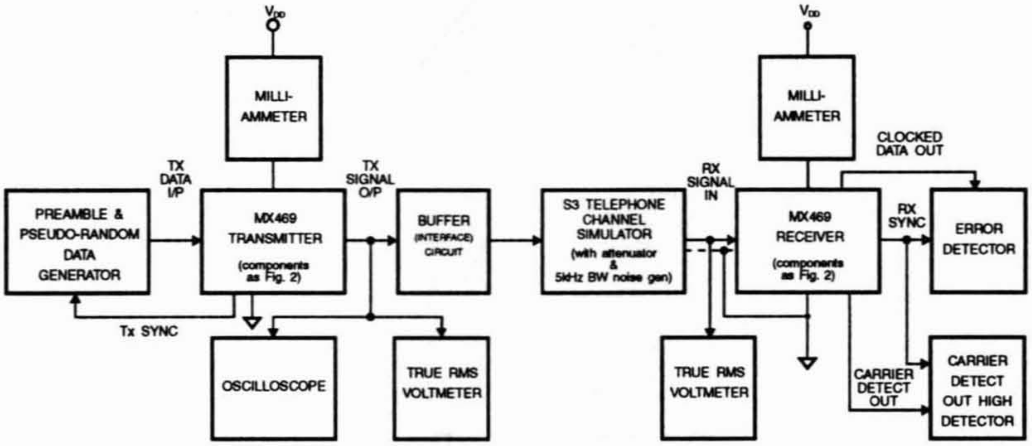

VDD
MILLI-AMMETER
TX DATA I/P
PREAMBLE & PSEUDO-RANDOM DATA GENERATOR
MX469 TRANSMITTER (components as Fig. 2)
Tx SYNC
TX SIGNAL O/P
BUFFER (INTERFACE) CIRCUIT
OSCILLOSCOPE
TRUE RMS VOLTMETER
S3 TELEPHONE CHANNEL SIMULATOR (with attenuator & 5kHz BW noise gen)
RX SIGNAL IN
TRUE RMS VOLTMETER
VDD
MILLI-AMMETER
MX469 RECEIVER (components as Fig. 2)
CLOCKED DATA OUT
RX SYNC
ERROR DETECTOR
CARRIER DETECT OUT
CARRIER DETECT OUT HIGH DETECTOR

Figure 10: MX469 Test Set-Up

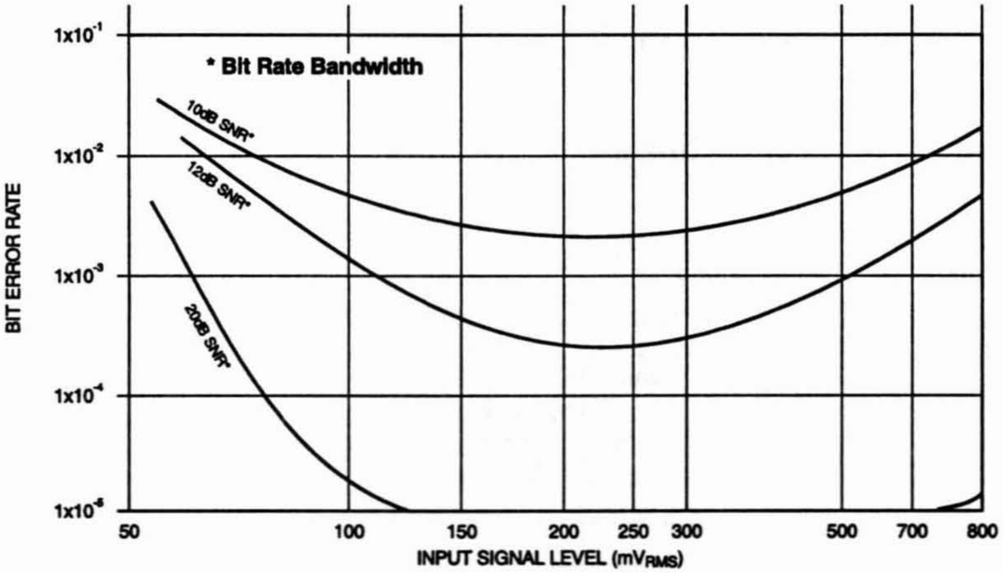


Figure 11: Typical Variation of Bit Error Rate with Input Level

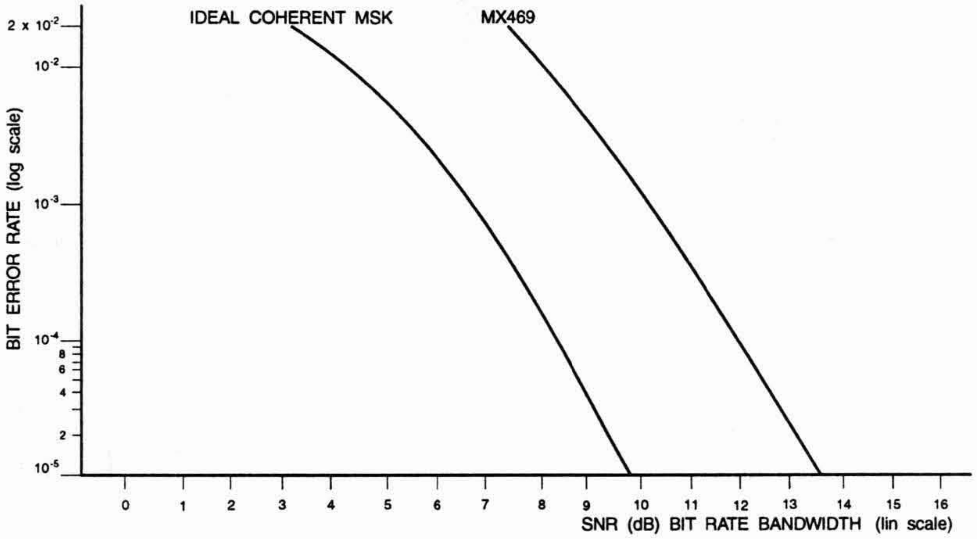


Figure 12: RX Bit-Error-Rate vs. Signal-to-Noise Ratio

6. Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
DW / D3 / P Packages					
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency		1.008		4.032	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB ref. = 300mV_{RMS}, Xtal/Clock Frequency = 4.032MHz
Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth
1200bps BRB = 1200Hz
2400bps BRB = 2400Hz
4800bps BRB = 4800Hz

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
RX Enabled, TX Disabled			3.6		mA
RX and TX Enabled			4.5		mA
RX and TX Disabled			650		µA
Logic '1' Level	1	4.0			V
Logic '0' Level	1			1.0	V
Digital Output Impedance			4.0		kΩ
Analog and Digital Input Impedance		100			kΩ
TX Output Impedance			0.6	1.0	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0			MΩ
R_{OUT}			10.0		kΩ
Inverter DC Voltage Gain			10.0		V/V
Gain Bandwidth Product			10.0		MHz
Dynamic Values					
Receiver					
Signal Input Dynamic Range					
SNR = 50dB	3, 4	100	230	1000	mV_{RMS}
Bit Error Rate					
SNR = 12dB	4		7.0		10^{-4}
1200bps			2.5		10^{-4}
2400bps			1.5		10^{-3}
4800bps			1.5		10^{-3}
SNR = 20dB	4				
1200/2400/4800bps			1.0		10^{-8}
Receiver Synchronization **SNR =12dB**	7				
Probability of Bit 8 Being Correct			99		%
Probability of Bit 16 Being Correct			99.5		%
Carrier Detect	5, 10				
Sensitivity	7, 8			150	mV_{RMS}
Probability of C.D. Being High					
After Bit 8 (1200bps) SNR = 12dB	5, 9		98		%
After Bit 16 SNR = 12dB	5, 9		99.5		%
0dB Noise No Signal	9		5		%

	Notes	Min.	Typ.	Max.	Units
Transmitter Output					
TX Output Level			775		mV_{RMS}
Output Level Variation					
1200/1800Hz		0		±1.0	dB
1200/2400Hz		0		±1.0	dB
2400/4800Hz		0		±1.0	dB
Output Distortion			3.0	5.0	%
3rd Harmonic Distortion			2.0	3.0	%
Logic '1' Carrier Frequency					
1200bps	6		1200		Hz
2400bps	6		1200		Hz
4800bps	6		2400		Hz
Logic '0' Carrier Frequency					
1200bps	6		1800		Hz
2400bps	6		2400		Hz
4800bps	6		4800		Hz
Isochronous Distortion					
1200Hz - 1800Hz/1200Hz - 2400Hz			25.0	40.0	µs
1800Hz - 1200Hz/2400Hz - 1200Hz			20.0	40.0	µs
2400Hz - 4800Hz/4800Hz - 2400Hz			10.0	20.0	µs

Operating Characteristics Notes:

1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 4 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mV_{RMS} input signal (no noise).
9. Reference (0dB) level for C.D. probability measurements is 230mV_{RMS}.
10. For 1200bps and 2400bps operation only: when operating at 4800bps the carrier detect output should be ignored.

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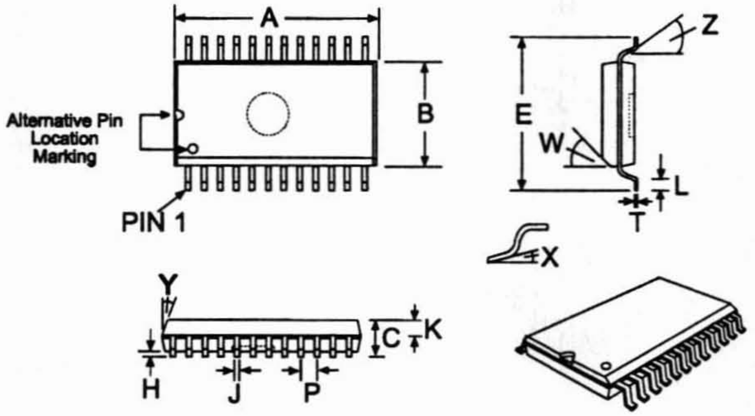
6.1.4 Packages

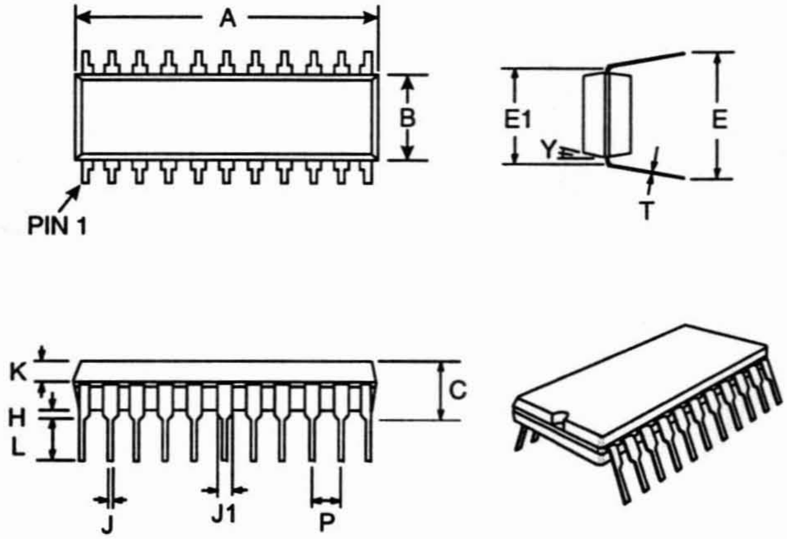


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin SOIC Mechanical Outline: Order as part no. MX469DW

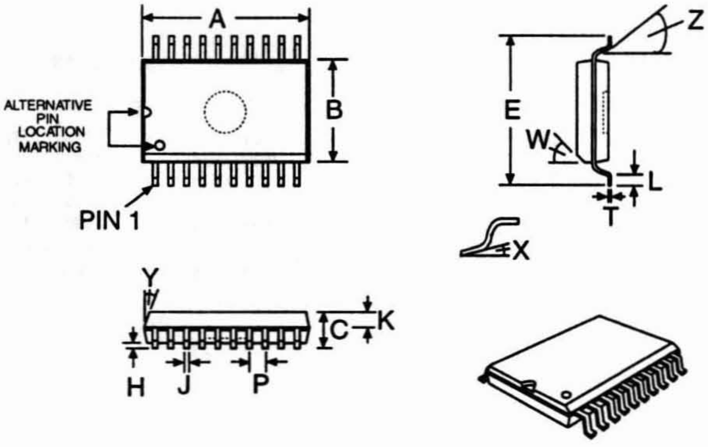


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 22-pin PDIP Mechanical Outline: ***Order as part no. MX469P***


A
B
ALTERNATIVE PIN LOCATION MARKING
PIN 1
Y
C
K
H
J
P
Z
E
W
L
T
X

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.495 (12.57)		0.510 (12.95)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 20-pin SOIC Mechanical Outline: ***Order as part no. MX469D3***

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX604 v.23 Compatible Modem

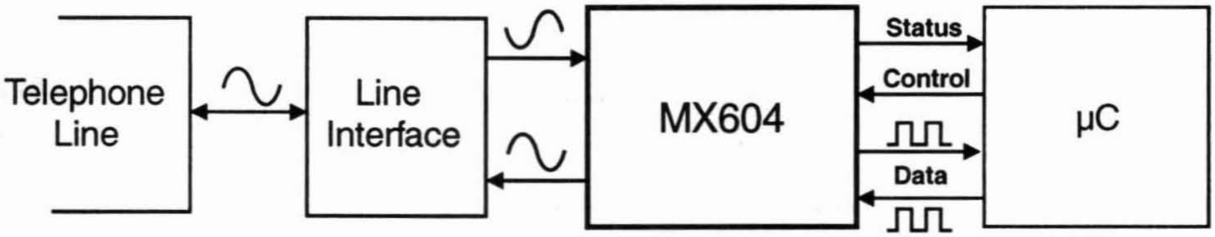
PRELIMINARY INFORMATION

FEATURES

- 1200bps forward, 75bps back channels
- Conforms to relevant sections of v.23 and ETSI specifications
- Line Equalization
- 1200bps Data Retiming Facility can eliminate external UART
- Low Voltage Operation (3.3 to 5.0V)

APPLICATIONS

- Low Power Operation
  - 1mA typ. @ 3.3V Operating Mode
  - 1µA typ. Zero-Power Mode
- Standard 3.58Mhz Xtal/Clock
- Telephone Telemetry System Applications



The MX604 is a low voltage, low power CMOS device, used for the reception or transmission of asynchronous 1200bps data and full-duplex 75bps back channel data in accordance with CCITT V.23 and ETSI specifications.

This device provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for an external UART when operating at 1200bps. The device can disable the back channel or be operated so only the mark or space tone is produced. The optional line equalizer is incorporated into the receive path and is controlled by an external logic level.

The MX604 may be used in a wide range of telephone telemetry systems. Low voltage capability, a low operating current (1mA typ. @ V_{DD} = 3.3V), and a very low current 'sleep' mode (1µA typ.) make the MX604 ideal for both portable terminal and line powered applications.

The MX604 is available in the following packages: 24-pin TSSOP (MX604TN), 16-pin SOIC (MX604DW) and 16-pin PDIP (MX604P).

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2. **Signal List** ..... **3 - 320**
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    - 4.3 Rx Input Amplifier ..... 3 - 322
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MX•COM, Inc. reserves the right to change specifications at any time and without notice

1. Block Diagram

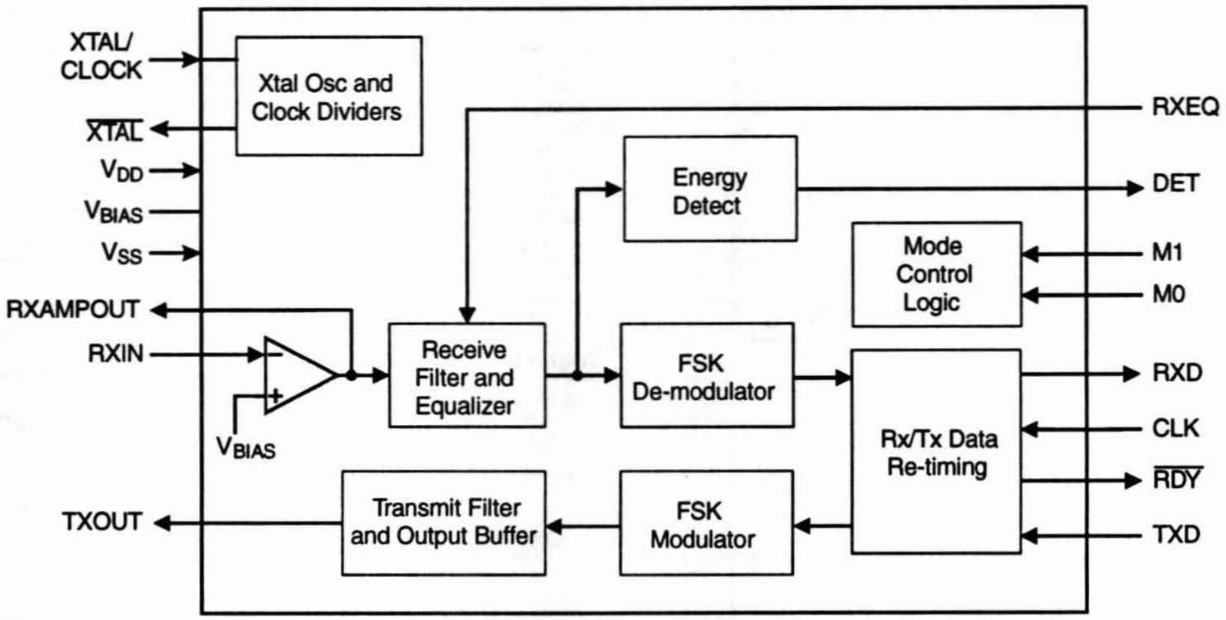

XTAL/ CLOCK
$\overline{XTAL}$
V_{DD}
V_{BIAS}
V_{SS}
RXAMPOUT
RXIN
V_{BIAS}
TXOUT
Xtal Osc and Clock Dividers
Energy Detect
Mode Control Logic
Receive Filter and Equalizer
FSK De-modulator
Rx/Tx Data Re-timing
Transmit Filter and Output Buffer
FSK Modulator
RXEQ
DET
M1
M0
RXD
CLK
$\overline{RDY}$
TXD

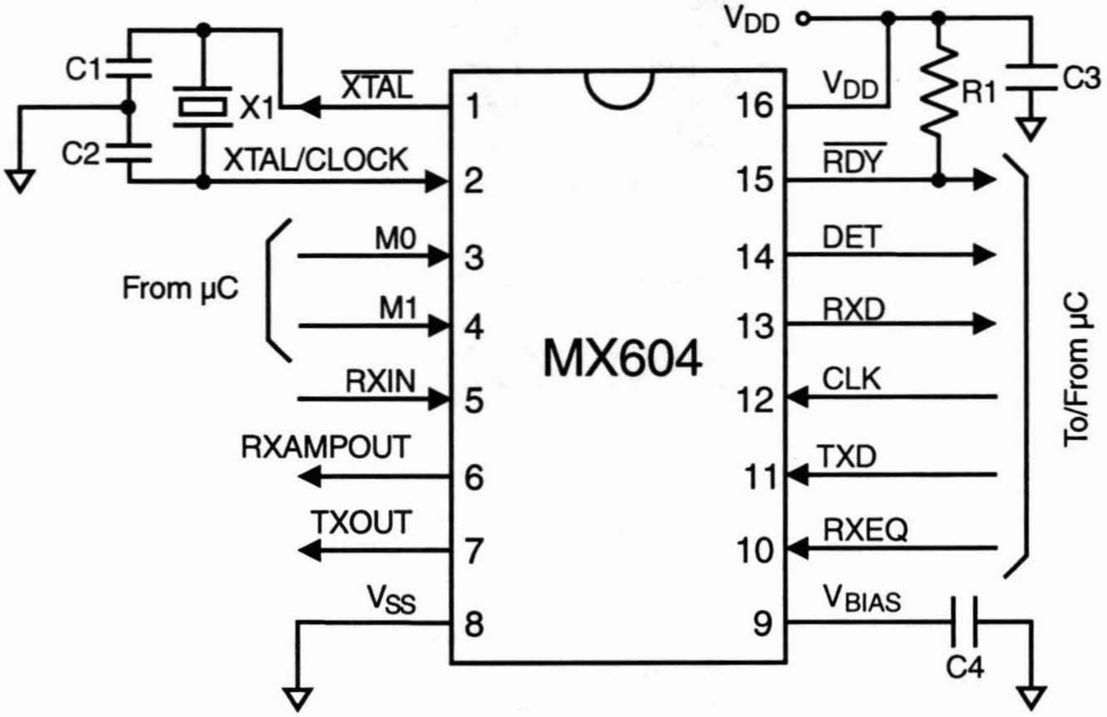
Figure 1: Block Diagram

2. Signal List

Pin No.		Name	Type	Description
P, DW	TN			
1	1	$\overline{\text{XTAL}}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier.
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at V_{DD} /2 when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in/out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip energy detect circuit.
15	23	$\overline{\text{RDY}}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10 ,15, 16, 21, 22	N/C		No internal connections

This device is capable of detecting and decoding small amplitude signals. Achieving the V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that decoupling capacitors be placed so the connection between them and the device pins is as short as possible. A ground plane protecting the receive path will help attenuate interfering signals.

3. External Components



R1		100kΩ	±5%,
C1, C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX604 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or it may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be used.

The on-chip oscillator is disabled in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX604 as well as generating undefined states of the RXD, DET and $\overline{RDY}$ outputs.

4.2 Mode Control Logic

The MX604's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	75bps	Rx
0	1	off	1200bps	Tx
1	0	1200bps	off	Rx
1	1	'Zero-Power'		-

[1] If enabled.

Note: On applying power to the device the mode must be set to 'ZP', i.e. M0=1, M1=1, until V_{DD} has stabilized.

In the 'Zero-Power' mode, power is removed from all internal circuitry. When leaving 'Zero-Power' mode there must be a 20ms delay before any Tx data is passed to, or Rx data read from, the device to allow the bias level, filters and oscillator to stabilize.

4.3 Rx Input Amplifier

The Rx Input Amplifier is used to adjust the signal received to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer is used to attenuate out of band noise and interfering signals, especially the locally generated 75bps transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

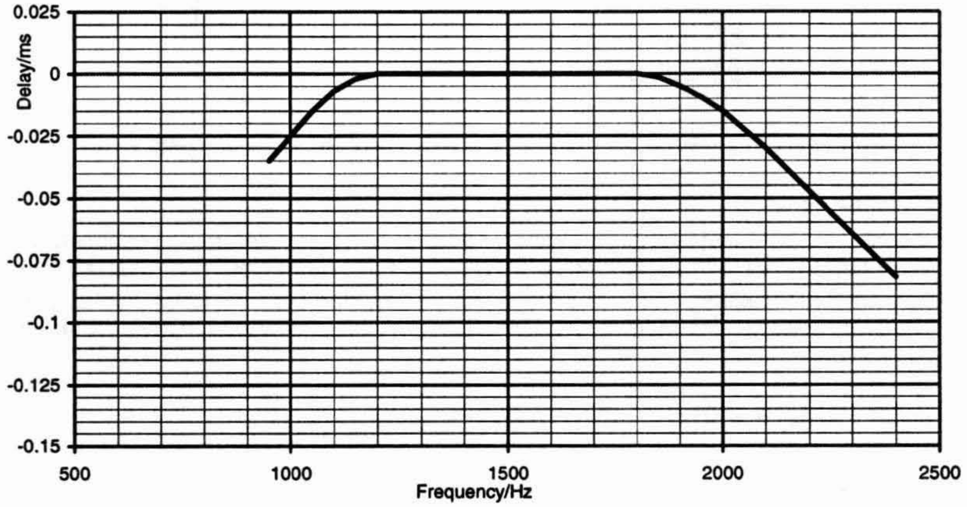


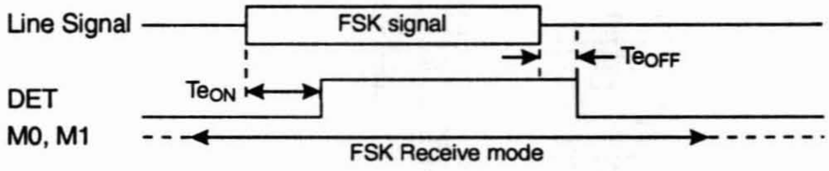
Figure 3: Rx Equalizer Group Delay (RXEQ = 1) with respect to 1700Hz

4.5 Energy Detector

The Energy Detector block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: This circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

The FSK Demodulator block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'off' or in 'ZP' the DET and RXD pins are held low.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin be read only when data is expected.

4.7 FSK Modulator and Transmit Filter

The FSK Modulator and Transmit Filter blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	
1	0	0Hz[1]	
0	0	450Hz	390Hz
0	1	2100Hz	1300Hz

FSK Modulator and Transmit Filter Note:

[1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

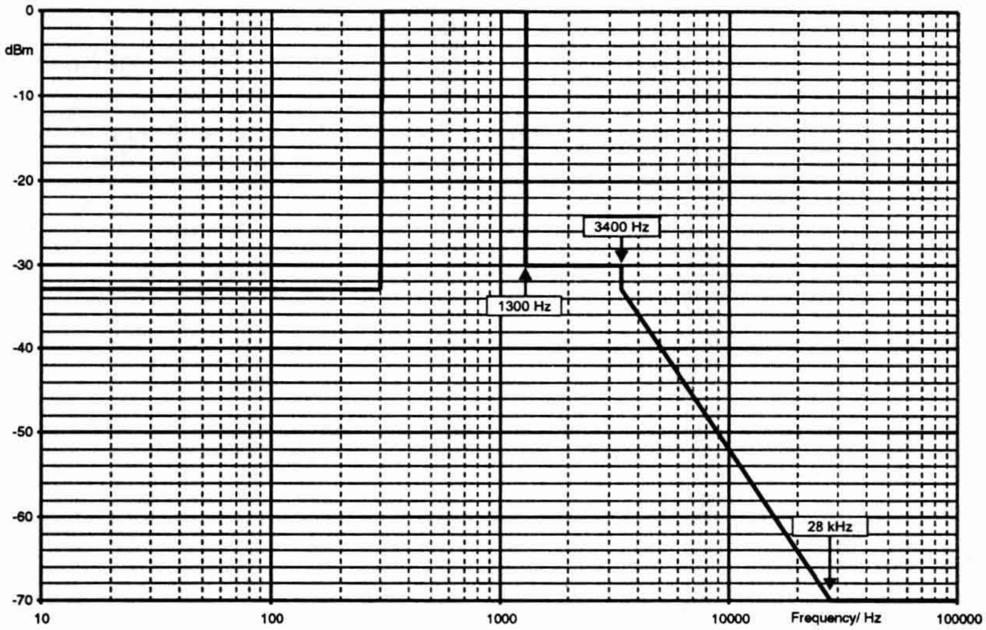


Figure 5: Tx limits at 75bps rate

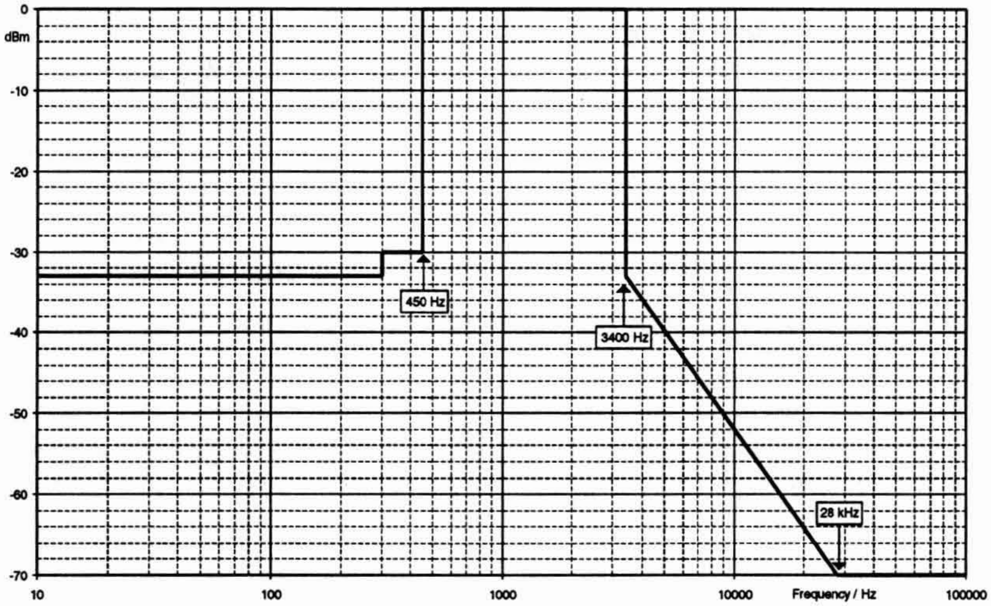


Figure 6: Tx limits at 1200bps rate

4.8 Rx Data Retiming

The Rx Data Retiming function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

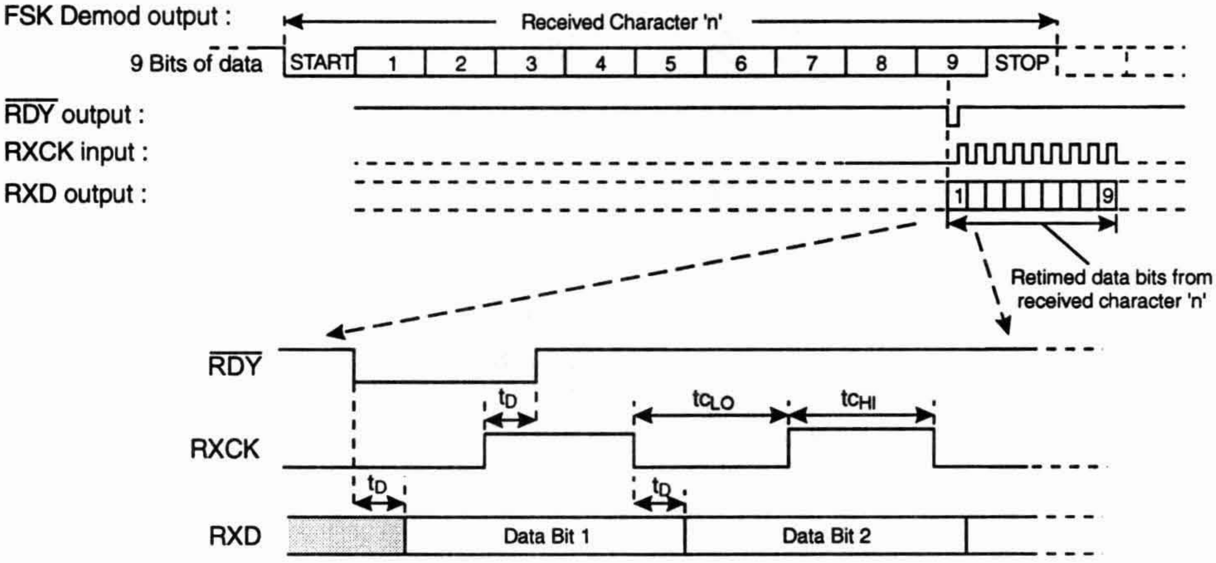
Data bits	Parity bits	Stop bits
7	0	≥2
7	1	≥1
8	0	≥1
8	1	≥1
9	0	≥1

When enabled in receive mode, the Data Retiming block extracts the first 9 bits of each character following the start bit, from the received asynchronous data stream, and presents them to the µC, under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical. They may be generated easily by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{\text{RDY}}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{\text{RDY}}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

To use the Data Retiming function, the CLK input should be kept low until the $\overline{\text{RDY}}$ output goes low; if the Data Retiming function is not required then the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the µC within the time of a complete character at 1200bps.



t_D = Internal MX604 delay, t_{CHI} = CLK high time, t_{CLO} = CLK low time

Figure 7: FSK Operation with Rx Data Re-timing

e: If enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX604 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{RDY}$ output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8

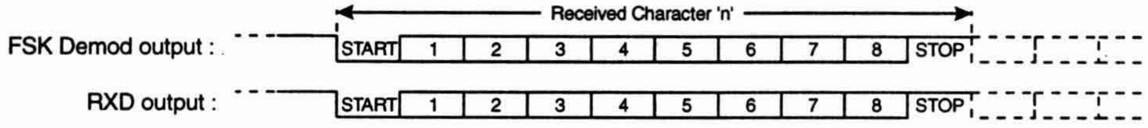


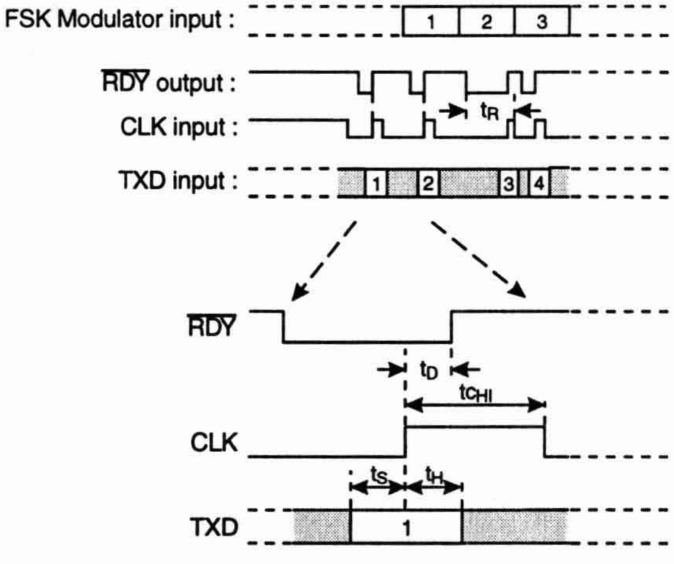
Figure 8: FSK Operation without Rx Data Re-timing (CLK always high)

4.9 Tx Data Retiming

The Tx Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling µC to load 1 bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical. It may be generated easily by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx retiming circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{RDY}$ pin is pulled low. The $\overline{RDY}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

To use the retiming option, the CLK input should be held low until the $\overline{RDY}$ output is pulled low. When the $\overline{RDY}$ pin goes low, the next data bit should be applied to the TXD input and the CLK input pulled high and then low within the time limits defined in Figure 9.



t_D = Internal MX604 delay; t_R = low to CLK going low; t_S = data set up time
t_{CHI} = CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

To ensure synchronization between controlling device and the MX604 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same lo level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, then the CLK input to the MX604 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 75bps data which has no retime option.

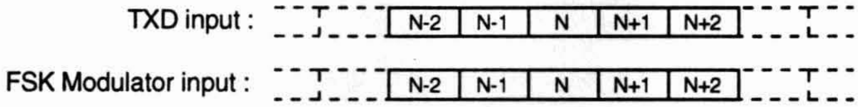

TXD input :
N-2
N-1
N
N+1
N+2
FSK Modulator input :
N-2
N-1
N
N+1
N+2

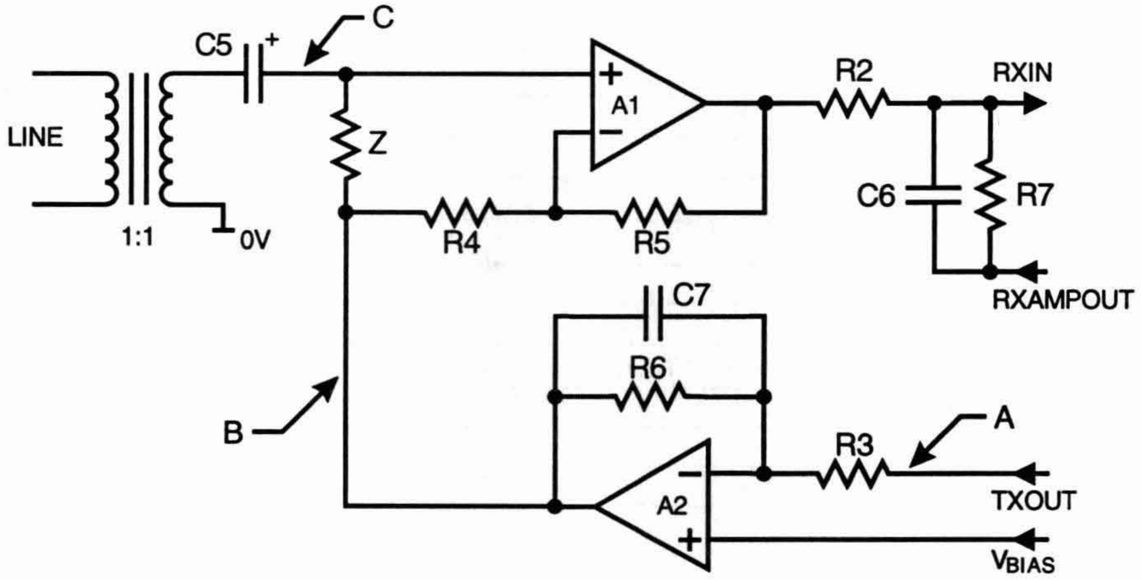
Figure 10: FSK Operation without Tx Data Re-timing (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX604. A Line Interface circuit is necessary to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals


C
C5
+
LINE
1:1
0V
Z
A1
+
−
R2
RXIN
C6
R7
R4
R5
RXAMPOUT
C7
R6
B
A
R3
A2
−
+
TXOUT
VBIAS

R2	See Notes	±1%,
R3	See Notes	±1%,
R4-R7	100kΩ	±1%,

C5	22µF	±20%
C6	100pF	±10%
C7	330pF	±10%

Figure 11: Line Interface Circuit

Line Interface Notes:

- The components 'Z' between points B and C should match the line impedance.
- Device A2 must be able to drive 'Z' and the line.
- R2: For optimum results R2 should be set so that the gain is V_{DD}/5.0, i.e. R2 = 100kΩ at V_{DD} = 5.0V, rising to 150kΩ at V_{DD} = 3.3V.
- R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

'A' = 20Log(VDD/5)
'B' = 'A' + 20Log(100kΩ/R3)
'C' = 'B' - 6

VDD	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C

Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS}, 0dB = 0dBm = 775mV_{RMS} into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0='1', M1='1')	1, 2		1		μA
I_{DD} (M0 or M1='0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1='0') at V_{DD}= 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	μA
Output Logic '1' Level (I_{OH} = 360μA)		V_{DD}-0.4			V
Output Logic '0' Level (I_{OL} = 360μA)				0.4	V
Output 'off' State Current (V_{OUT} = V_{DD})				1.0	μA
FSK Demodulator					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1280	1300	1320	Hz
Space (Logical 0) Frequency		2068	2100	2132	Hz
Valid Input Level Range	3	-40.0		-8.0	dBV
Acceptable Twist (Mark Level WRT Space Level)		-7.0		7.0	dB
Acceptable Signal to Noise Ratio	4	20.0			dB
Level Detector 'On' Threshold Level	3			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level	5	-1.0	0	1.0	dB
Twist (Mark Level WRT Space Level)		-2.0	0	2.0	dB
1200bps (M1='0', M0='1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1297		1303	Hz
Space (Logical 0) Frequency		2097		2103	Hz
75bps (M1='0', M0='0').					
Bit Rate		0	75	76	Baud
Mark (Logical 1) Frequency		388		392	Hz
Space (Logical 0) Frequency		448		452	Hz

	Notes	Min.	Typ.	Max.	Units
Input Amplifier					
Impedance (RXIN Pin)	6	10.0			MΩ
Voltage Gain	6		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	7	100			ns
'Low' Pulse Width	7	100			ns

Operating Characteristics Notes:

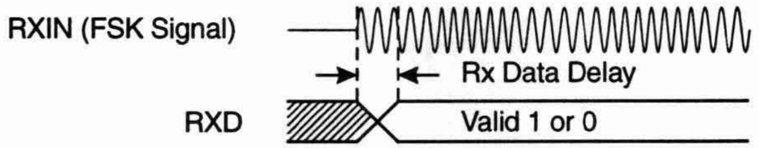
1. Not including any current drawn from the MX604 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1300Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1
4. Flat noise in 300-3400Hz band.
5. Relative to 775mV$_{RMS}$ with V_{DD}= 5.0V for load resistance greater than 40kΩ.
6. Open loop, small signal low frequency measurements.
7. Timing for an external input to the XTAL/CLOCK pin.

6.2 Timing

Data and Mode Timing	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX604 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

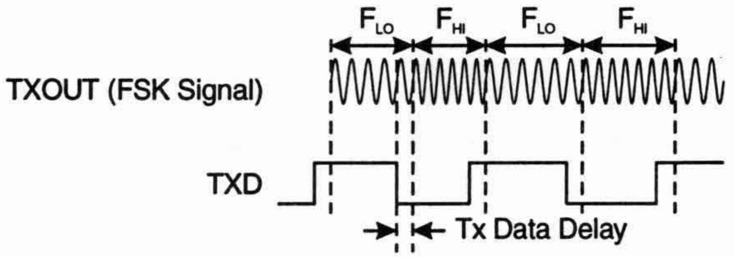
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

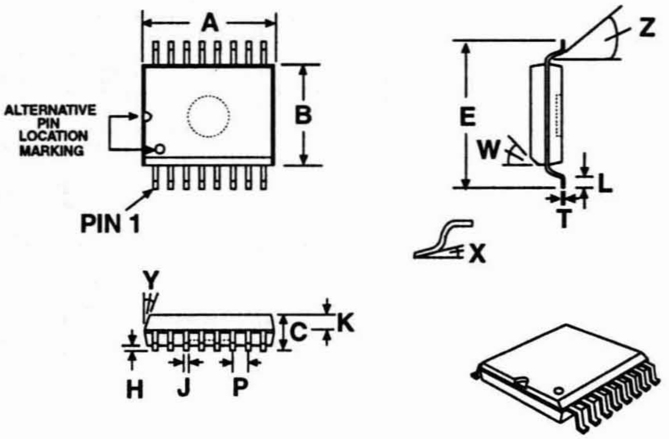
Figure 12: RXIN to RXD Delay time



Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

6.3 Packaging

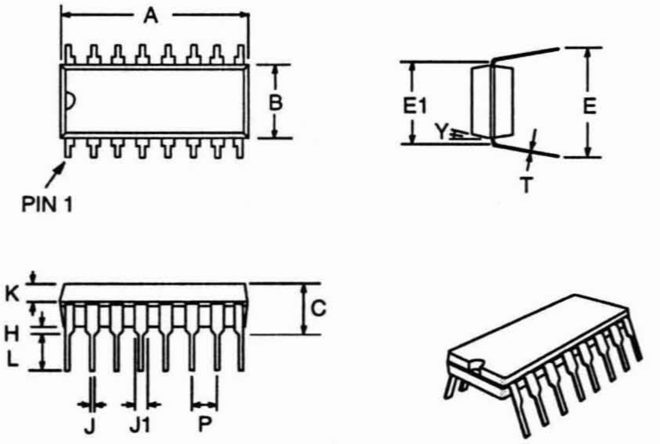


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: ***Order as part no. MX604DW***

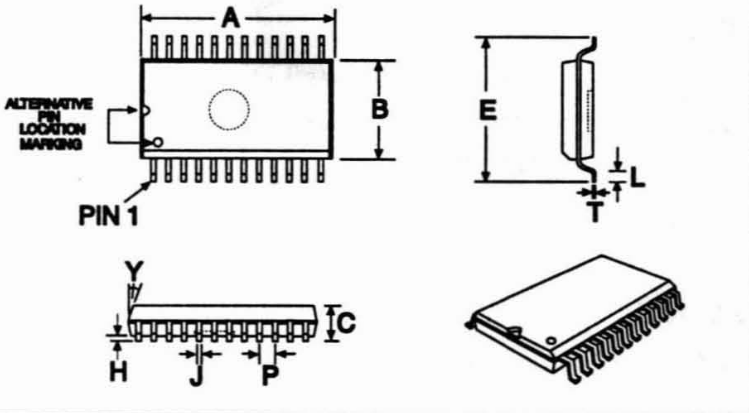


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: ***Order as part no. MX604P***


A
ALTERNATIVE PIN LOCATION MARKING
B
E
L
T
PIN 1
Y
C
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin TSSOP Mechanical outline: ***Order as part no. MX604TN***

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX609

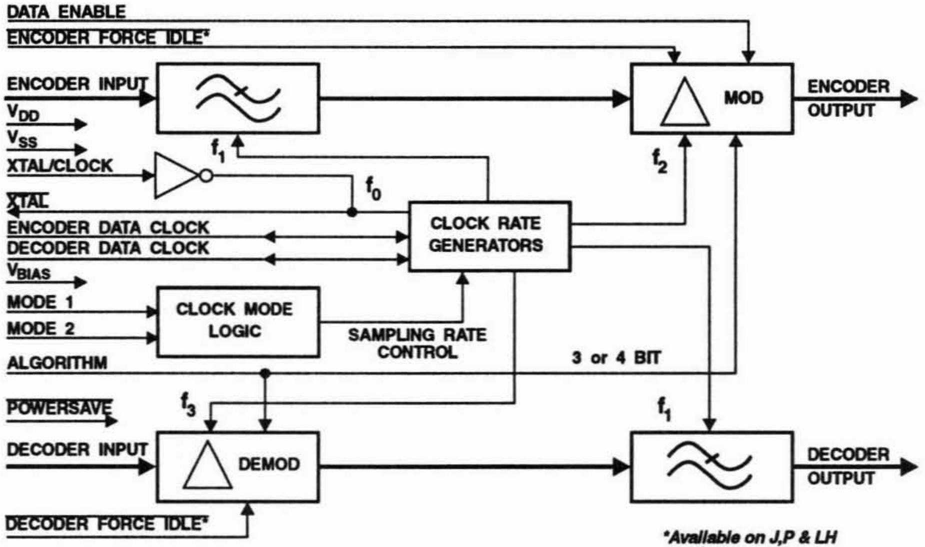
PCN/PCS DELTA MODULATION CODEC

Features

- Single Chip full Duplex CVSD CODEC
- On-chip Input and Output Filters
- Programmable Sampling Clocks
- 3- or 4-bit Companding Algorithm
- Powersave Capabilities
- Low Power, 5.0V Operation

Applications

- Digital PCN/PCS Systems
- Digital Cordless Phones
- Digital Delay Lines
- Digital Voice Storage
- Multiplexers, Switches, and Phones
- Time Domain Scramblers


DATA ENABLE
ENCODER FORCE IDLE*
ENCODER INPUT
VDD
VSS
XTAL/CLOCK
XTAL
ENCODER DATA CLOCK
DECODER DATA CLOCK
VBIAS
MODE 1
MODE 2
ALGORITHM
POWERSAVE
DECODER INPUT
DECODER FORCE IDLE*
f1
f0
f2
f3
f1
MOD
ENCODER OUTPUT
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 or 4 BIT
DEMOD
DECODER OUTPUT

***Available on J,P & LH package styles only**

The MX609 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

Companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode when Powersave is selected.

The MX609 operates with a supply voltage of 5.0V and is available in the following packages: 24-pin PLCC (MX609LH), 16-pin SOIC (MX609DW), 22-pin CERDIP (MX609J), and 22-pin PDIP (MX609P).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

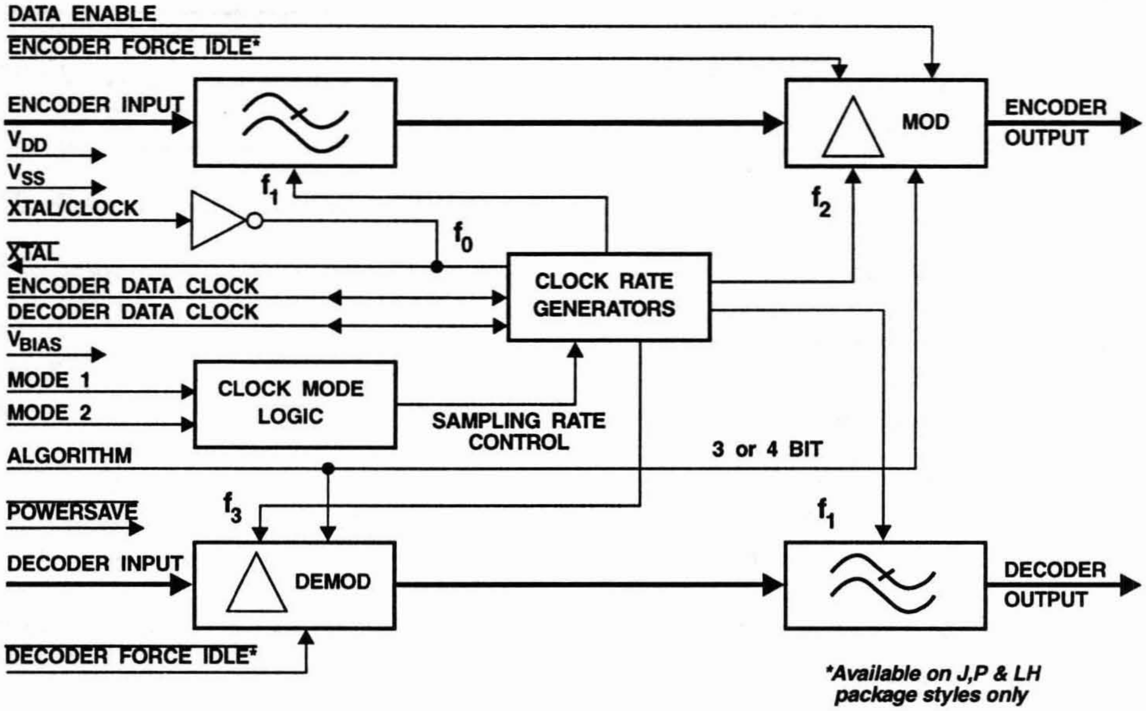
DATA ENABLE
ENCODER FORCE IDLE*
ENCODER INPUT
VDD
VSS
XTAL/CLOCK
XTAL
ENCODER DATA CLOCK
DECODER DATA CLOCK
VBIAS
MODE 1
MODE 2
ALGORITHM
POWERSAVE
DECODER INPUT
DECODER FORCE IDLE*
f1
f0
f2
f3
f1
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 or 4 BIT
MOD
DEMOD
ENCODER OUTPUT
DECODER OUTPUT
*Available on J,P & LH package styles only

Figure 1: Block Diagram

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2 Signal List

1	1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and figure 3.
	2		N/C		
2	3	2	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4		N/C		No Connection
4	5	3	Encoder Data Clock	input/ output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	4	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and $\overline{\text{Powersave}}$ inputs. See Table 2:
6	7	-	$\overline{\text{Encoder Force Idle}}$		When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1MΩ pullup.
7	8	5	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9		N/C		No Connection
9	10	6	Bias		Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V_{SS} when "$\overline{\text{Powersave}}$" is a logical "0".
10	11	7	Encoder Input	input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	8	V_{SS}	power	Negative Supply
12	13	-	N/C		No Connection
13	14	9	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15		N/C		No Connection
15	16	10	$\overline{\text{Powersave}}$		A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 MΩ pullup.
	17				No Connection
16	18	-	$\overline{\text{Decoder Force Idle}}$		A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical "1" the decoder operates as normal. Internal 1MΩ pullup.
17	19	11	Decoder Input		The received digital signal input. Internal 1 MΩ pullup.
18	20	12	Decoder Data Clock	input/ output	A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	13	Algorithm		A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

20	22	14	Clock Mode 2		Clock rates refer to f = 1024MHz Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1MΩ pullups.
21	23	15	Clock Mode 1		
22	24	16	V_{DD}	power	Positive Supply. A single 5.0V supply is required.

Table 1: Signal List

Data Enable	Powersave	Encoder Output
1	1	Enable
0	1	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kbps = f/16
1	0	Internal, 32kbps = f/32
1	1	Internal, 16kbps = f/64

Table 3: Clock Mode

3 External Components

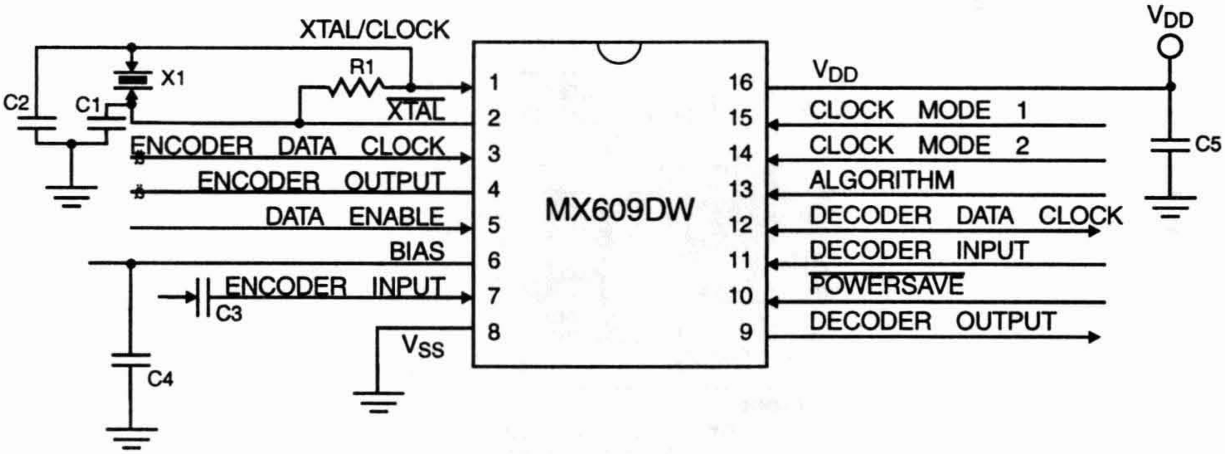

XTAL/CLOCK
X1
R1
C2
C1
XTAL
ENCODER DATA CLOCK
ENCODER OUTPUT
DATA ENABLE
BIAS
ENCODER INPUT
C3
C4
V_{SS}
1
2
3
4
5
6
7
8
MX609DW
16
15
14
13
12
11
10
9
V_{DD}
CLOCK MODE 1
CLOCK MODE 2
ALGORITHM
DECODER DATA CLOCK
DECODER INPUT
POWERSAVE
DECODER OUTPUT
V_{DD}
C5

Figure 2: Recommended External Components for Typical Application

R1	Note 1	1MΩ	±10%	C4	Note 4	1.0µF	±20%
C1	Note 2	33pF	±20%	C5	Note 5	1.0µF	±20%
C2	Note 2	68pF	±20%	X1	Note 6, 7	1.024MHz	
C3	Note 3	1.0µF	±20%				

Table 4: Recommended External Components for Typical Application

Notes:

1. Oscillator inverter bias resister
2. Xtal circuit load capacitor
3. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100W. Output idle channel noise levels will improve with even lower source impedance.
4. Bias decoupling capacitor
5. VDD decoupling capacitor
6. A 1.024MHz Xtal/Clock input will yield exactly 16/32/64kbps data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note.
7. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult you crystal manufacturer.

4 General Description

The MX609 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

Companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode when Powersave is selected.

5 Application

5.1 CODEC Integration

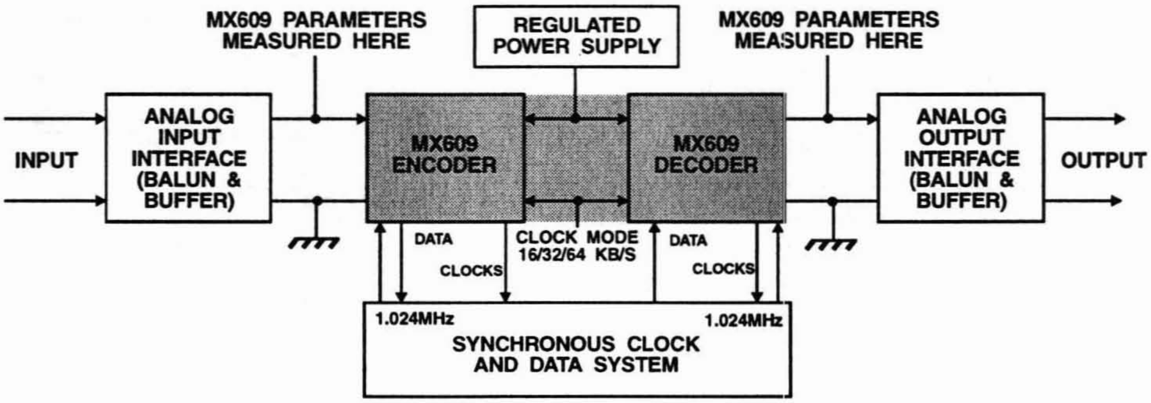

MX609 PARAMETERS MEASURED HERE
REGULATED POWER SUPPLY
MX609 PARAMETERS MEASURED HERE
INPUT
ANALOG INPUT INTERFACE (BALUN & BUFFER)
MX609 ENCODER
MX609 DECODER
ANALOG OUTPUT INTERFACE (BALUN & BUFFER)
OUTPUT
DATA
CLOCKS
CLOCK MODE 16/32/64 KB/S
DATA
CLOCKS
1.024MHz
1.024MHz
SYNCHRONOUS CLOCK AND DATA SYSTEM

Figure 3: System Configuration using the MX609

5.2 CODEC Performance

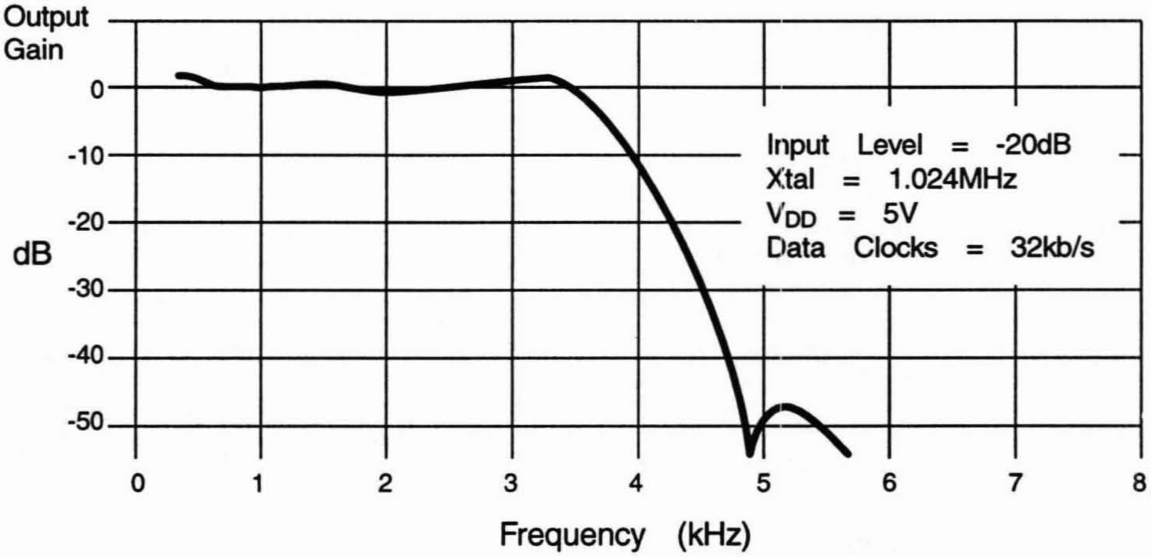


Figure 4: Typical CODEC Frequency Response

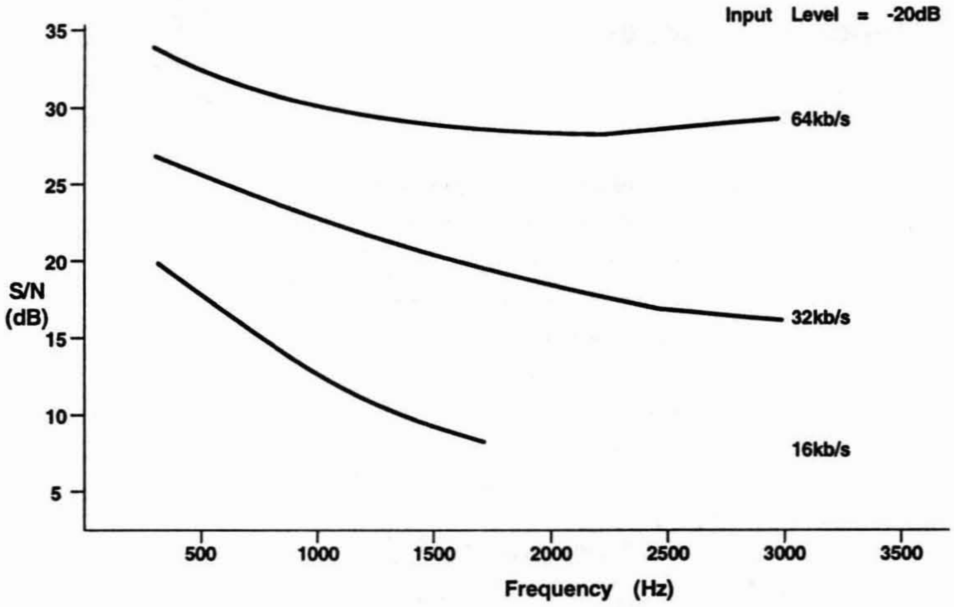


Figure 5: Typical S/N Ratio with Input Frequency

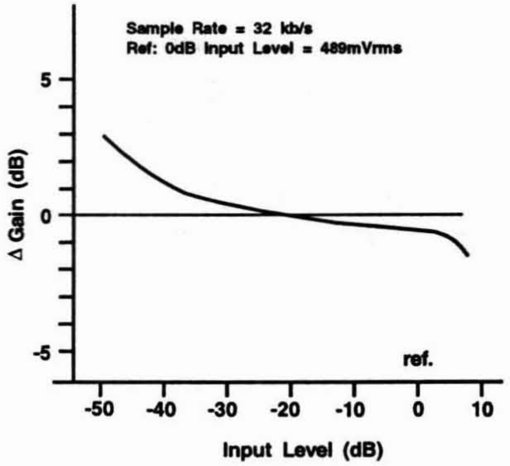


Figure 6: Typical Variation of Gain with Input Level

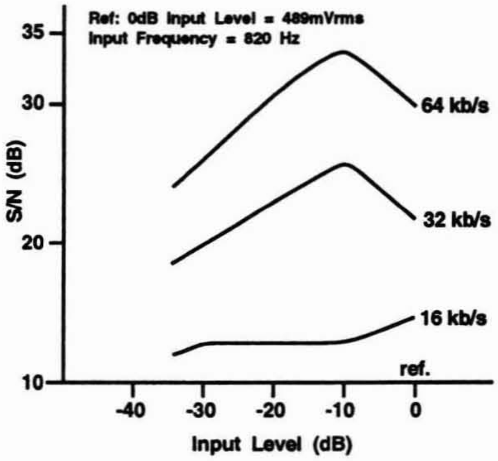


Figure 7: Typical S/N Ratio with Input Level

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
J / P / LH / DW Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C	-	800	mW
Derating above 25°C	-	10	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	4.5	5.0	5.5	V
Operating Temperature	-30		70	°C
Xtal Frequency	500	1.024	1500	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0V at T_{AMB} = 25°C, Audio Test Frequency = 820Hz Xtal/Clock f_0 = 1.024MHz
Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)			3.5		mA
Supply Current (Powersave)			500		µA
Input logic '1'		3.5			V
Input Logic '0'				1.5	V
Output Logic '1'		4.0			V
Output Logic '0'				1.0	V
Digital input Impedance					
Logic I/O pins			10		MΩ
Logic Input pins, Pullup Resistor	2	300			kΩ
Digital output impedance			4		kΩ
Analog Input Impedance			100		kΩ
Analog Output Impedance	6		800		Ω
Three State Output Leakage			±4		µA
Insertion Loss	2		0		dB
Dynamic Values	1				
Encoder					
Analog signal Input levels	6	-30		8	dB
Principal Integrator Frequency			275		Hz
Encoder passband			3400		Hz
Compand Time Constant			4		ms
Decoder					
Analog Signal Output Levels	6	-30	0	8	dB
Decoder Passband	3		3400		Hz
Encoder Decoder (Full Codec)					
Passband		300		3400	Hz
Stopband		6		10	KHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
Output Noise (Input Short Circuit)			-60		dB
Perfect Idle Channel Noise					
(Encode Forced)	7		-63		dB
Group Delay Distrotion	4				
(1000Hz-2600Hz)				450	µs
(600Hz-2800Hz)				750	µs
(500Hz-3000Hz)				1.5	µs
Xtal/clock Frequency		500	1024	1500	kHz

Notes:

1. Dynamic characteristics specified at 5.0V only.
2. All logic inputs except Encoder and Decoder Data clocks
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with and 820Hz, -20dB signal at the encoder input
5. Relative timings are shown in figure 4
6. Recommended values
7. Forced idle Encode/Decode not available on DW package.

6.1.4 TIMING

Serial Bus Timings (See Figure 8)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			µs
t_{CL}	Clock 0 pulse width	1.0			µs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU}+t_H$	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

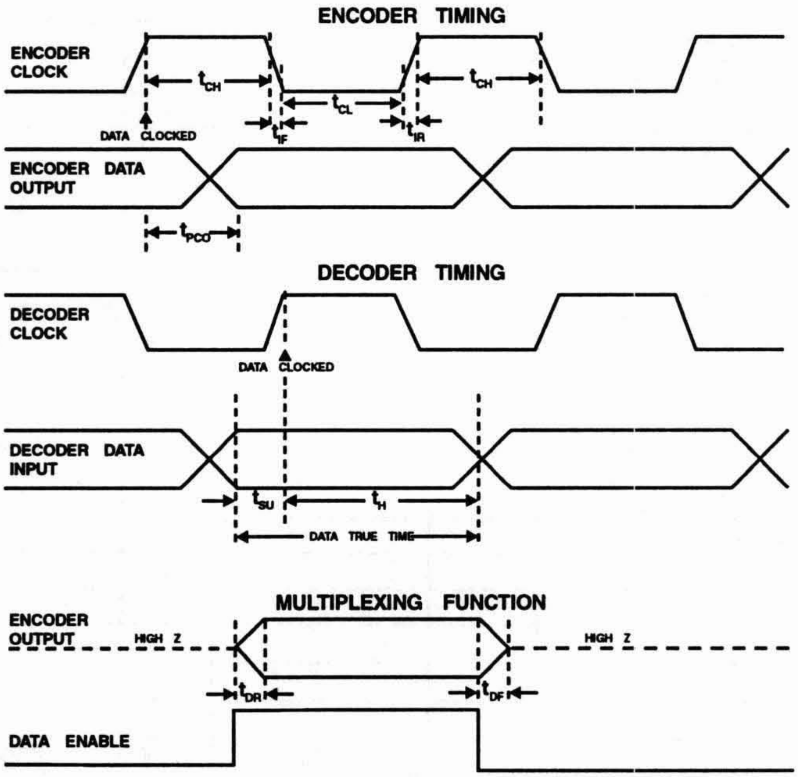
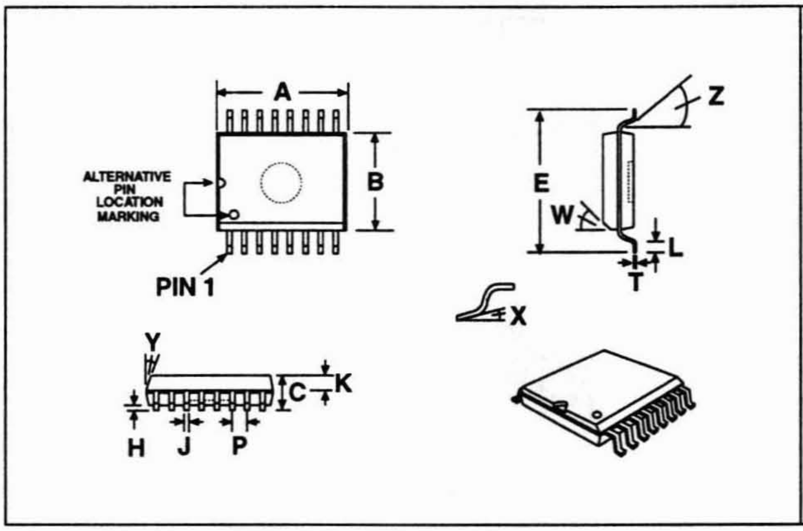

ENCODER TIMING
ENCODER CLOCK
t_{CH}
t_{CL}
t_{CH}
DATA CLOCKED
t_{IF}
t_{IR}
ENCODER DATA OUTPUT
t_{PCO}
DECODER TIMING
DECODER CLOCK
DATA CLOCKED
DECODER DATA INPUT
t_{SU}
t_H
DATA TRUE TIME
MULTIPLEXING FUNCTION
ENCODER OUTPUT
HIGH Z
HIGH Z
t_{DR}
t_{DF}
DATA ENABLE

Figure 8: Serial Bus Timing

6.2 Packaging

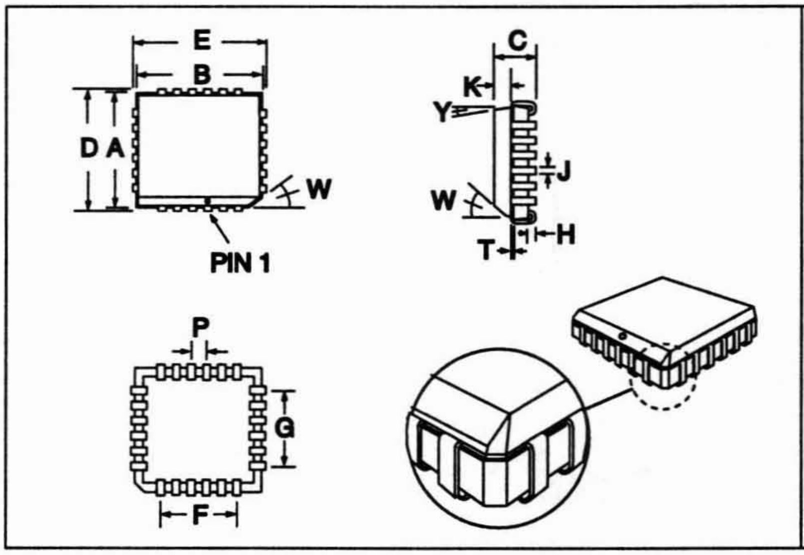


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin SOIC (DW) Mechanical Outline: *Order as part no. MX609DW*

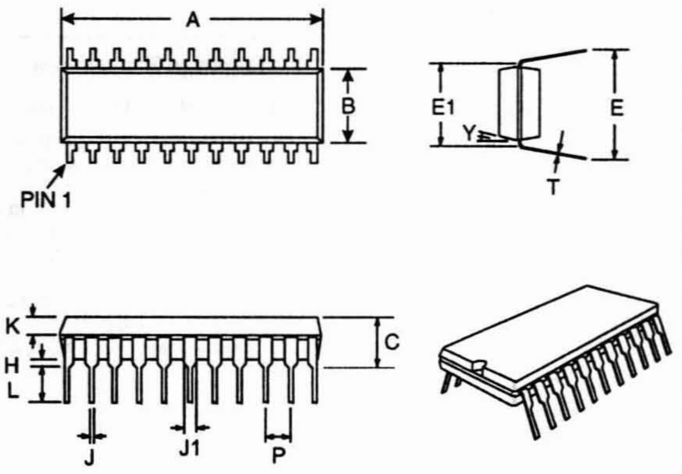


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin PLCC (LH) Mechanical Outline: *Order as part no. MX609LH*

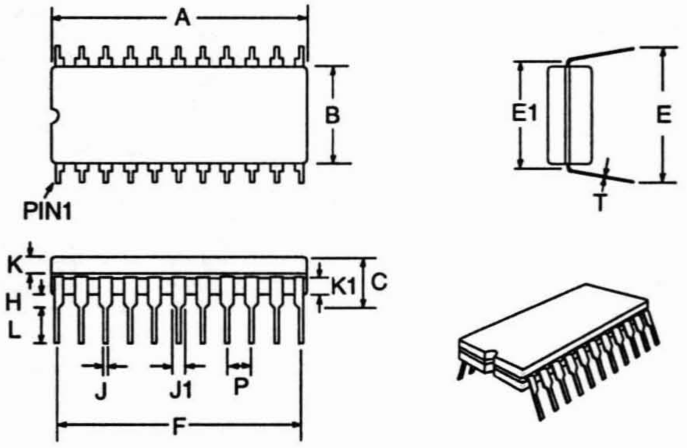


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 22-pin PDIP (P) Mechanical Outline: ***Order as part no. MX609P***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 22-pin CERDIP (J) Mechanical Outline: ***Order as part no. MX609J***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX614 Bell 202 Compatible Modem

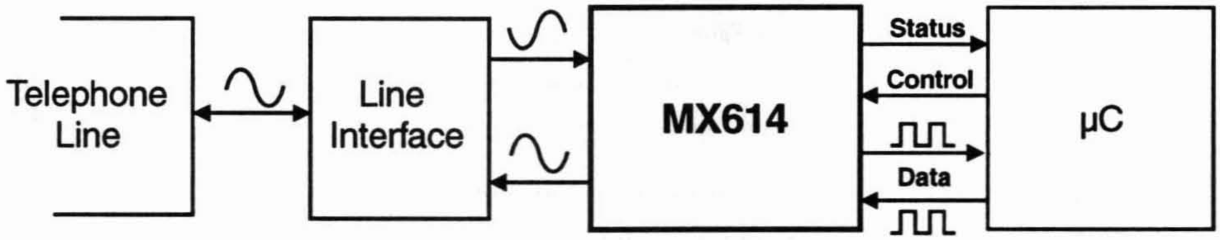
PRELIMINARY INFORMATION

Features

- **1200bps half duplex Bell 202 Compatible Modem**
- **Optional 1200bps Data Retiming Facility can eliminate external UART**
- **Optional 5bps and 150bps Back Channel**
- **Optional Line Equalization**

Applications

- **Low Voltage Operation (3.3V to 5.0V)**
- **Low Power Operation**
  - **1mA typ. @ 3.3V Operating Mode**
  - **1µA typ. Zero-Power Mode**
- **Standard 3.58MHz Xtal/Clock**
- **Telephone Telemetry Applications**



The MX614 is a low voltage, low power CMOS integrated circuit designed for the reception or transmission of asynchronous 1200bps data. This device is compatible with Bell 202 type systems. The MX614 supports 5bps and 150bps 'back channel' operation.

The MX614 provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for a UART in the associated µC when operating at 1200bps. An optional line equalizer has been incorporated into the receive path and is controlled by an external logic level.

The MX614 may be used in a wide range of telephone telemetry systems. A very low current "Zero Power Mode (1µA typ.) and an operating current of 1mA typ. @ V_{DD} = 3.3V, make the MX614 ideal for portable, terminal and line powered applications. A standard 3.58MHz Xtal/Clock is required and the device operates from a 3.0V to 5.5V supply.

The MX614 is available in 24-pin TSSOP (MX614TN), 16-pin SOIC (MX614DW) and 16-pin PDIP (MX614P) packages.

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2. Signal List .... 3 - 350

3. External Components .... 3 - 351

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- 4.1 Xtal Osc and Clock Dividers .... 3 - 352
- 4.2 Mode Control Logic .... 3 - 352
- 4.3 Rx Input Amplifier .... 3 - 352
- 4.4 Receive Filter and Equalizer .... 3 - 352
- 4.5 Energy Detector .... 3 - 353
- 4.6 FSK Demodulator .... 3 - 353
- 4.7 FSK Modulator and Transmit Filter .... 3 - 354
- 4.8 Rx Data Retiming .... 3 - 355
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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

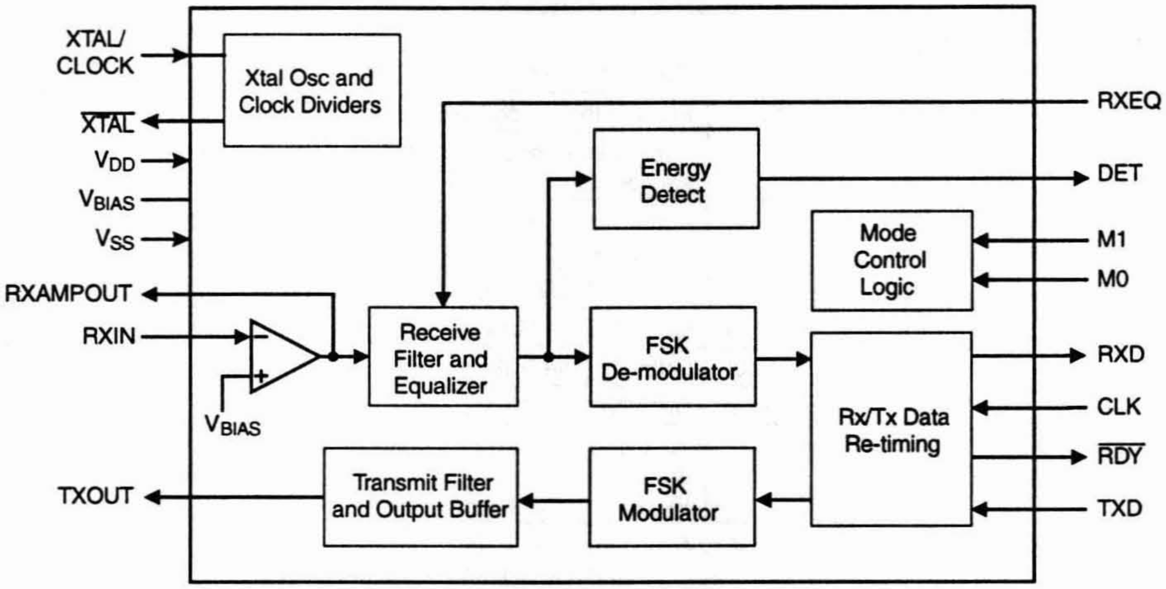
XTAL/
CLOCK
Xtal Osc and
Clock Dividers
XTAL
VDD
VBIAS
VSS
RXEQ
Energy
Detect
DET
Mode
Control
Logic
M1
M0
RXAMPOUT
RXIN
VBIAS
Receive
Filter and
Equalizer
FSK
De-modulator
Rx/Tx Data
Re-timing
RXD
CLK
RDY
TXD
TXOUT
Transmit Filter
and Output Buffer
FSK
Modulator

Figure 1: Block Diagram

2. Signal List

Pin No.		Signal		Description
P, DW	TN	Name	Type	
1	1	$\overline{\text{XTAL}}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	Power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in or out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip Energy Detect circuit.
15	23	$\overline{\text{RDY}}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	Power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10, 15, 16, 21, 22	N/C		No internal connection

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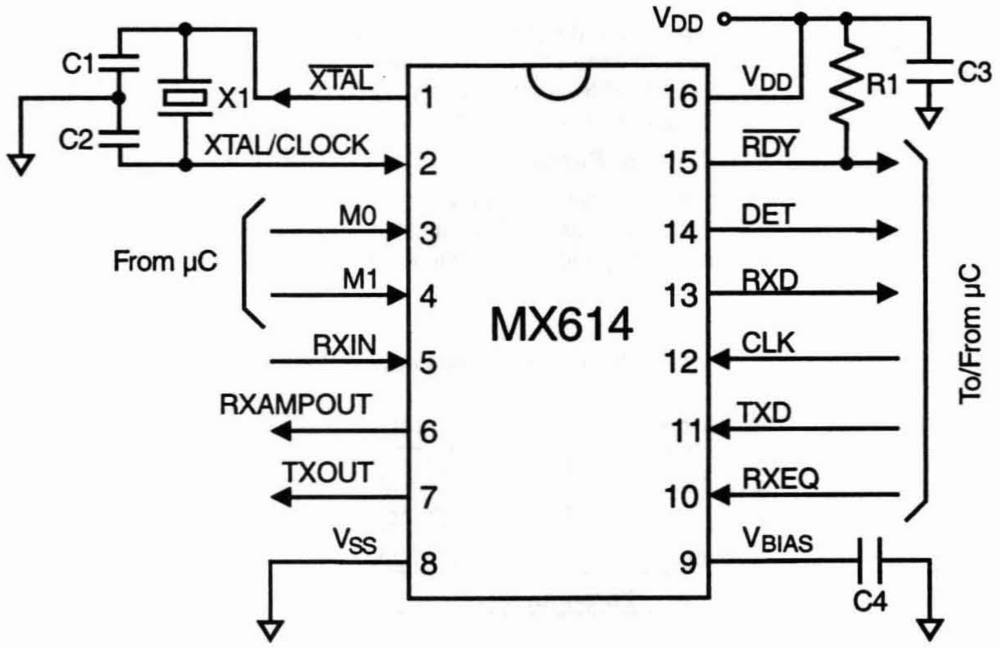
3. External Components


VDD
C1
C2
X1
XTAL
XTAL/CLOCK
From µC
M0
M1
RXIN
RXAMPOUT
TXOUT
VSS
MX614
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VDD
RDY
DET
RXD
CLK
TXD
RXEQ
VBIAS
R1
C3
C4
To/From µC

R1		100kΩ	±5%
C1 C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes

1. **IMPORTANT:** This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the decoupling capacitors be placed so that connections between them and the device pins are as short as practicable e.g. ≤ 1 inch from device pins. A ground plane protecting the receive path will help attenuate interfering signals
2. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX614 is determined by a 3.579545MHz clock signal present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX614 as well as generating undefined states of the RXD, DET and $\overline{\text{RDY}}$ outputs.

4.2 Mode Control Logic

The MX614's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	150bps	Rx
0	1	Off	1200bps	Tx
1	0	1200bps	Off / 5bps	Rx
1	1	'Zero-Power'		-

[1] If enabled

Note: On applying power to the device, the mode must be set to 'ZP', i.e. M0 = '1', M1 = '1', until V_{DD} has stabilized.

In the 'Zero-Power' (ZP) mode, power is removed from all internal circuitry. When leaving the 'ZP' mode there must be a delay of 20ms before any Tx data is passed to, or Rx data read from the device to allow the bias level, filters, and oscillator to stabilize.

4.3 Rx Input Amplifier

This amplifier is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer section is used to attenuate out of band noise and interfering signals, especially the locally generated transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low, the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

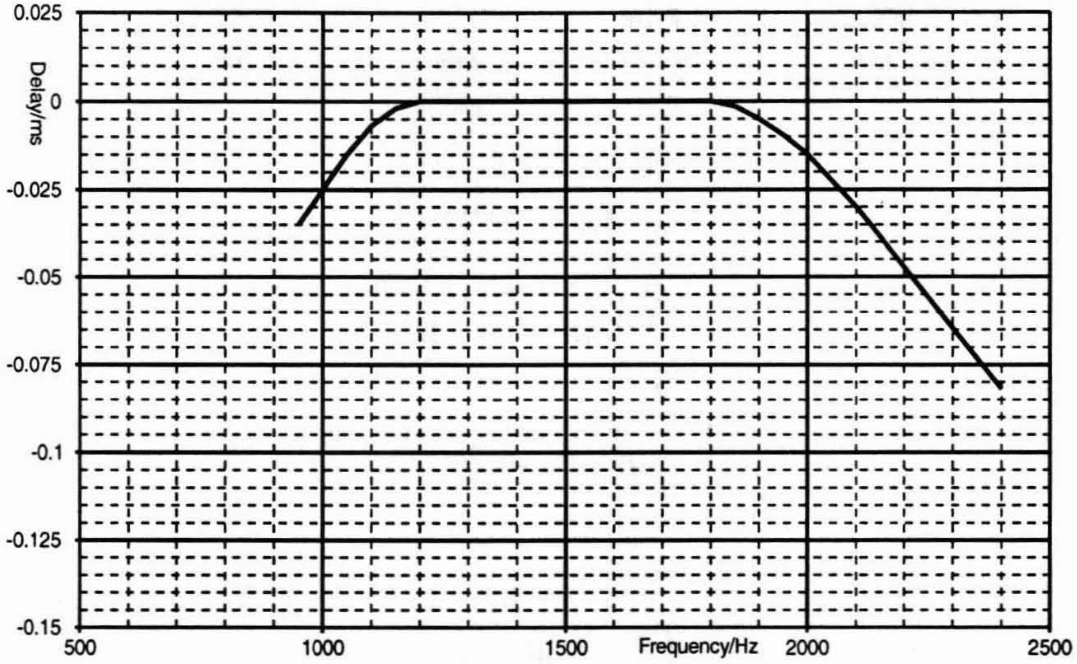


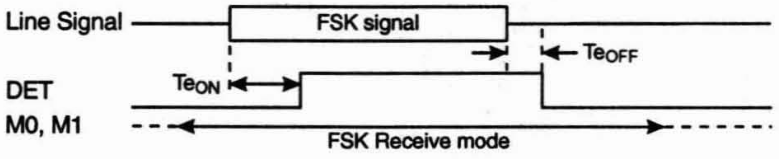
Figure 3: Rx Equalizer Group Delay (RXEQ = '1') wrt 1700Hz

4.5 Energy Detector

This block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient period of time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note that this circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

This block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'Off' or in 'ZP' the DET and RXD pins are held low.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin is read only when data is expected.

4.7 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	-
1	0	0Hz[1]	387Hz
0	0	487Hz	387Hz
0	1	2200Hz	1200Hz

Note: [1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

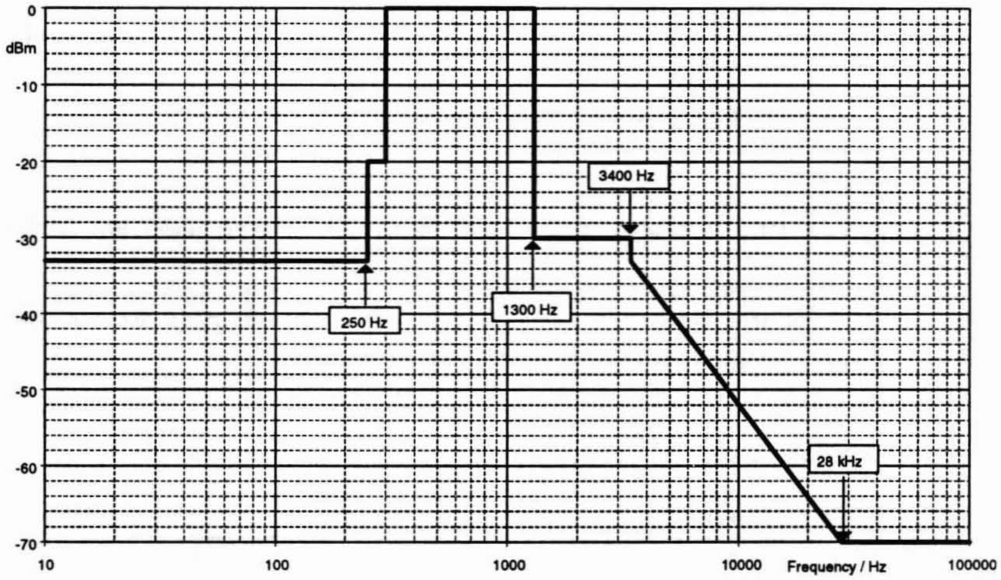


Figure 5: Tx limits at 5bps and 150bps rate

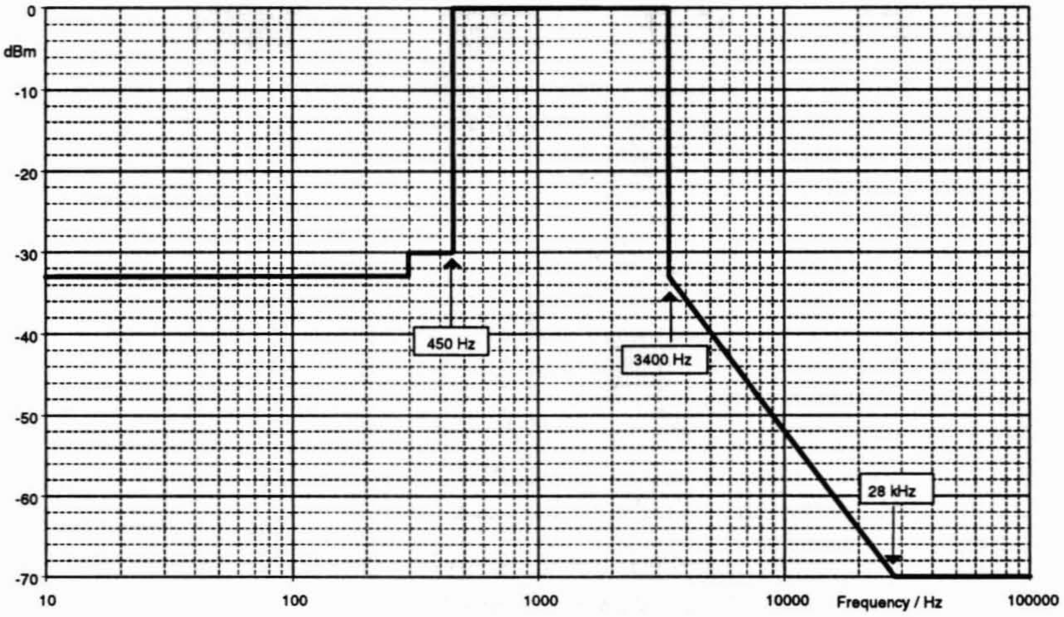


Figure 6: Tx limits at 1200bps rate

4.8 Rx Data Retiming

This function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

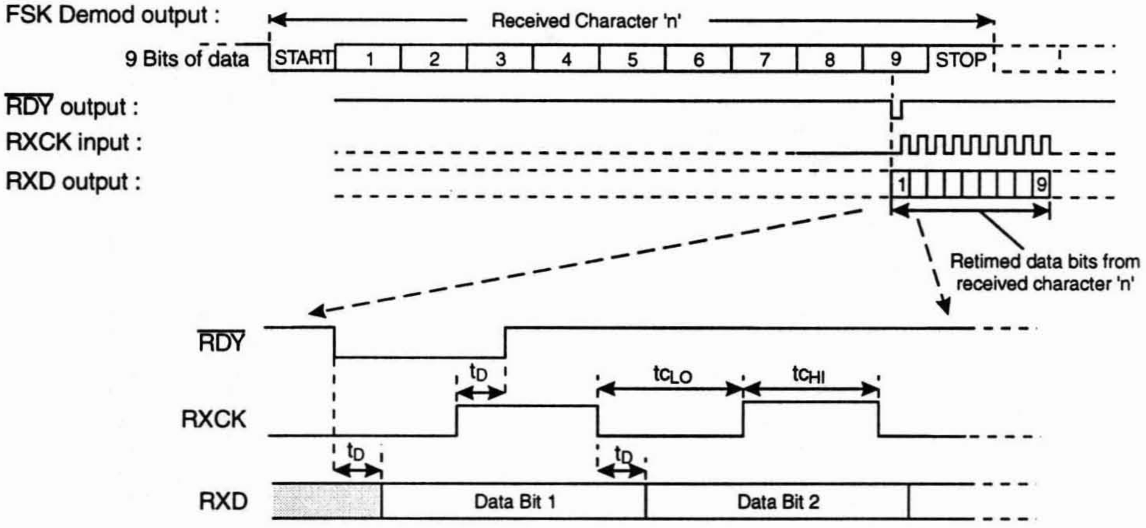
Data bits	Parity bits	Stop bits
7	0	≥ 2
7	1	≥ 1
8	0	≥ 1
8	1	≥ 1
9	0	≥ 1

The Data Retiming block, when enabled in receive mode, extracts the first 9 bits of each character following the start bit from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{\text{RDY}}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{\text{RDY}}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

So to use the Data Retiming function, the CLK input should be kept low until the $\overline{\text{RDY}}$ output goes low; if the Data Retiming function is not required the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the µC within the time of a complete character at 1200bps. See Section 6.2 for Timing specifications.


FSK Demod output :
Received Character 'n'
9 Bits of data
START
1
2
3
4
5
6
7
8
9
STOP
RDY output :
RXCK input :
RXD output :
1
9
Retimed data bits from received character 'n'
RDY
RXCK
RXD
tD
tCLO
tCHI
tD
tD
Data Bit 1
Data Bit 2

t_D = Internal MX614 delay, t_{CHI} = CLK high time, t_{CLO} = CLK low time

Figure 7: FSK Operation with Rx Data Retiming

Note that, if enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the RDY output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8.

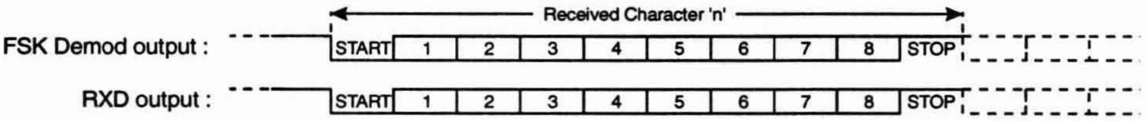

Received Character 'n'
FSK Demod output :
START
1
2
3
4
5
6
7
8
STOP
RXD output :
START
1
2
3
4
5
6
7
8
STOP

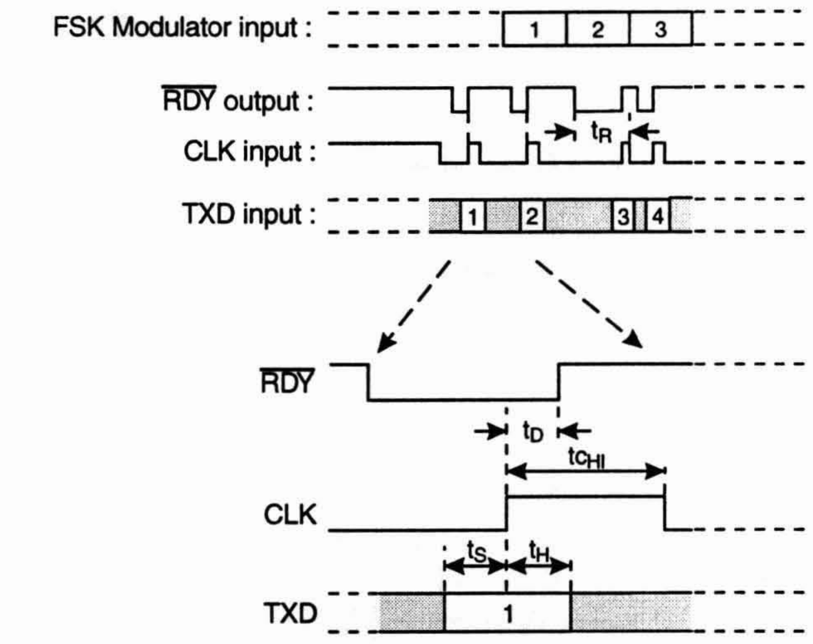
Figure 8: FSK Operation without Rx Data Retiming (CLK always high)

4.9 Tx Data Retiming

The Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling µC to load one bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the RDY pin is pulled low. The RDY output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the RDY output is pulled low. When the RDY pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 9. See Section 6.2 for Timing specifications.


FSK Modulator input :
1
2
3
RDY output :
CLK input :
t_R
TXD input :
1
2
3
4
RDY
t_D
tc_{HI}
CLK
t_S
t_H
TXD
1

t_D = Internal MX614 delay, t_R = $\overline{\text{RDY}}$ low to CLK going low, t_S = data set up time

tc_{HI} = CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

To ensure synchronization between the controlling device and the MX614 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 5bps or 150bps data which has no retime option.

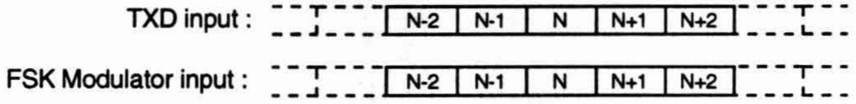

TXD input :
N-2
N-1
N
N+1
N+2
FSK Modulator input :
N-2
N-1
N
N+1
N+2

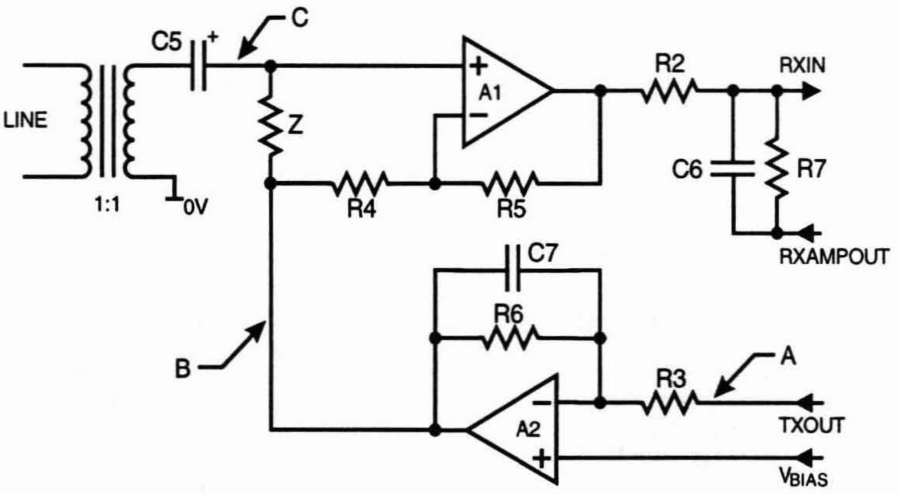
Figure 10: FSK Operation without Tx Data Retiming (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX614. A Line Interface circuit is required to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes		±1%,
R3	See Notes		±1%,
R4-R7		100kΩ	±1%,
C5		22µF	±20%
C6		100pF	±10%
C7		330pF	±10%

Figure 11: Line Interface Circuit

Line Interface Notes:

1. The components 'Z' between points B and C should match the line impedance.
2. Device A2 must be able to drive 'Z' and the line.
3. R2: For optimum results R2 should be set so that the gain is $V_{DD}/5.0$, i.e. R2 = 100kΩ at $V_{DD} = 5.0V$, rising to 150kΩ at $V_{DD} = 3.3V$.
4. R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

Level at 'A' = $20\mathrm{Log}(V_{DD}/5)$
" 'B' = 'A' + 20Log(100kΩ/R3)
" 'C' = 'B' - 6

Example:

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of and pins			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C
Xtal Frequency = 3.579545MHz ± 0.1% 0dBV corresponds to 1.0V_{RMS}
0dBm corresponds to 775mV_{RMS} into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0 = '1', M1 = '1')	1, 2		1.0		µA
I_{DD} (M0 or M1 = '0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1 = '0') at V_{DD} = 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD} -0.4			V
Output Logic '0' Level (I_{OL} = 360µA)				0.4	V
$\overline{RDY}$ Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Demodulator					
Bit Rate		0	1200	1212	Baud
Mark (Logical '1') Frequency		1188	1200	1212	Hz
Space (Logical '0') Frequency		2178	2200	2222	Hz
Valid Input Level Range	3	-40.0		-8.0	dBV
Maximum Twist (Mark Level wrt Space Level)		±6.0			dB
Acceptable Signal to Noise Ratio	4	20.0			dB
Level Detector 'On' Threshold Level	3			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level Driving ≥ 40kΩ load	5	-1.0	0	1.0	dB
Twist (Mark Level wrt Space Level)		-2.0	0	2.0	dB
Tx 1200bps (M1 = '0', M0 = '1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical '1') Frequency		1197		1203	Hz
Space (Logical '0') Frequency		2196		2204	Hz
Tx 150bps (M1 = '0', M0 = '0').					
Bit Rate		0	150	152	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency		485		489	Hz
Tx 5bps (M1 = '1', M0 = '0').					
Bit Rate		0	5.0	5.1	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency	6		0		Hz

	Notes	Min.	Typ.	Max.	Units
Input Amplifier					
Impedance (RXIN Pin)	7	10.0			MΩ
Voltage Gain	7		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	8	100			ns
'Low' Pulse Width	8	100			ns

Operating Characteristics Notes:

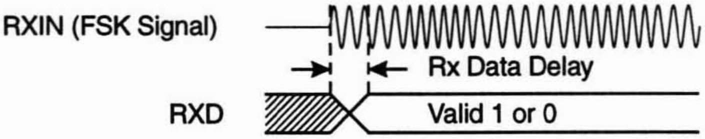
1. Not including any current drawn from the MX614 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1200Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1
4. Flat noise in 200 - 3200Hz band.
5. Relative to 775mV_{RMS} at V_{DD}= 5.0V for load resistance greater than 40kΩ.
6. TXOUT held at approximately V_{DD}/2.
7. Open loop, small signal low frequency measurements.
8. Timing for an external input to the XTAL/CLOCK pin.

6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX614 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

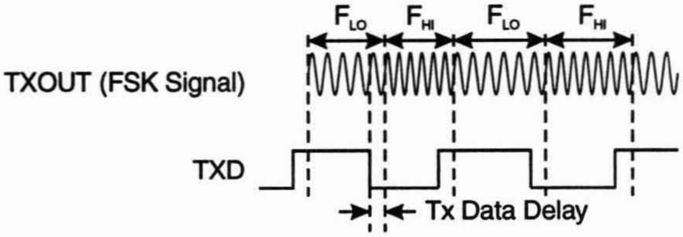
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

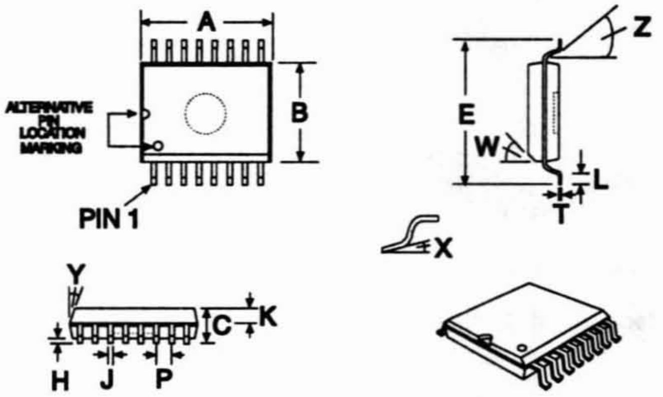
Figure 12: RXIN to RXD Delay time



Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

6.3 Packaging

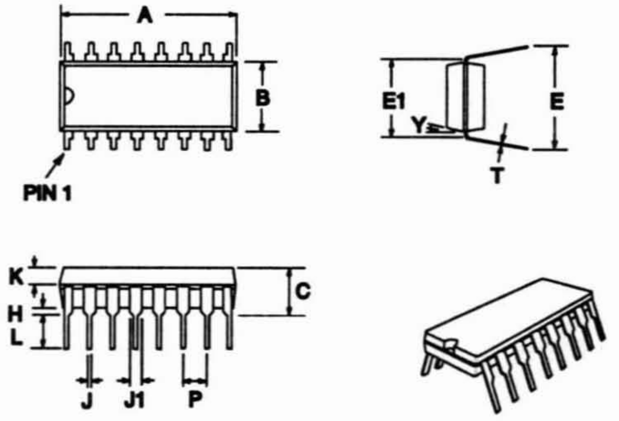


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX614DW*

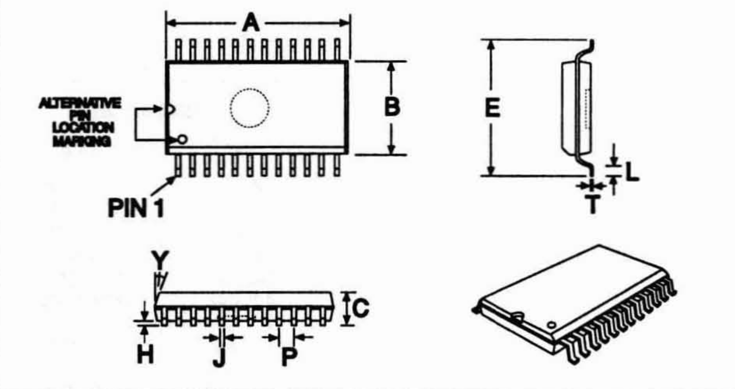


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX614P*


A
ALTERNATIVE PIN LOCATION MARKING
B
E
L
T
PIN 1
Y
C
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16 : 24-pin TSSOP Mechanical Outline: ***Order as part no. MX614TN***

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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX619

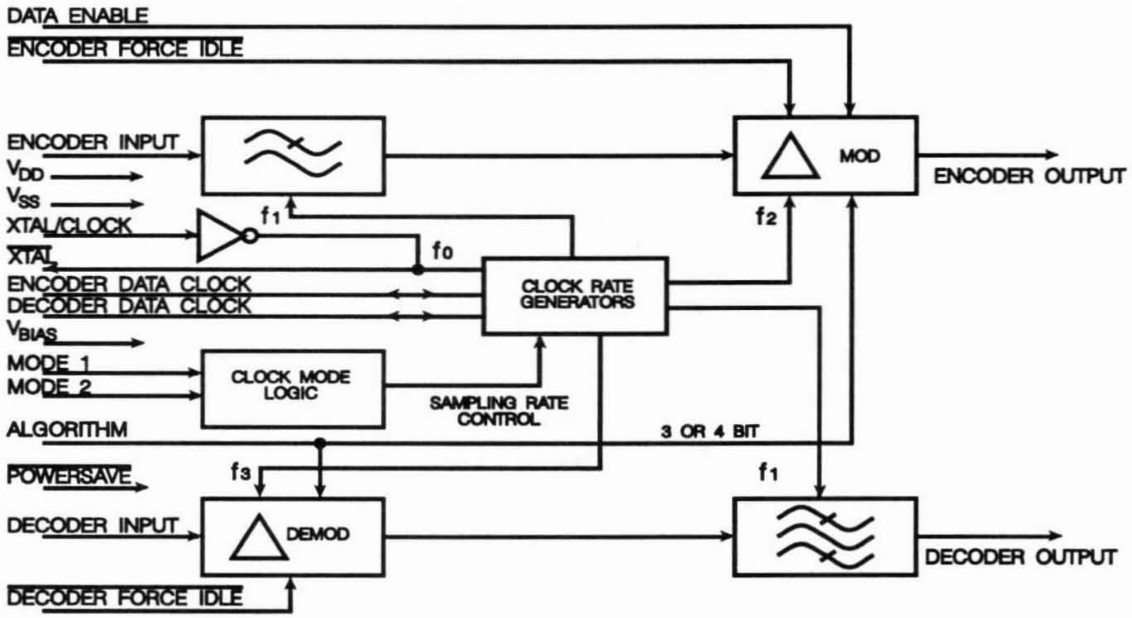
DELTA MODULATION CODEC meets EUROCOM D1-IA8

Features

- Meets EUROCOM D1-IA8
- Single Chip Full Duplex CVSD CODEC
- On-chip Input and Output Filters
- Programmable Sampling Clocks
- 3- or 4-bit Companding Algorithm
- Powersave Capabilities
- Low Power, 5.0V Operation

Applications

- Military Communications
- Multiplexers, Switches, & Phones



DATA ENABLE
ENCODER FORCE IDLE
ENCODER INPUT
V_{DD}
V_{SS}
XTAL/CLOCK
XTAL
ENCODER DATA CLOCK
DECODER DATA CLOCK
V_{BIAS}
MODE 1
MODE 2
ALGORITHM
POWERSAVE
DECODER INPUT
DECODER FORCE IDLE
f_1
f_0
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 OR 4 BIT
f_3
DEMOD
MOD
f_2
ENCODER OUTPUT
f_1
DECODER OUTPUT

The MX619 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches, and phones. The MX619 is designed to meet EUROCOM D1-IA8 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010...pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

The MX619 operates with a supply voltage of 5.0V and is available in the following packages: 24-pin PLCC (MX619LH), 22-pin CERDIP (MX619J), and 22-pin PDIP (MX619P).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

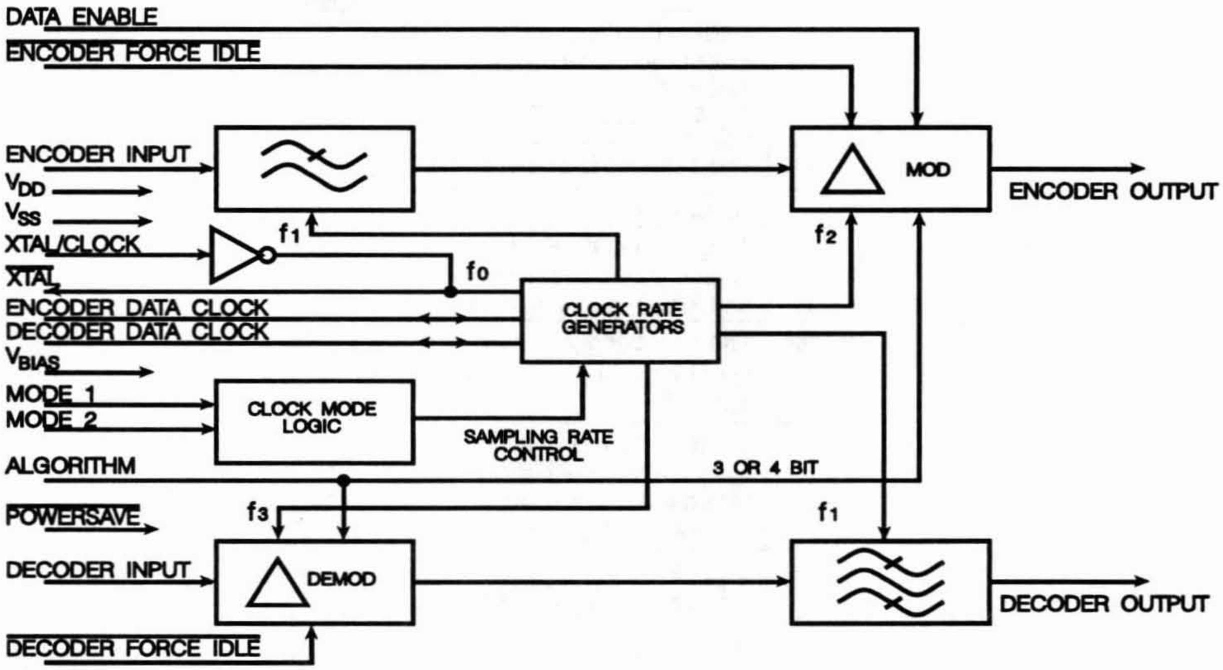

DATA ENABLE
ENCODER FORCE IDLE
ENCODER INPUT
V_{DD}
V_{SS}
XTAL/CLOCK
XTAL
ENCODER DATA CLOCK
DECODER DATA CLOCK
V_{BIAS}
MODE 1
MODE 2
ALGORITHM
POWERSAVE
DECODER INPUT
DECODER FORCE IDLE
f1
f0
f2
f3
f1
MOD
ENCODER OUTPUT
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 OR 4 BIT
DEMOD
DECODER OUTPUT

Figure 1: Block Diagram

2 Signal List

J/P	LH	Name	Signal	Description
1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 2.
	2	N/C		No Connection
2	3	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4	N/C		No Connection
4	5	Encoder Data Clock	input/ output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and $\overline{\text{Powersave}}$ inputs. See Table 2.
6	7	$\overline{\text{Encoder Force Idle}}$		When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1MΩ pullup.
7	8	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9	N/C		No Connection
9	10	V_{BIAS}		Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V_{SS} when "$\overline{\text{Powersave}}$" is a logical "0".
10	11	Encoder Input	input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 2.
11	12	V_{SS}	power	Negative Supply
12	13	N/C		No Connection
13	14	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15	N/C		No Connection
15	16	$\overline{\text{Powersave}}$		A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 MΩ pullup.
	17	N/C		No Connection
16	18	$\overline{\text{Decoder Force Idle}}$		A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical "1" the decoder operates as normal. Internal 1MΩ pullup.
17	19	Decoder Input		The received digital signal input. Internal 1 MΩ pullup.
18	20	Decoder Data Clock	input/ output	A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm		A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

J/P	LH	Name	Signal	Description
20	22	Clock Mode 2		Clock rates refer to f = 1024MHz Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1MΩ pullups. See Table 3.
21	23	Clock Mode 1		
22	24	V_{DD}	power	Positive Supply. A single 5.0V supply is required.

Table 1: Signal List

Data Enable	Powersave	Encoder Output
1	1	Enable
0	1	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kbps = f/16
1	0	Internal, 32kbps = f/32
1	1	Internal, 16kbps = f/64

Table 3: Clock Mode

3 External Components

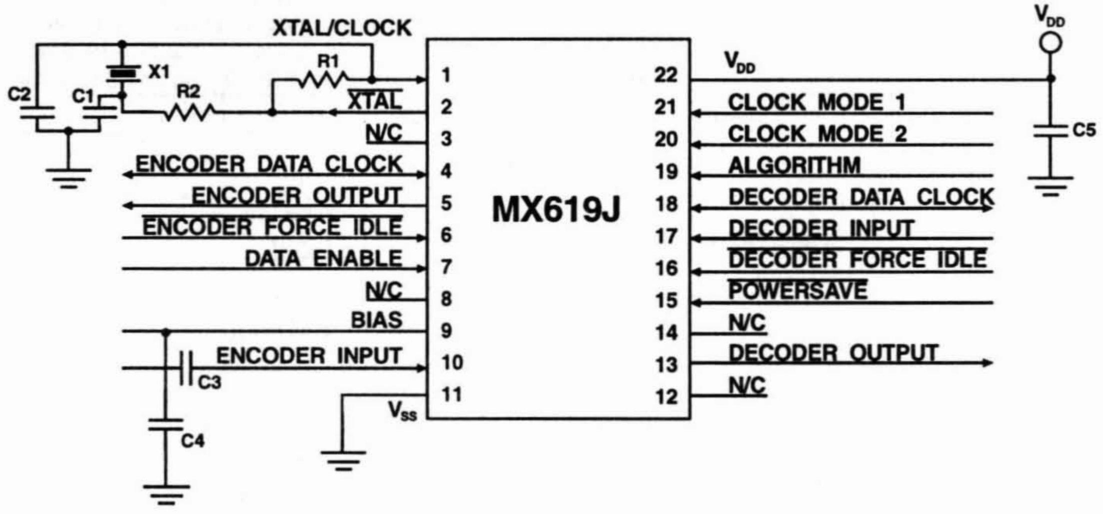

XTAL/CLOCK
X1
R1
R2
C1
C2
XTAL
N/C
ENCODER DATA CLOCK
ENCODER OUTPUT
ENCODER FORCE IDLE
DATA ENABLE
N/C
BIAS
ENCODER INPUT
C3
C4
V_{SS}
1
2
3
4
5
6
7
8
9
10
11
MX619J
22
21
20
19
18
17
16
15
14
13
12
V_{DD}
CLOCK MODE 1
CLOCK MODE 2
ALGORITHM
DECODER DATA CLOCK
DECODER INPUT
DECODER FORCE IDLE
POWERSAVE
N/C
DECODER OUTPUT
N/C
V_{DD}
C5

Figure 2: Recommended External Components for Typical Application

R1	Note 1	1MΩ	±10%
R2	Note 2	Selectable	
C1	Note 3	33pF	±20%
C2	Note 3	68pF	±20%

C3	Note 4	1.0µF	±20%
C4	Note 5	1.0µF	±20%
C5	Note 6	1.0µF	±20%
X1	Note 7, 8	1.024MHz	

Table 4: Recommended External Components for Typical Application

Notes:

1. Oscillator inverter bias resister.
2. Xtal Drive limiting resistor.
3. Xtal circuit load capacitor.
4. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with even lower source impedance.
5. Bias decoupling capacitor
6. V_{DD} decoupling capacitor
7. A 1.024MHz Xtal/Clock input will yield exactly 16/32/64kbps data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note.
8. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult you crystal manufacturer.

4 General Description

The MX619 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches and phones. The MX619 is designed to meet EUROCOM D1-IA8 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010...pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

5 Application

Due to the very low levels of a signal idle channel noise specified for military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

1. Care should be taken in the design and layout of the printed circuit board.
2. All external components (as recommended in Figure 2) should be kept close to the package.
3. Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.
4. Xtal/Clock tracks should be kept well away from analog inputs and outputs.
5. Inputs and outputs should be screened whenever possible.
6. A 'ground plane' connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.
7. It is recommended that the power supply rails have less that 1mV$_{RMS}$ of noise allowed.
8. The source impedance to the Encoder Input pin must be less that 100W; output idle channel, noise levels will improve with even power source impedances.

5.1 CODEC Integration

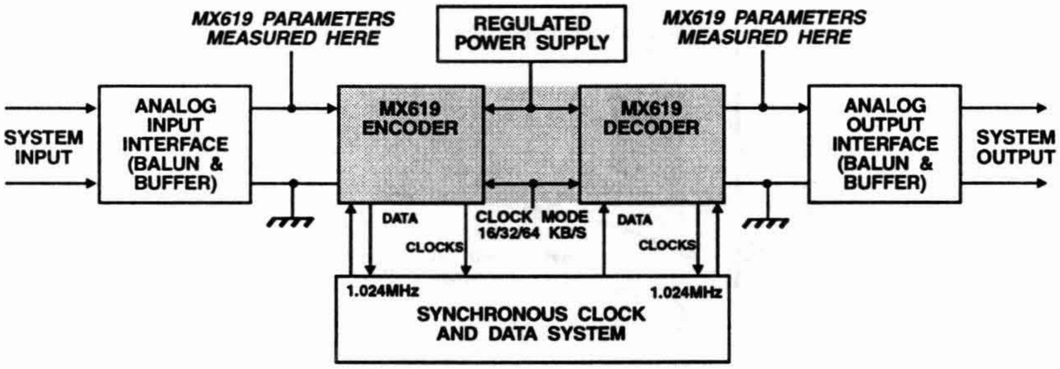

MX619 PARAMETERS MEASURED HERE
REGULATED POWER SUPPLY
MX619 PARAMETERS MEASURED HERE
SYSTEM INPUT
ANALOG INPUT INTERFACE (BALUN & BUFFER)
MX619 ENCODER
MX619 DECODER
ANALOG OUTPUT INTERFACE (BALUN & BUFFER)
SYSTEM OUTPUT
DATA
CLOCKS
CLOCK MODE 16/32/64 KB/S
DATA
CLOCKS
1.024MHz
1.024MHz
SYNCHRONOUS CLOCK AND DATA SYSTEM

Figure 3: System Configuration using the MX619

5.2 Digital to Analog Performance

Test	Sample Rate	Bit Sequence at Decoder Input	MLA Duty Cycle	Typical Output Level
a	16kbps 32kbps	1011010010010010110 1 1011011010101001001001001001010101101101	0 0	-41.5dBmO –42.5dBmO
b	16kbps 32kbps	1101100100100100110 1 1011011010101001001000100100101011011011	0.05 0.05	-25.0dBmO –25.0dBmO
c	16kbps 32kbps	10110101000100101011 1101101101010010001000100100101011011101	0.1 0.1	-19.0dBmO -18.5dBmO
d	16kbps 32kbps	11011001000010011011 1101110110010100010000100010011010111011	0.2 0.2	-11.0dBmO –11.5dBmO
e	16kbps 32kbps	11011010000010010111 111011101100100010000001001001101110111	0.3 0.3	-6.5dBmO –6.5dBmO
f	16kbps 32kbps	11011010000001001111 1111011101010001000000001000101011101111	0.4 0.4	-3.0dBmO –3.0dBmO
g	16kbps 32kbps	1110101000000001011 1111101110100010000000000100010111011111	0.5 0.5	0dBmO 0dBmO

Table 5: Bit Sequence Test

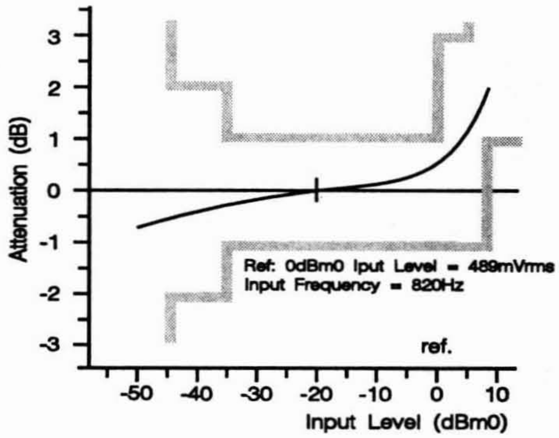


Figure 4: Gain vs. Input Level (16kbps)

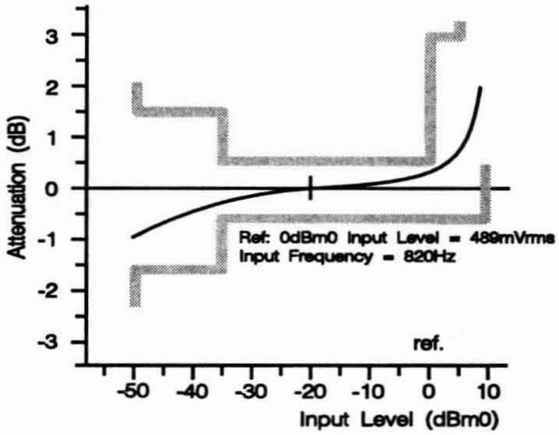


Figure 5: Gain vs. Input Level (32kbps)

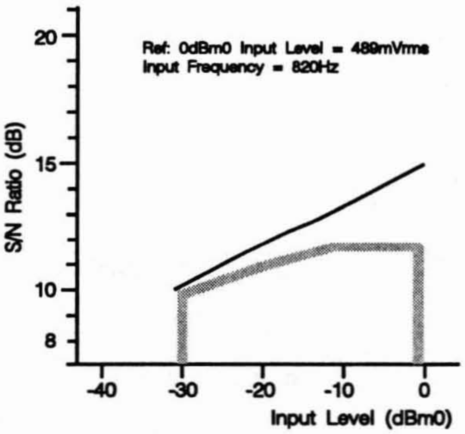


Figure 6: S/N vs. Input Level (16kbps)

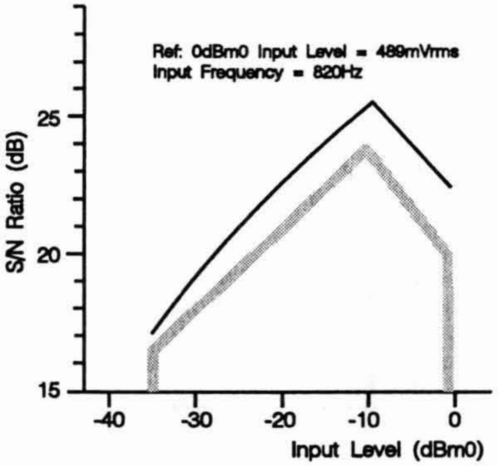


Figure 7: S/N vs. Input Level (32kbps)

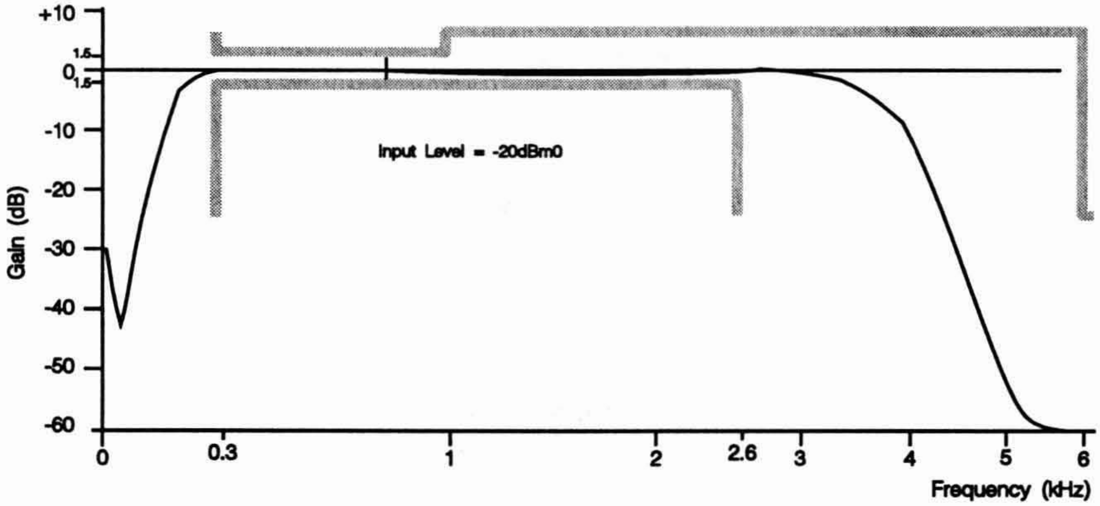


Figure 8: Attenuation distrotion vs. Frequency (16kbps)

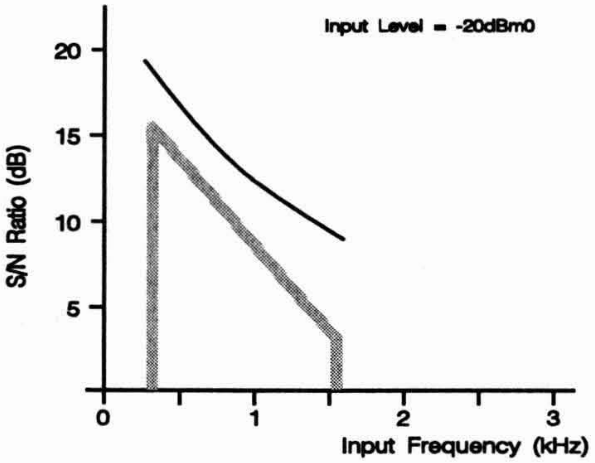


Figure 9: S/N vs. Input Frequency (16kbps)

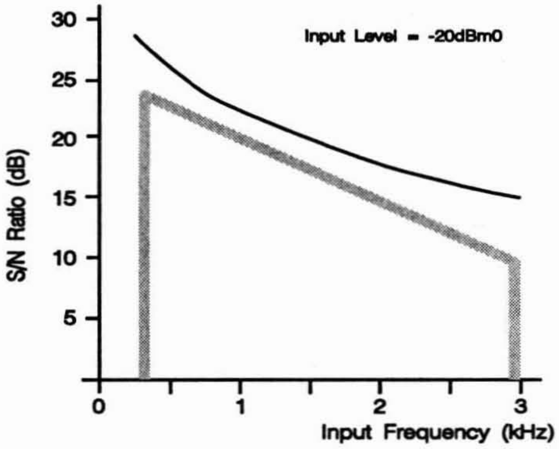


Figure 10: S/N vs. Input Frequency (32kbps)

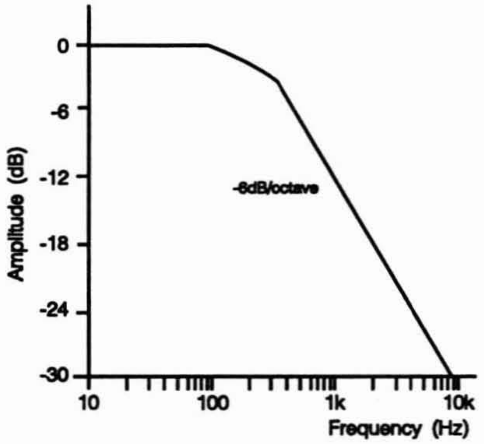


Figure 11: Principal Integrator Response

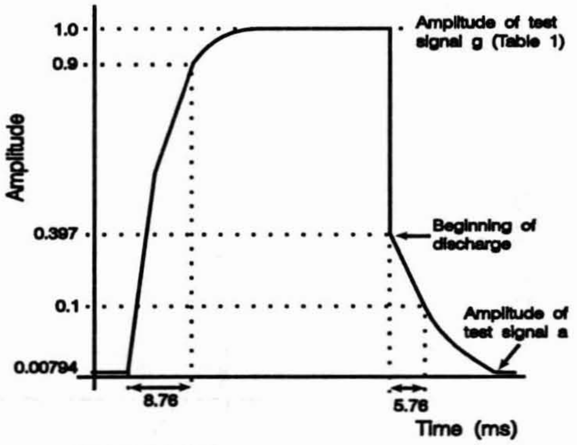


Figure 12: Compand Envelope

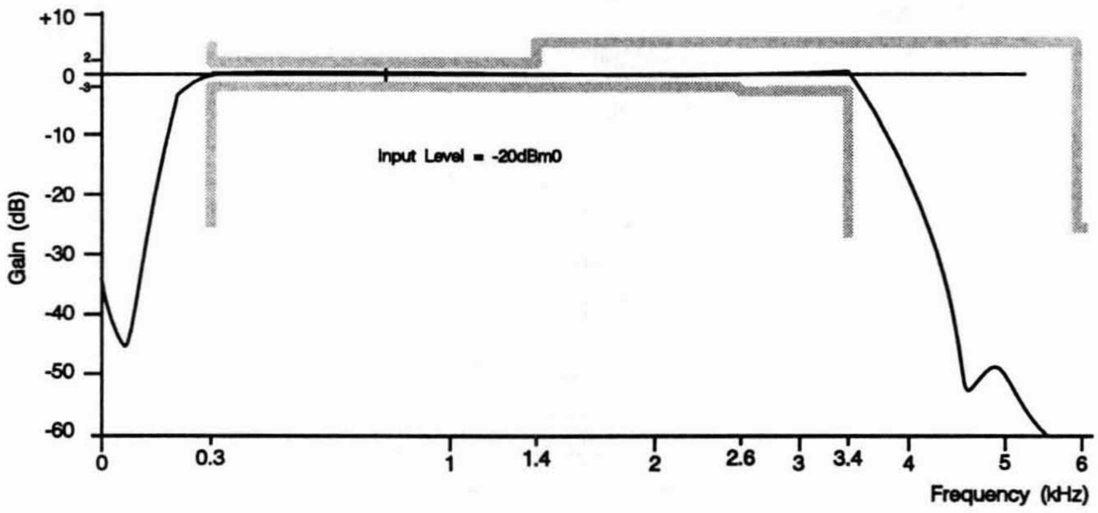


Figure 13: Attenuation Distortion vs. Frequency (32kbps)

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
J / P / LH Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C	-	800	mW
Derating above 25°C	-	10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	4.5	5.0	5.5	V
Operating Temperature	-40		85	°C
Xtal Frequency	500	1.024	1500	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0V at T_{AMB} = 25°C, Audio Test Frequency = 820Hz Xtal/Clock f_0 = 1.024MHz
3-bit Compand Algorithm, Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)			5.5		mA
Supply Current (Powersave)			400		µA
Input logic '1'	8	3.5			V
Input Logic '0'	8			1.5	V
Output Logic '1'		4.0			V
Output Logic '0'				1.0	V
Digital Input Impedance					
Logic I/O pins		1.0	10		MΩ
Logic Input pins, Pullup Resistor	2	300			kΩ
Digital output impedance			4		kΩ
Analog Input Impedance	4		1		kΩ
Analog Output Impedance	7			800	Ω
Three State Output Leakage		-4		4	µA
Insertion Loss	3	-2		2	dB
Dynamic Values	1,9				
Encoder					
Analog signal Input levels	5, 9	-35		6	dBmO
Principal Integrator Frequency			275		Hz
Encoder Passband			3400		Hz
Compand Time Constant			4.0		ms
Decoder					
Analog Signal Output Levels	5, 9	-35	-10	6	dBmO
Decoder Passband		300		3400	Hz
Encoder Decoder (Full Codec)					
Compression Ration (Cd = 0.5 to Cd = 0.0)		50			
Passband		300		3400	Hz
Stopband		6		10	KHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
300Hz – 1400Hz		-1		1	dB
1400Hz – 2600Hz		-1		1	dB
2600Hz –3400Hz		-2		3	dB
Output Noise (Input Short Circuit)	9			-60	dBmO
Perfect Idle Channel Noise					
(Encode Forced)	9		-63		dBmO

	Notes	Min.	Typ.	Max.	Units
Group Delay Distrotion	4				
(1000Hz-2600Hz)	6			450	µs
(600Hz-2800Hz)	6			750	µs
(500Hz-3000Hz)	6			1.5	ms
Xtal/clock Frequency			1024		kHz

Notes:

1. Dynamic characteristics are specified at 5.0V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data clocks
3. For and encoder/Decoder combination, Insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 4, 5, 6, and 7.
6. Group Delay Distortion for the full codec is relative to the delay with and 820Hz, -20dB signal at the encoder input
7. An Emitter Follower output stage.
8. 4V = 80%V_{DD}, 3.5V = 70%V_{DD}, 1.5V = 30%V_{DD}, 1V = 20%V_{DD}
9. Analog Voltage Levels used: 0dBmO = 489mV_{RMS} = -4dBm = 0dB. –15dBmO = 87mV_{RMS}. –20dBmO = 49mV_{RMS} = -24dBm.

6.1.4 TIMING

Serial Bus Timings (See Figure 14)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			µs
t_{CL}	Clock 0 pulse width	1.0			µs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU} + t_H$	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

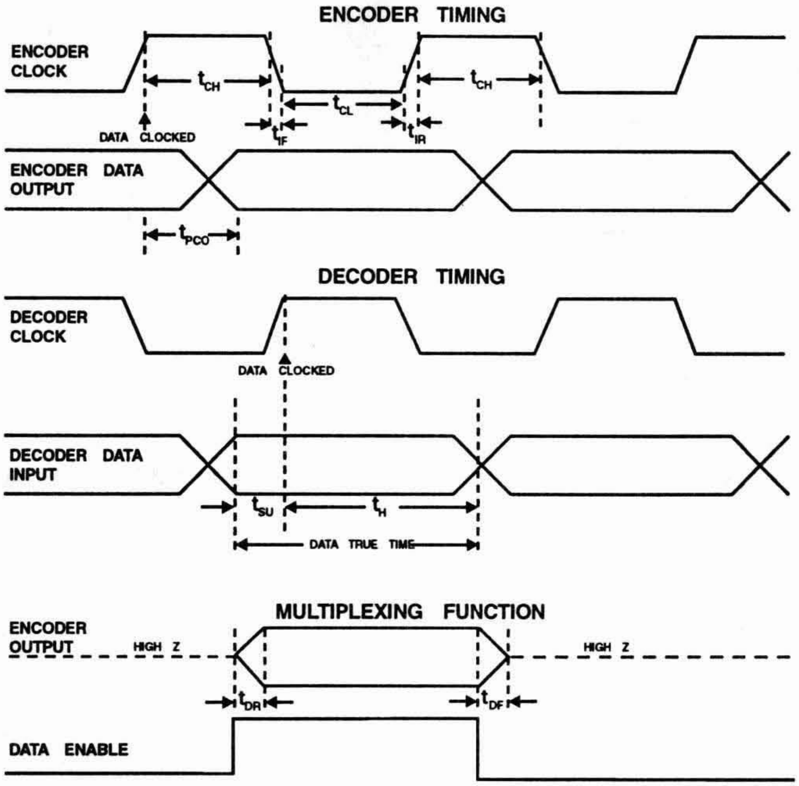
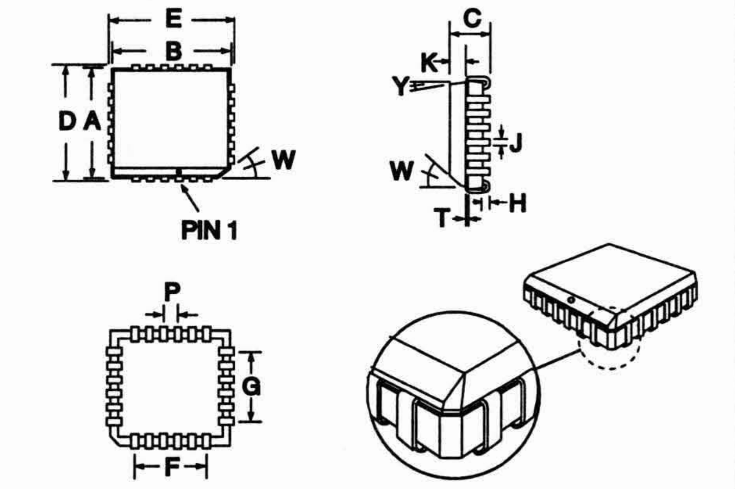

ENCODER TIMING
ENCODER CLOCK
t_{CH}
t_{CL}
t_{IF}
t_{IR}
DATA CLOCKED
ENCODER DATA OUTPUT
t_{PCO}
DECODER TIMING
DECODER CLOCK
DATA CLOCKED
DECODER DATA INPUT
t_{SU}
t_{H}
DATA TRUE TIME
MULTIPLEXING FUNCTION
ENCODER OUTPUT
HIGH Z
HIGH Z
t_{DR}
t_{DF}
DATA ENABLE

Figure 14: CODEC Timing

6.2 Packaging

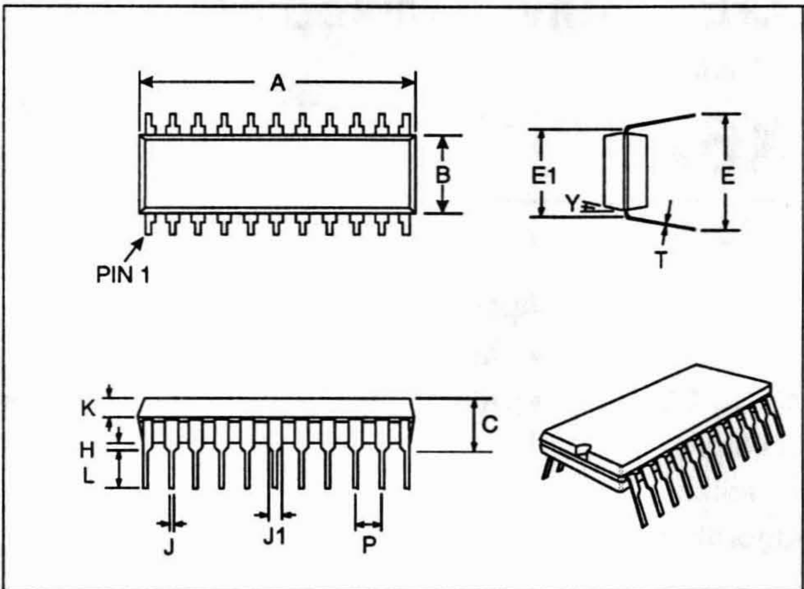

E
B
D
A
W
PIN 1
C
K
Y
J
W
T
H
P
G
F

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin PLCC (LH) Mechanical Outline: *Order as part no. MX619LH*

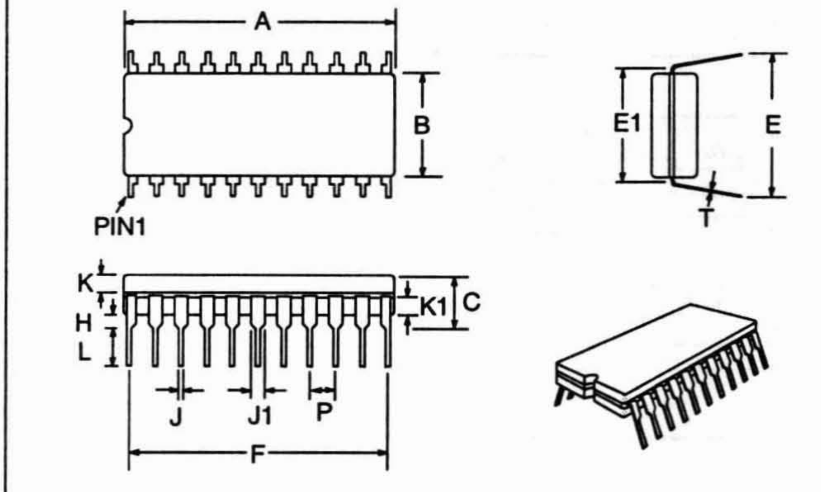


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 22-pin PDIP (P) Mechanical Outline: ***Order as part no. MX619P***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 22-pin CERDIP (J) Mechanical Outline: ***Order as part no. MX619J***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX629

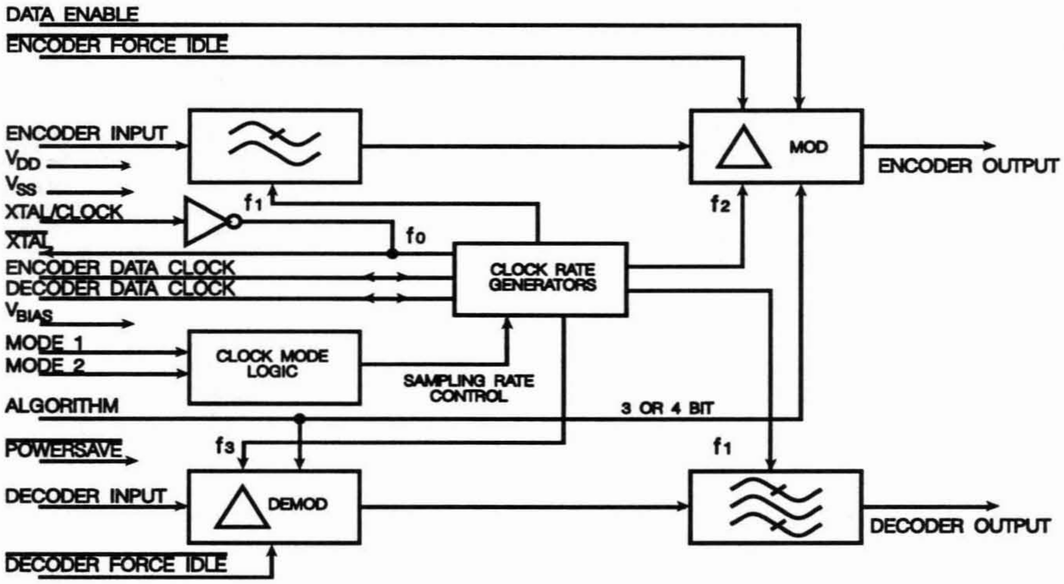
DELTA MODULATION CODEC
meets Mil-Std-188-113

Features

- **Meets Mil-Std-188-113**
- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input and Output Filters**
- **Programmable Sampling Clocks**
- **3- or 4-bit Companding Algorithm**
- **Powersave Capabilities**
- **Low Power, 5.0V Operation**

Applications

- **Military Communications**
- **Multiplexers, Switches, & Phones**


DATA ENABLE
$\overline{\text{ENCODER FORCE IDLE}}$
ENCODER INPUT
V_{DD}
V_{SS}
XTAL/CLOCK
$\overline{\text{XTAL}}$
ENCODER DATA CLOCK
DECODER DATA CLOCK
V_{BIAS}
MODE 1
MODE 2
ALGORITHM
$\overline{\text{POWERSAVE}}$
DECODER INPUT
$\overline{\text{DECODER FORCE IDLE}}$
f_1
f_0
f_2
f_3
f_1
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 OR 4 BIT
MOD
DEMOD
ENCODER OUTPUT
DECODER OUTPUT

The MX629 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches, and phones. The MX629 is designed to meet Mil-Std-188-113 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010...pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

The MX629 operates with a supply voltage of 5.0V and is available in the following packages: 24-pin PLCC (MX629LH), 22-pin CERDIP (MX629J), and 22-pin PDIP (MX629P).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

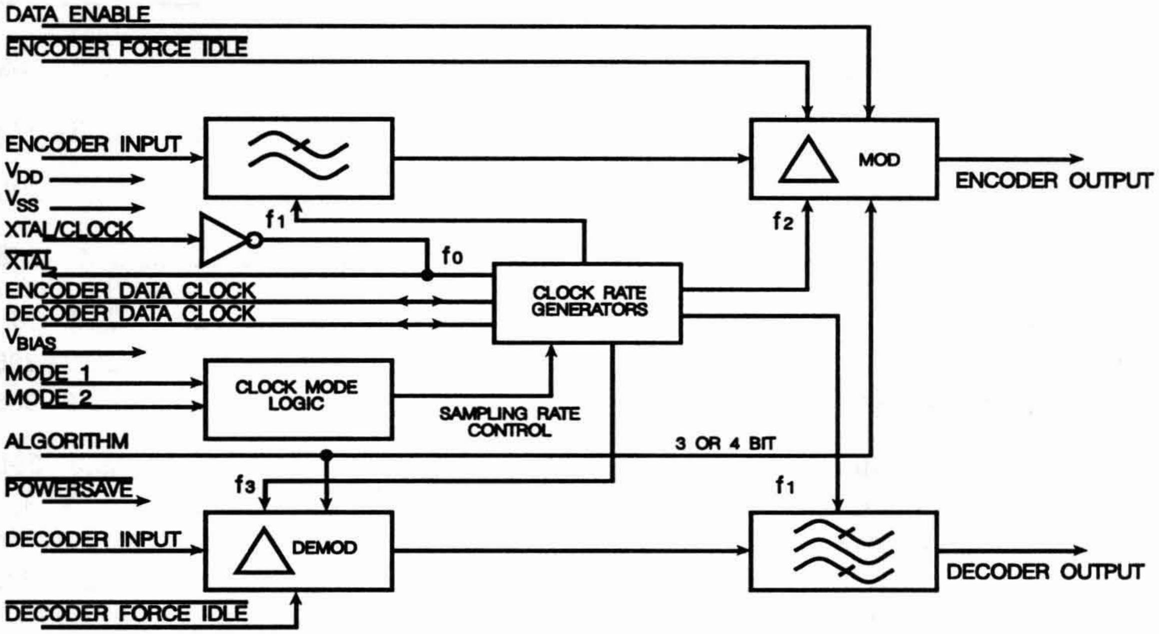

DATA ENABLE
ENCODER FORCE IDLE
ENCODER INPUT
VDD
VSS
XTAL/CLOCK
XTAL
ENCODER DATA CLOCK
DECODER DATA CLOCK
VBIAS
MODE 1
MODE 2
ALGORITHM
POWERSAVE
DECODER INPUT
DECODER FORCE IDLE
f1
f0
f2
f3
f1
MOD
ENCODER OUTPUT
CLOCK RATE GENERATORS
CLOCK MODE LOGIC
SAMPLING RATE CONTROL
3 OR 4 BIT
DEMOD
DECODER OUTPUT

Figure 1: Block Diagram

2 Signal List

J/P	LH	Name	Signal	Description
1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 2.
	2	N/C		No Connection
2	3	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4	N/C		No Connection
4	5	Encoder Data Clock	input/ output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and $\overline{\text{Powersave}}$ inputs. See Table 2.
6	7	$\overline{\text{Encoder Force Idle}}$		When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1MΩ pullup.
7	8	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9	N/C		No Connection
9	10	V_{BIAS}		Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V_{SS} when "$\overline{\text{Powersave}}$" is a logical "0".
10	11	Encoder Input	input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 2.
11	12	V_{SS}	power	Negative Supply
12	13	N/C		No Connection
13	14	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15	N/C		No Connection
15	16	$\overline{\text{Powersave}}$		A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 MΩ pullup.
	17	N/C		No Connection
16	18	$\overline{\text{Decoder Force Idle}}$		A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical "1" the decoder operates as normal. Internal 1MΩ pullup.
17	19	Decoder Input		The received digital signal input. Internal 1 MΩ pullup.
18	20	Decoder Data Clock	input/ output	A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm		A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

J/P	LH	Name	Signal	Description
20	22	Clock Mode 2		Clock rates refer to f = 1024MHz Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1MΩ pullups. See Table 3.
21	23	Clock Mode 1		
22	24	V_{DD}	power	Positive Supply. A single 5.0V supply is required.

Table 1: Signal List

Data Enable	Powersave	Encoder Output
1	1	Enable
0	1	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kbps = f/16
1	0	Internal, 32kbps = f/32
1	1	Internal, 16kbps = f/64

Table 3: Clock Mode

3 External Components

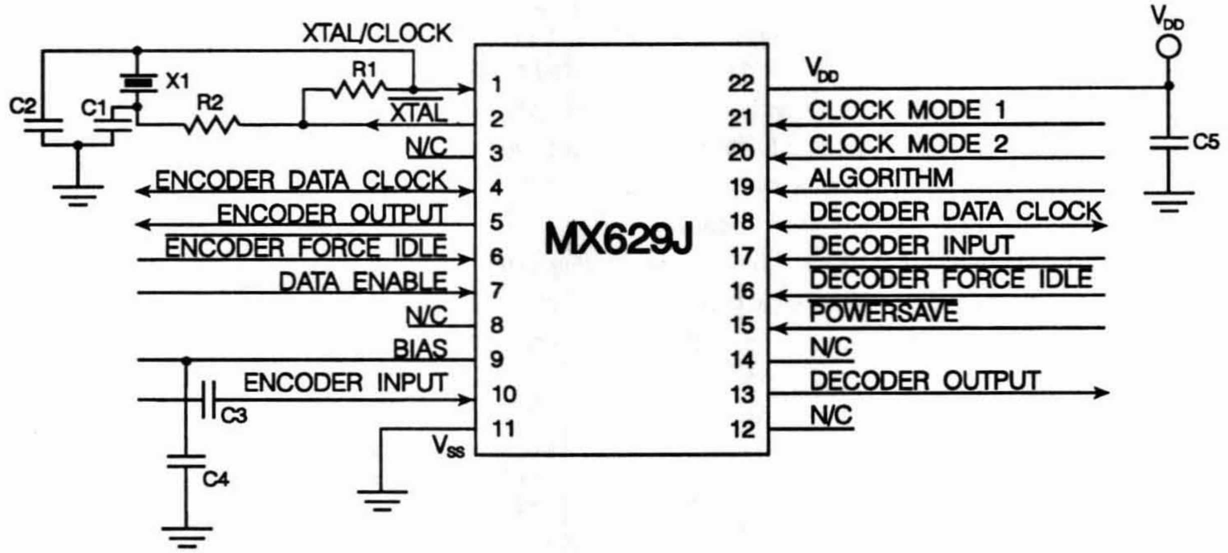

XTAL/CLOCK
X1
R1
R2
C2
C1
XTAL
N/C
ENCODER DATA CLOCK
ENCODER OUTPUT
ENCODER FORCE IDLE
DATA ENABLE
N/C
BIAS
ENCODER INPUT
C3
C4
V_{SS}
1
2
3
4
5
6
7
8
9
10
11
MX629J
22
21
20
19
18
17
16
15
14
13
12
V_{DD}
CLOCK MODE 1
CLOCK MODE 2
ALGORITHM
DECODER DATA CLOCK
DECODER INPUT
DECODER FORCE IDLE
POWERSAVE
N/C
DECODER OUTPUT
N/C
V_{DD}
C5

Figure 2: Recommended External Components for Typical Application

R1	Note 1	1MΩ	±10%
R2	Note 2	Selectable	
C1	Note 3	33pF	±20%
C2	Note 3	68pF	±20%

C3	Note 4	1.0µF	±20%
C4	Note 5	1.0µF	±20%
C5	Note 6	1.0µF	±20%
X1	Note 7, 8	1.024MHz	

Table 4: Recommended External Components for Typical Application

Notes:

1. Oscillator inverter bias resister.
2. Xtal Drive limiting resistor.
3. Xtal circuit load capacitor.
4. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with even lower source impedance.
5. Bias decoupling capacitor
6. V_{DD} decoupling capacitor
7. A 1.024MHz Xtal/Clock input will yield exactly 16/32/64kbps data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note.
8. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult you crystal manufacturer.

4 General Description

The MX629 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches and phones. The MX629 is designed to meet Mil-Std-188-113 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010...pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

5 Application

Due to the very low levels of a signal idle channel noise specified for military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

1. Care should be taken in the design and layout of the printed circuit board.
2. All external components (as recommended in Figure 2) should be kept close to the package.
3. Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.
4. Xtal/Clock tracks should be kept well away from analog inputs and outputs.
5. Inputs and outputs should be screened whenever possible.
6. A 'ground plane' connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.
7. It is recommended that the power supply rails have less that $1mV_{RMS}$ of noise allowed.
8. The source impedance to the Encoder Input pin must be less that 100W; output idle channel, noise levels will improve with even power source impedances.

5.1 CODEC Integration

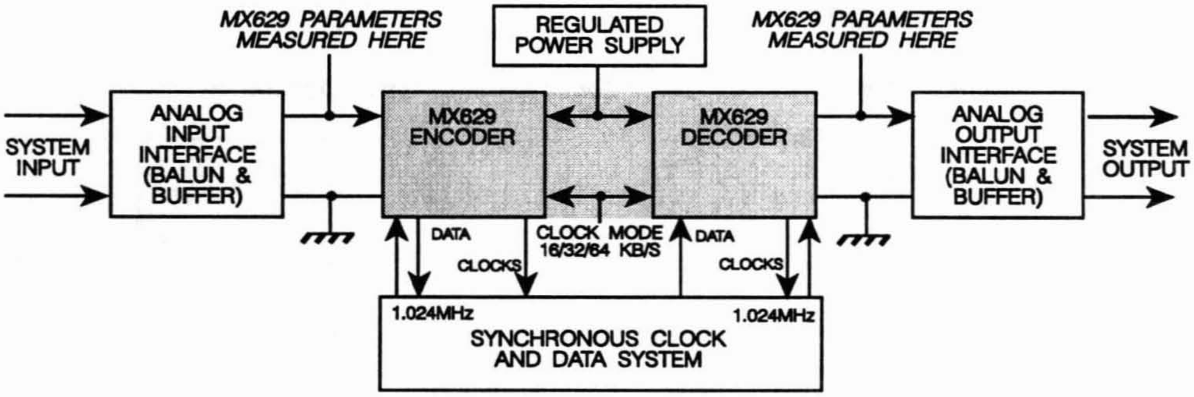

MX629 PARAMETERS MEASURED HERE
REGULATED POWER SUPPLY
MX629 PARAMETERS MEASURED HERE
SYSTEM INPUT
ANALOG INPUT INTERFACE (BALUN & BUFFER)
MX629 ENCODER
MX629 DECODER
ANALOG OUTPUT INTERFACE (BALUN & BUFFER)
SYSTEM OUTPUT
DATA
CLOCKS
CLOCK MODE 16/32/64 KB/S
DATA
CLOCKS
1.024MHz
1.024MHz
SYNCHRONOUS CLOCK AND DATA SYSTEM

Figure 3: System Configuration using the MX629

5.2 Digital to Analog Performance

Sample Rate	Bit Sequence at Decoder Input	'Run of Threes' (%)	Output level (dBm0)
16kbps	11011011010010010010	0	-29.2±2
32kbps	1101101101010100100100100100101010110110	0	-30.0±2
16kbps	1111101101000010010	30	0±1
32kbps	1111110110101010000100000010010101011110	30	0±1

Table 5: Bit Sequence Test and Results

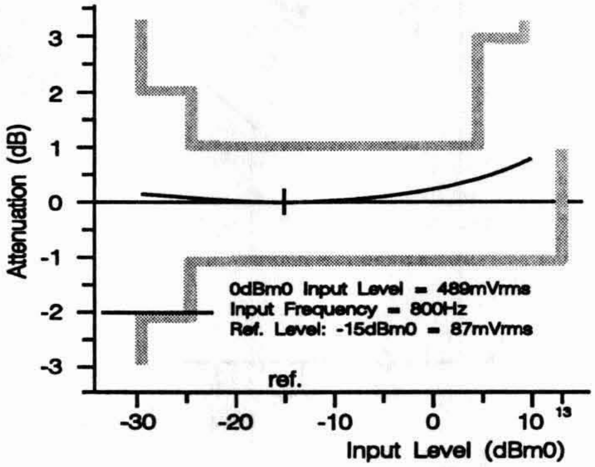


Figure 4: Gain vs. Input Level (16kbps)

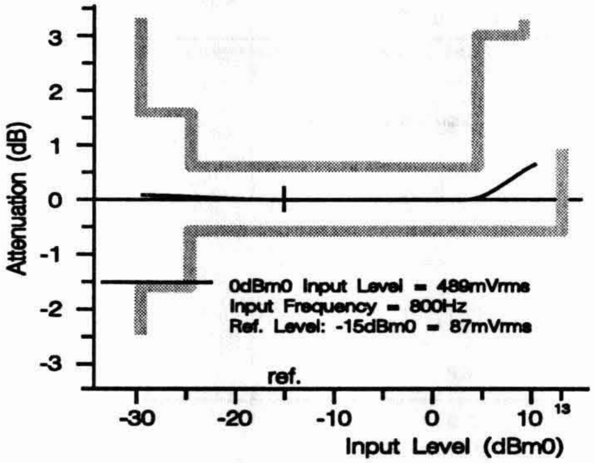


Figure 5: Gain vs. Input Level (32kbps)

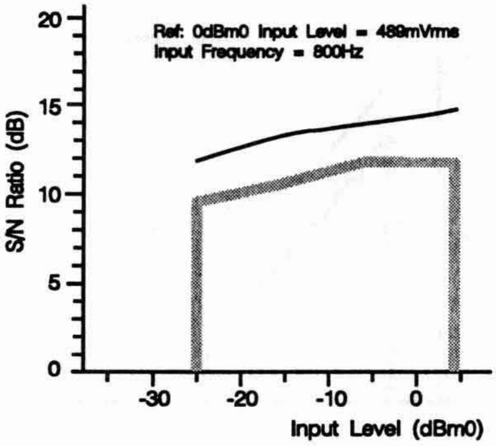


Figure 6: S/N vs. Input Level (16kbps)

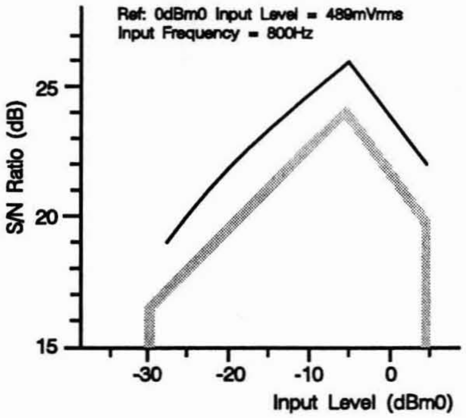


Figure 7: S/N vs. Input Level (32kbps)

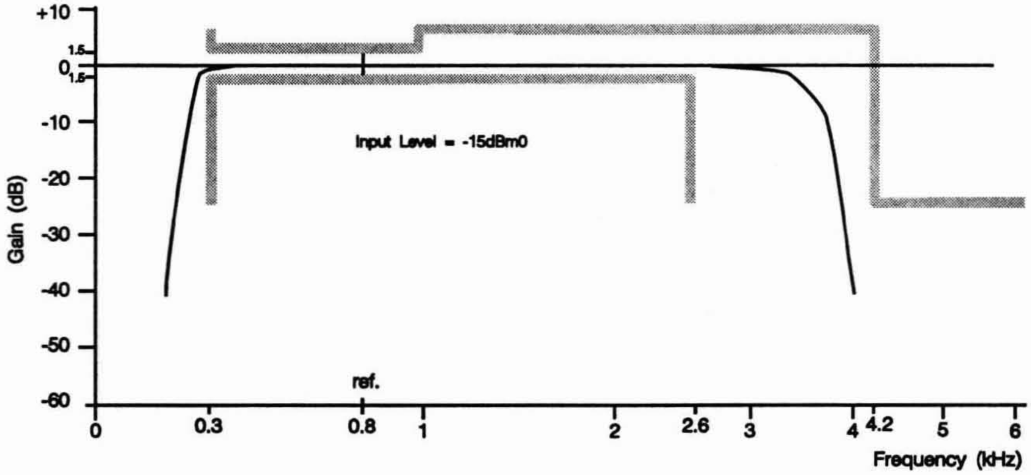


Figure 8: Attenuation distrotion vs. Frequency (16kbps)

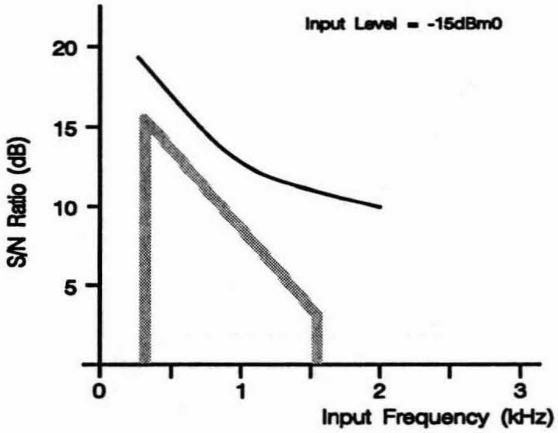


Figure 9: S/N vs. Input Frequency (16kbps)

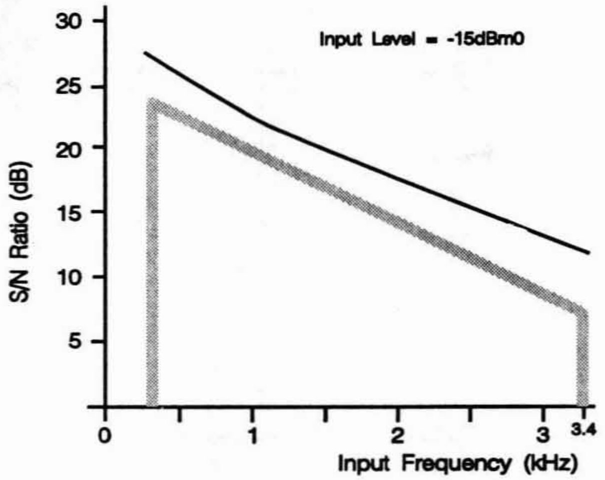


Figure 10: S/N vs. Input Frequency (32kbps)

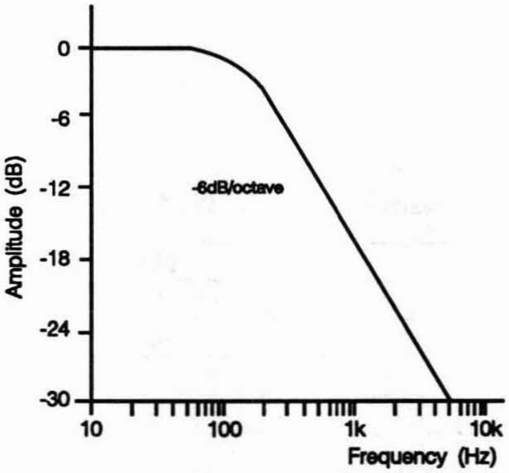


Figure 11: Principal Integrator Response

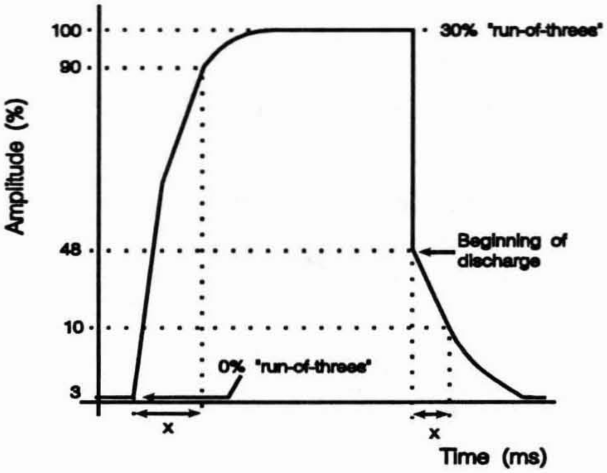


Figure 12: Compand Envelope

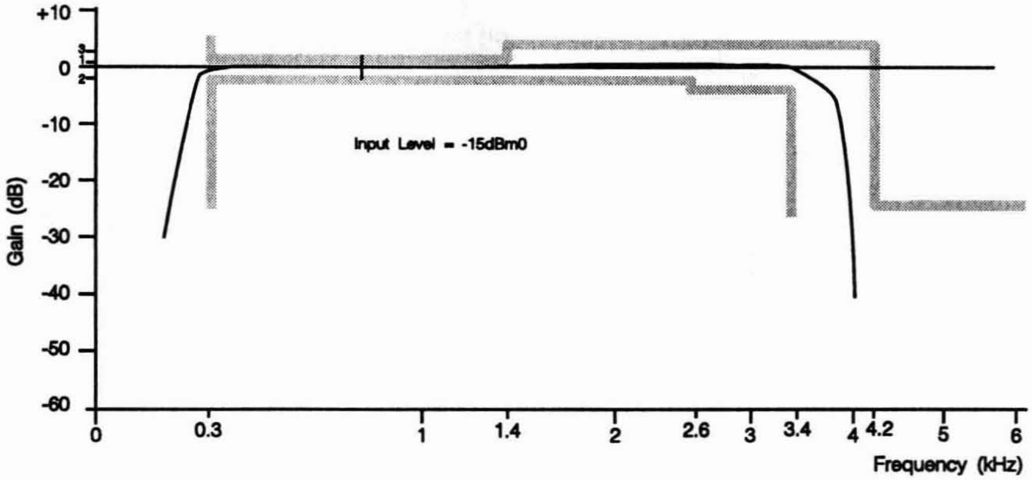


Figure 13: Attenuation Distortion vs. Frequency (32kbps)

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
J / P / LH Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C	-	800	mW
Derating above 25°C	-	10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	4.5	5.0	5.5	V
Operating Temperature	-40		85	°C
Xtal Frequency	500	1.024	1500	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0V at T_{AMB} = 25°C, Audio Test Frequency = 820Hz Xtal/Clock f_0 = 1.024MHz
3-bit Compand Algorithm, Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV$_{RMS}$.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)			5.5		mA
Supply Current (Powersave)			400		µA
Input logic '1'	8	3.5			V
Input Logic '0'	8			1.5	V
Output Logic '1'		4.0			V
Output Logic '0'				1.0	V
Digital input Impedance					
Logic I/O pins		1.0	10		MΩ
Logic Input pins, Pullup Resistor	2	300			kΩ
Digital output impedance				4	kΩ
Analog Input Impedance	4		1		kΩ
Analog Output Impedance	7			800	Ω
Three State Output Leakage		-4		4	µA
Insertion Loss	3	-2		2	dB
Dynamic Values	1,9				
Encoder					
Analog signal Input levels	5, 9	-35		12	dBmO
Principal Integrator Frequency		127	159	212	Hz
Encoder Passband			3400		Hz
Compand Time Constant		4.0	5.0	6.0	ms
Decoder					
Analog Signal Output Levels	5, 9	-35		12	dBmO
Decoder Passband		300		3400	Hz
Encoder Decoder (Full Codec)					
Compression Ration (Cd = 0.3 to Cd = 0.0)			16:1		
Passband		300		3400	Hz
Stopband		4.2			KHz
Stopband Attenuation					
4200Hz to 6000Hz		25			dB
>6000Hz			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
300Hz – 1400Hz		-1		1	dB
1400Hz – 2600Hz		-1		1	dB
2600Hz –3400Hz		-2		3	dB
Output Noise (Input Short Circuit)	9		-55		dBmO
Perfect Idle Channel Noise					
(Encode Forced)	9		-57		dBmO

	Notes	Min.	Typ.	Max.	Units
Group Delay Distrotion	4				
(1000Hz-2600Hz)	6			450	µs
(600Hz-2800Hz)	6			750	µs
(500Hz-3000Hz)	6			1.5	ms
Xtal/clock Frequency			1024		kHz

Notes:

1. Dynamic characteristics are specified at 5.0V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data clocks
3. For and encoder/Decoder combination, Insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 4, 5, 6, and 7.
6. Group Delay Distortion for the full codec is relative to the delay with and 820Hz, -20dB signal at the encoder input
7. An Emitter Follower output stage.
8. 4V = 80%V_{DD}, 3.5V = 70%V_{DD}, 1.5V = 30%V_{DD}, 1V = 20%V_{DD}
9. Analog Voltage Levels used: 0dBmO = 489mV_{RMS} = -4dBm = 0dB. –15dBmO = 87mV_{RMS}. –20dBmO = 49mV_{RMS} = -24dBm.

6.1.4 TIMING

Serial Bus Timings (See Figure 14)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			µs
t_{CL}	Clock 0 pulse width	1.0			µs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
t_{SU} +t_H	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

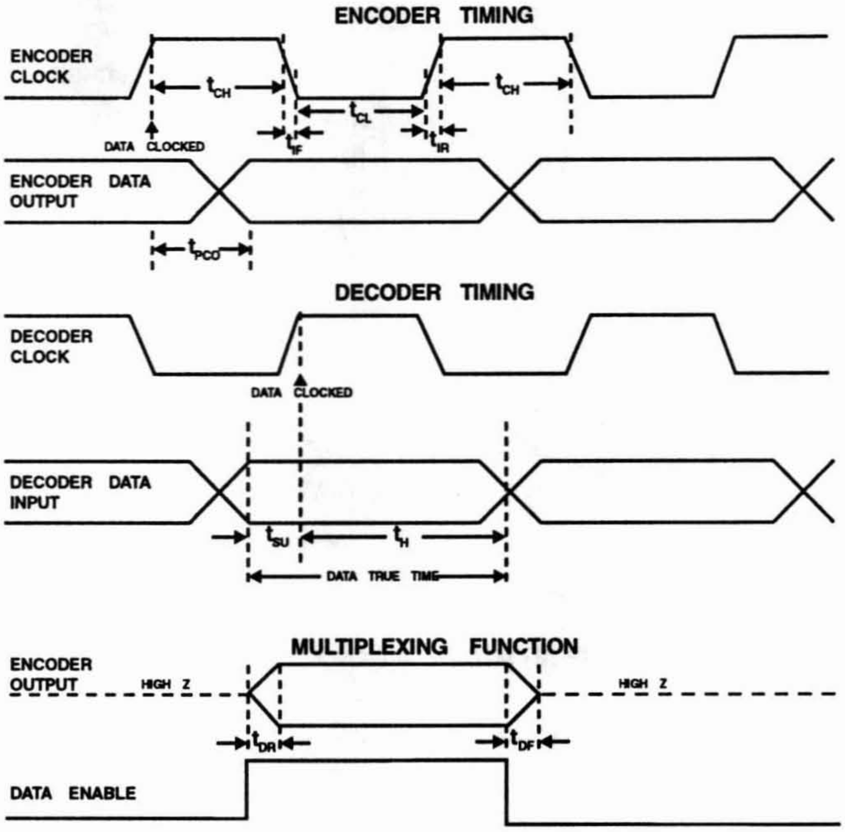
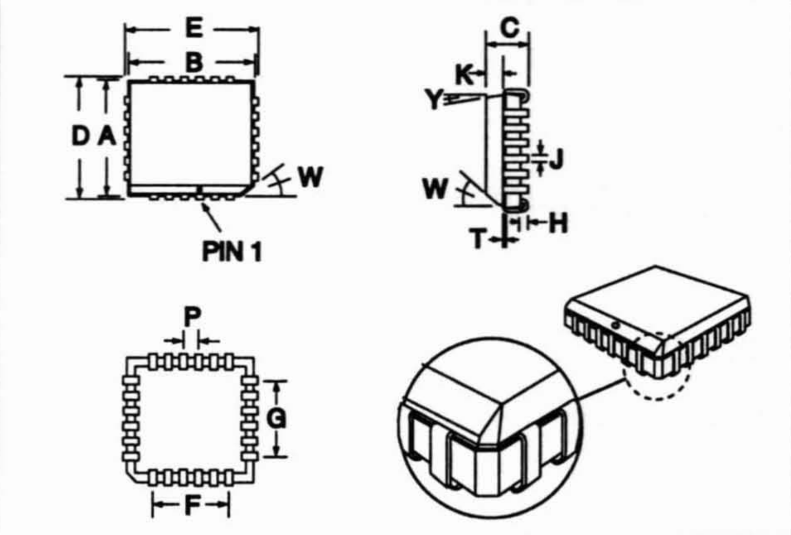

ENCODER TIMING
ENCODER CLOCK
t_{CH}
t_{CL}
t_{IF}
t_{IR}
t_{CH}
DATA CLOCKED
ENCODER DATA OUTPUT
t_{PCO}
DECODER TIMING
DECODER CLOCK
DATA CLOCKED
DECODER DATA INPUT
t_{SU}
t_H
DATA TRUE TIME
MULTIPLEXING FUNCTION
ENCODER OUTPUT
HIGH Z
HIGH Z
t_{DR}
t_{DF}
DATA ENABLE

Figure 14: CODEC Timing

6.2 Packaging

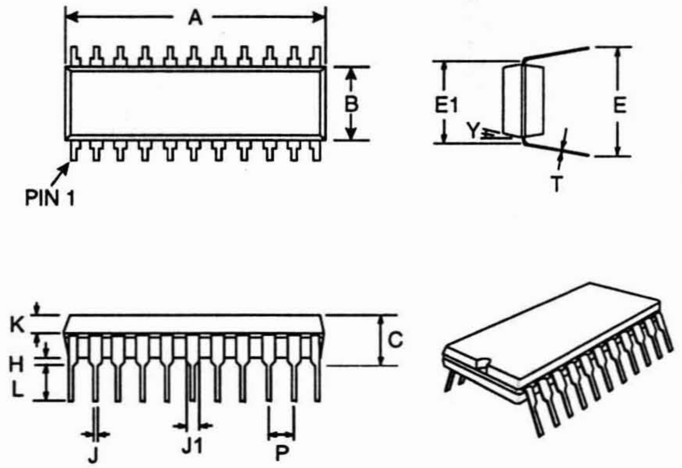

E
B
D
A
W
PIN 1
C
K
Y
J
W
T
H
P
G
F

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin PLCC (LH) Mechanical Outline: ***Order as part no. MX629LH***

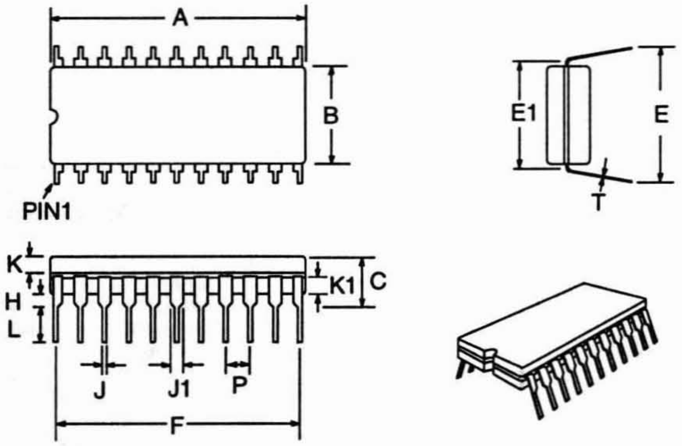


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 22-pin PDIP (P) Mechanical Outline: ***Order as part no. MX629P***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 22-pin CERDIP (J) Mechanical Outline: ***Order as part no. MX629J***

MX•COM,INC. MiXed Signal ICs

DATA BULLETIN

MX633 Call Progress Tone Detector

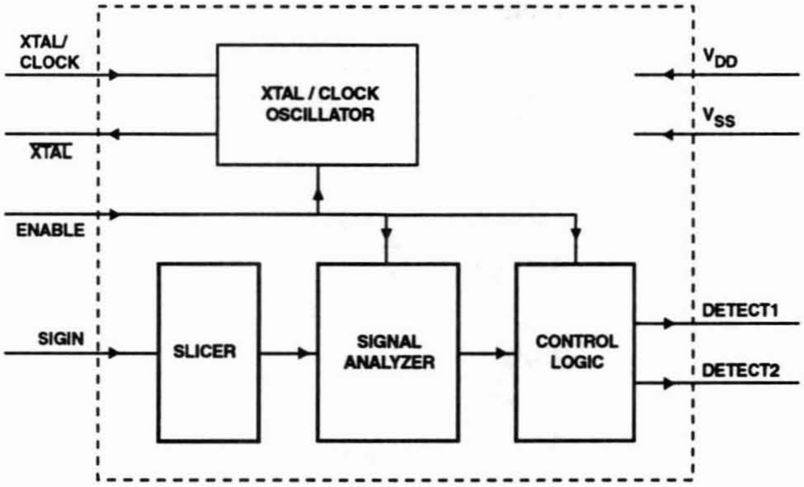
PRELIMINARY INFORMATION

Features

- Worldwide Tone Compatibility
- Single and Dual Tones Detected
- U.S. Busy-Detect Output
- Voice-Detect Output
- Wide Dynamic Range > 40dBm
- Low Supply Current (0.3mA/0.5mA)
- Low Supply Voltage (3.3V/5.0V)
- Standard 3.58MHz Xtal

Applications

- Automatic Calling Products



The MX633 is a low cost, low power device that uses signal processing techniques to detect audible tone signals such as Dial, Ringing, Busy and other conditions found when placing a call throughout the world's telecom systems. Detection of these call progress stages is essential to the proper operation of automatic calling products.

The MX633 adds new features to Call Progress monitoring. It detects and indicates the 'U.S. Busy' tones, reducing the need to measure 'tone cadence' to identify 'U.S. Busy'. It also detects and indicates voice and other signals from Call Progress tones, reducing voice-falsing and adding voice-answer as a connection prompt.

The MX633 may be used with a 3.0V to a 5.5V supply and is available in the following package styles: 8-pin PDIP (MX633P), 16-pin SOIC (MX633DW), and 24-pin TSSOP (MX633TN).

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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX641 Dual SPM Detector

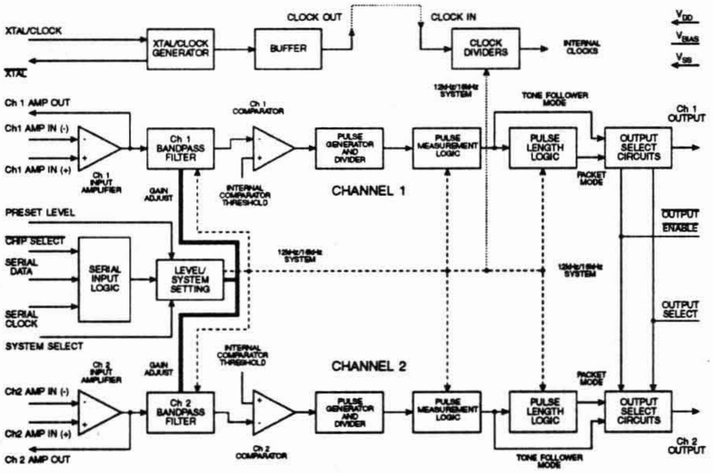
PRELIMINARY INFORMATION

Features

- Two (12kHz / 16kHz) SPM Detectors on a Single Chip
- Detects 12 or 16kHz SPM Frequencies
- 'Controlled' (µC) & 'Fixed' Signal Sensitivity Modes
- Selectable Tone Follower or Packet Mode Outputs
- High Speech-Band Rejection Properties
- 'Output Enable' Multiplexing Facility

Applications

- Call Charge Applications on PABX Line Cards
- Remote Telephone Applications


XTAL/CLOCK
XTAL
XTAL/CLOCK GENERATOR
BUFFER
CLOCK OUT
CLOCK IN
CLOCK DIVIDERS
INTERNAL CLOCKS
V_{DD}
V_{BIAS}
V_{SS}
12kHz/16kHz SYSTEM
TONE FOLLOWER MODE
Ch 1 OUTPUT
Ch 1 AMP OUT
Ch1 AMP IN (-)
Ch1 AMP IN (+)
Ch 1 INPUT AMPLIFIER
Ch 1 BANDPASS FILTER
GAIN ADJUST
Ch 1 COMPARATOR
INTERNAL COMPARATOR THRESHOLD
PULSE GENERATOR AND DIVIDER
PULSE MEASUREMENT LOGIC
PULSE LENGTH LOGIC
OUTPUT SELECT CIRCUITS
PACKET MODE
CHANNEL 1
PRESET LEVEL
CHIP SELECT
SERIAL DATA
SERIAL CLOCK
SYSTEM SELECT
SERIAL INPUT LOGIC
LEVEL/ SYSTEM SETTING
12kHz/16kHz SYSTEM
12kHz/16kHz SYSTEM
OUTPUT ENABLE
OUTPUT SELECT
CHANNEL 2
INTERNAL COMPARATOR THRESHOLD
Ch 2 INPUT AMPLIFIER
GAIN ADJUST
Ch2 AMP IN (-)
Ch2 AMP IN (+)
Ch 2 AMP OUT
Ch 2 BANDPASS FILTER
Ch 2 COMPARATOR
PULSE GENERATOR AND DIVIDER
PULSE MEASUREMENT LOGIC
PULSE LENGTH LOGIC
PACKET MODE
OUTPUT SELECT CIRCUITS
TONE FOLLOWER MODE
Ch 2 OUTPUT

The MX641 is a low-power, system-selectable Dual Subscriber Pulse Metering (SPM) Detector designed to indicate the presence, on a telephone line, of either 12kHz or 16kHz telephone call-charge frequencies. It is designed for PBX and PABX line-card and remote telephone installations. Under µProcessor control via a common serial interface, each channel of the MX641 will detect call-charge pulses from a telephone line and provide a digital output for recording, billing or security purposes. A common set of external components and a stable 3.579545MHz Xtal/clock input ensures that the MX641 adheres accurately to most national "Must and Must-Not" decode band-edges and threshold levels. For non-µProcessor systems a preset sensitivity/system input allows external channel level and system setting

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode: logic level for the period of a correct decode.
(2) Packet mode: respond/de-respond after a cumulative period of tone or notone in a fixed (intrinsic hardwired period that is not user controlled) period.
(3) High-impedance output: for device multiplexing.

The MX641 requires a 5V supply and is available in the following packages: 24-pin SOIC (MX641DW) and 24-pin PDIP (MX641P).

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

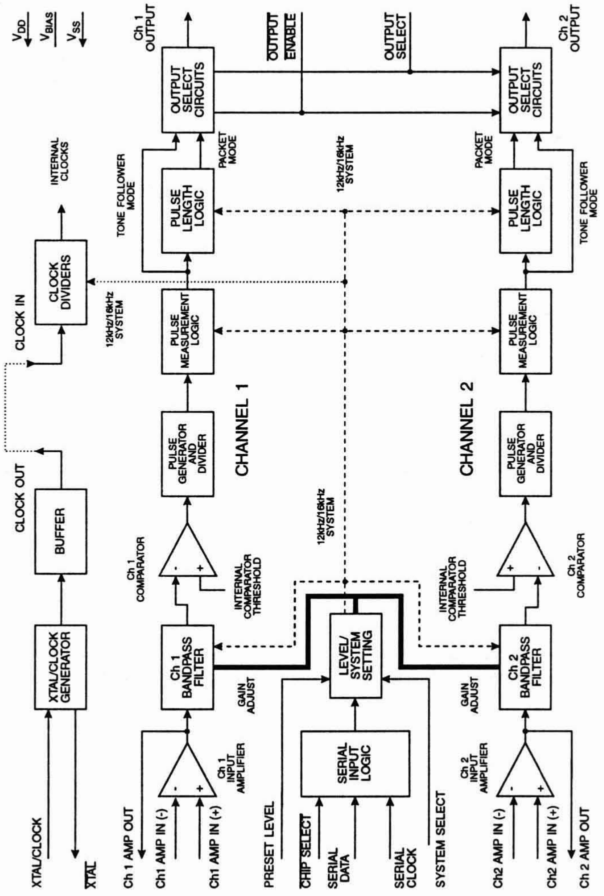

XTAL/CLOCK
XTAL
XTAL/CLOCK GENERATOR
BUFFER
CLOCK OUT
CLOCK IN
CLOCK DIVIDERS
INTERNAL CLOCKS
V_{DD}
V_{BIAS}
V_{SS}
12kHz/16kHz SYSTEM
TONE FOLLOWER MODE
Ch 1 OUTPUT
Ch 1 AMP OUT
Ch1 AMP IN (-)
Ch1 AMP IN (+)
Ch 1 INPUT AMPLIFIER
Ch 1 BANDPASS FILTER
Ch 1 COMPARATOR
INTERNAL COMPARATOR THRESHOLD
PULSE GENERATOR AND DIVIDER
PULSE MEASUREMENT LOGIC
PULSE LENGTH LOGIC
OUTPUT SELECT CIRCUITS
PACKET MODE
CHANNEL 1
GAIN ADJUST
PRESET LEVEL
CHIP SELECT
SERIAL DATA
SERIAL INPUT LOGIC
LEVEL/ SYSTEM SETTING
SERIAL CLOCK
SYSTEM SELECT
12kHz/16kHz SYSTEM
12kHz/16kHz SYSTEM
OUTPUT ENABLE
OUTPUT SELECT
CHANNEL 2
GAIN ADJUST
INTERNAL COMPARATOR THRESHOLD
PACKET MODE
Ch 2 INPUT AMPLIFIER
Ch2 AMP IN (-)
Ch2 AMP IN (+)
Ch 2 AMP OUT
Ch 2 BANDPASS FILTER
Ch 2 COMPARATOR
PULSE GENERATOR AND DIVIDER
PULSE MEASUREMENT LOGIC
PULSE LENGTH LOGIC
OUTPUT SELECT CIRCUITS
Ch 2 OUTPUT
TONE FOLLOWER MODE

Figure 1: Block Diagram

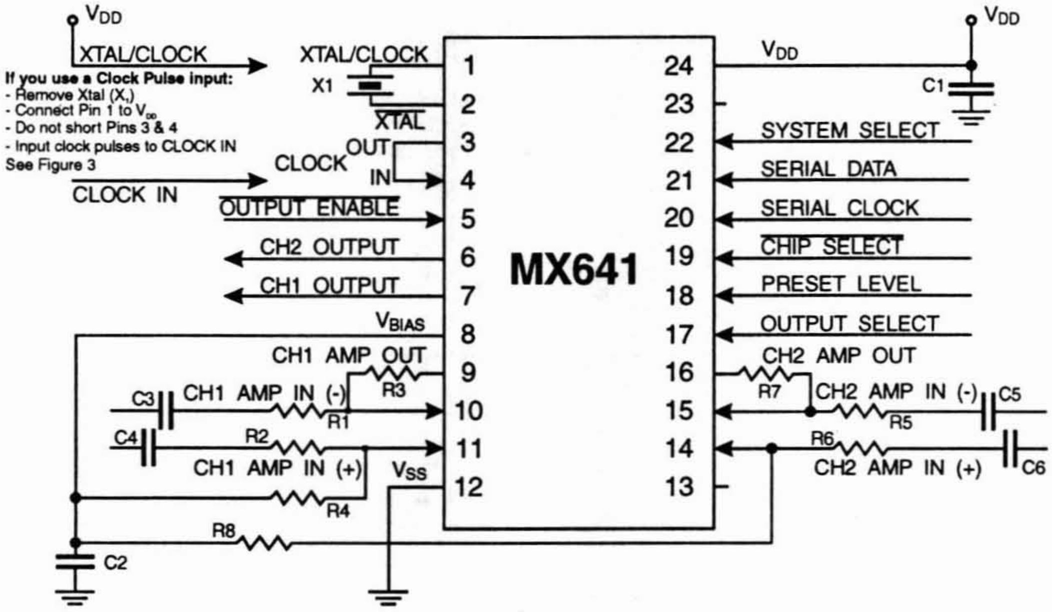
2. Signal List

Pin No.	Name	Type	Description
1	Xtal/Clock	input	The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is used at the Clock In pin, this (Xtal/Clock) pin must be connected directly to V_{DD} (see Figure 2). See Figure 3 for details of clock frequency distribution.
2	$\overline{\text{XTAL}}$	output	The output of the on-chip clock oscillator inverter.
3	Clock Out	output	The buffered output of the on-chip-clock oscillator inverter. If a Xtal input is used, this output should be connected directly to the Clock In pin. This output can support up to 3 additional MX641 ICs. See Figure 3 for details of clock frequency distribution.
4	Clock In	input	The 3.579545 clock pulse input to the internal clock dividers. If an externally generated clock pulse input is used, the Xtal/Clock input pin should be connected to V_{DD}.
5	$\overline{\text{Output Enable}}$	input	For multi-chip output multiplexing; controls the state of both Ch1 and Ch2 outputs. When this input is placed high (logic '1') both outputs are set to a high impedance. When placed low (logic '0') both outputs are enabled.
6	Ch 2 Output	output	The digital output of the Channel 2 SPM detector when enabled. The format of the signal at this pin, in common with Ch 1, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
7	Ch 1 Output	output	The digital output of the Channel 1 SPM detector when enabled. The format of the signal at this pin, in common with Ch 2, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
8	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
9	Ch 1 Amp Out	output	The output of the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
10	Ch 1 Amp In (-):	input	The negative input to the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
11	Ch 1 Amp In (+):	input	The positive input to the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
12	V_{SS}	power	Negative supply (GND).
13	N/C		No internal connection; leave open circuit.
14	Ch 2 Amp In (+):	input	The positive input to the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
15	Ch 2 Amp In (-):	input	The negative input to the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
16	Ch 2 Amp Out	output	The output of the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
17	Output Select	input	A logic input to set the Channel 1 and Channel 2 output modes. When high (logic '1'), the outputs are in the Tone Follower mode; when low (logic '0'), the outputs are in the Packet mode.
18	Preset Level	input	A logic input to set the sensitivity mode of the MX641. When high (logic '1'), both channels are in the Fixed Sensitivity mode. The external components govern the input sensitivity; the System Select input selects 12kHz or 16kHz operation. When low (logic '0'), both channels are in the Controlled Sensitivity mode. Device sensitivities and system selection are via the Chip Select/Serial Data/Serial Clock inputs. This input has an internal pullup resistor on chip (Fixed Sensitivity Mode).
19	$\overline{\text{Chip Select}}$	input	The Chip Select input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). The device is selected when this input is set low (logic '0'). When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.

Pin No.	Name	Type	Description
20	Serial Clock	input	The Serial Clock input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). Data is loaded to the MX641 on this clock's rising edge. When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
21	Serial Data	input	The Serial Data input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9 and Table 4). When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
22	System Select	input	In the Fixed Sensitivity mode this pin selects the system frequency. High (logic '1') = 12kHz; Low (logic '0') = 16kHz. In the Controlled Sensitivity mode this pin is inactive and may be left unconnected. This pin has an internal pullup resistor on chip.
23	N/C		No internal connection; leave open circuit.
24	V_{DD}	power	Positive supply rail; a single, stable power supply is required. Critical levels and voltages within the MX641 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin

Table 1: Signal List

3. External Components


VDD
XTAL/CLOCK
XTAL/CLOCK
X1
XTAL
CLOCK
OUT
IN
CLOCK IN
OUTPUT ENABLE
CH2 OUTPUT
CH1 OUTPUT
VBIAS
CH1 AMP OUT
R3
C3
CH1 AMP IN (-)
R1
C4
R2
CH1 AMP IN (+)
VSS
R4
R8
C2
MX641
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
C1
SYSTEM SELECT
SERIAL DATA
SERIAL CLOCK
CHIP SELECT
PRESET LEVEL
OUTPUT SELECT
CH2 AMP OUT
R7
CH2 AMP IN (-)
C5
R5
R6
CH2 AMP IN (+)
C6

If you use a Clock Pulse input:
- Remove Xtal (X_1)
- Connect Pin 1 to V_{DD}
- Do not short Pins 3 & 4
- Input clock pulses to CLOCK IN

See Figure 3

Figure 2: Recommended External Components

R1		68kΩ	± 1%
R2		68kΩ	±1%
R3	Note 1	750kΩ	±1%
R4	Note 1	750kΩ	±1%
R5		68kΩ	± 1%
R6		68kΩ	± 1%
R7	Note 1	750kΩ	±1%
R8	Note 1	750kΩ	±1%

C1		1.0µF	±20%
C2		1.0µF	±20%
C3		270pF	±5%
C4		270pF	±5%
C5		270pF	±5%
C6		270pF	±5%
X1	Note 2, 3	3.579545MHz	

Table 2: Recommended External Components

Note:

1. Fixed Sensitivity Setting: when calculating/selecting gain components, R3, R4, R7 and R8 should always be greater than or equal to 100kΩ.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The on-chip crystal circuitry includes a feedback resistor (nominally 2MΩ) between pins 1 & 2 and load capacitors on pins 1 & 2 (nominally 10pF each, excluding package and board parasitics).

4. General Description

4.1 Xtal/Clock Distribution

The MX641 requires a 3.579545MHz Xtal or clock pulse input. With the exception of the Xtal, all oscillator components are incorporated on chip. If a Xtal input is employed the Clock Out pin should be directly linked to the Clock In pin.

To reduce component and layout complexity, the clock requirements of up to 3 additional MX641 microcircuits may be supplied from a Xtal-driven MX641 acting as the system master clock. With reference to Figure 3, the clock should be distributed as illustrated and the Xtal/Clock pins of the driven microcircuits should be connected directly to V_{DD}.
Note (see section 6.1.3) that the maximum load on the master Clock Out pin should not be exceeded.

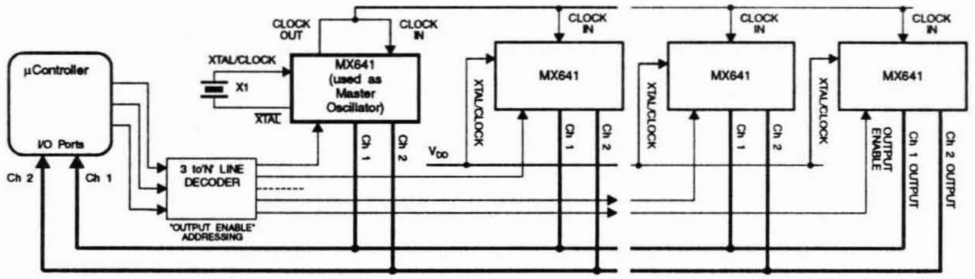

CLOCK OUT
CLOCK IN
CLOCK IN
CLOCK IN
CLOCK IN
µController
I/O Ports
XTAL/CLOCK
X1
XTAL
MX641 (used as Master Oscillator)
MX641
MX641
MX641
XTAL/CLOCK
XTAL/CLOCK
XTAL/CLOCK
Ch 1
Ch 2
Ch 1
Ch 2
Ch 1
Ch 2
V_{DD}
OUTPUT ENABLE
Ch 1 OUTPUT
Ch 2 OUTPUT
Ch 2
Ch 1
3 to'N' LINE DECODER
"OUTPUT ENABLE" ADDRESSING

Figure 3: Xtal/Clock Distribution and Output Multiplexing

4.2 Channel Outputs

Channel 1 and Channel 2 outputs operate together under the control of the Output Enable and Output Select inputs. Table 3 describes the operations.

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode: a logic level for the period of a correct decode.
(2) Packet mode: respond/de-respond after a cumulative period of tone or notone in a fixed (intrinsic hardwired period that is not user controlled) period.
(3) High-impedance output: for device multiplexing.

System Select	Preset Level	Output Select	Output Enable	Operating Mode		
				Mode	Sensitivity	Frequency
X	0	0	0	Packet Mode Output;	Serial Data Control (see note)	
X	0	1	0	Tone Follower Output;	Serial Data Control (see note)	
0	1	0	0	Packet Mode Output;	Fixed Sensitivity	16kHz
1	1	0	0	Packet Mode Output;	Fixed Sensitivity	12kHz
0	1	1	0	Tone Follower Output;	Fixed Sensitivity	16kHz
1	1	1	0	Tone Follower Output;	Fixed Sensitivity	12kHz
X	X	X	1	Tristate Output (High Z)		

X = don't care

Note: Device sensitivity and system frequency must be serially loaded

Table 3: Operating Mode Configuration

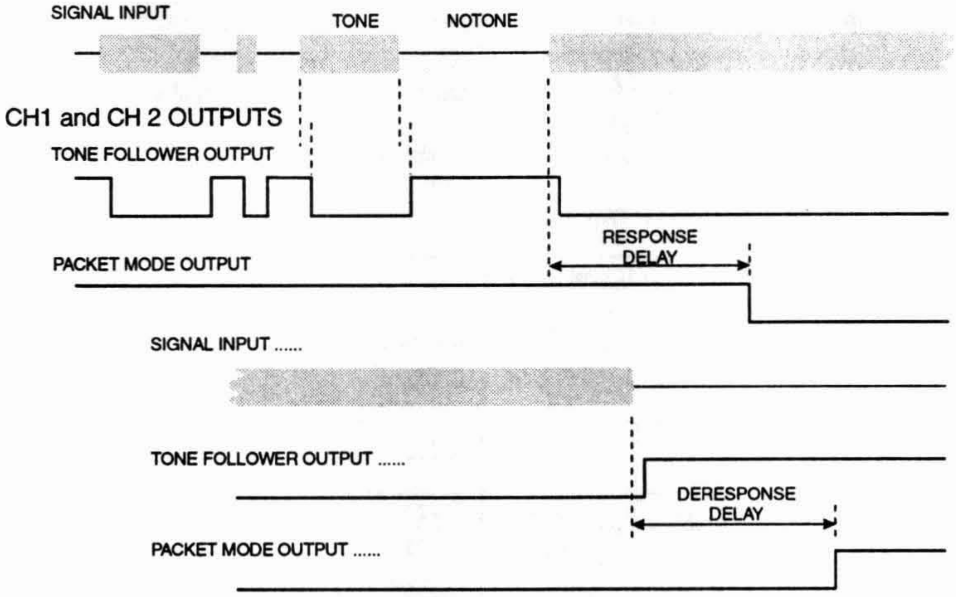


Figure 4: Tone Follower and Packet Mode Outputs

4.3 Sensitivity Setting

To enable the MX641 to operate correctly to most national 12kHz and 16kHz SPM specifications, the input sensitivity can be accurately adjusted and set.

There are two different pin-selectable modes of sensitivity setting available to the MX641: Controlled Sensitivity Mode and Fixed Sensitivity Mode

The Controlled Sensitivity mode allows the sensitivity setting from a µController via a 6-bit serial data input. This same serial input also sets operation (bit 0) to either 12kHz or 16kHz systems. Both channels are set identically.

The Fixed Sensitivity mode allows the sensitivity of each channel to be set to a fixed "gain" by external components at the input amplifiers. Operation to either 12kHz or 16kHz is by the System Select input.

4.3.1 Controlled Sensitivity Setting

With the external gain (sensitivity) components used as shown in Figure 2, the gain of the input stages is 19.8dB (12kHz) or 20.5dB (16kHz). For controlled sensitivity setting the gain of each bandpass filter, and therefore the device sensitivity, is adjusted by the applied serial bits D1 to D5.

In the Controlled Sensitivity mode the system frequency is selected by bit D0 ('1' = 12kHz; '0' = 16kHz). Data is loaded Bit 5 (D5) first. Table 4 details the serial data inputs for the required sensitivity. Minimum, Nominal and Maximum Sensitivity figures are provided to make complete allowance for internal circuit offsets and component tolerances. 0dB(ref.) = 775mV$_{RMS}$ at V$_{DD}$ = 5.0 volts; varies directly with V$_{DD}$.

Note: Device sensitivity is directly proportional to V$_{DD}$

4.3.1.1 Controlled Sensitivity Setting Information

The sensitivity figures in Table 4 are based on the following:

1. The recommended amplifier components (see Figure 2) are used, providing an amplifier gain at 16kHz of 19.8dB ±0.3dB or at 12kHz of 19.1dB ±0.3dB.
2. A comparator sensitivity of 1.6dB(ref.) ±1dB (the variation is due to filter gain error, filter output offset, comparator input offset or a combination of all 3).
3. The applied V_{DD} is 5.0 volts; 0dB (ref.) = 775mV_{RMS}.

		12kHz System Bit D0 = '1'			**16kHz System Bit D0 = '0'**		
Serial Data Bits	**Bandpass Filter Gain**	**Minimum Sensitivity**	**Nominal Sensitivity**	**Maximum Sensitivity**	**Minimum Sensitivity**	**Nominal Sensitivity**	**Maximum Sensitivity**
D5 - D1	(dB)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)
00000	0	-16.2	-17.5	-18.8	-16.9	-18.2	-19.5
00001	1.0	-17.2	-18.5	-19.8	-17.9	-19.2	-20.5
00010	2.0	-18.2	-19.5	-20.8	-18.9	-20.2	-21.5
00011	3.0	-19.2	-20.5	-21.8	-19.9	-21.2	-22.5
00100	4.0	-20.2	-21.5	-22.8	-20.9	-22.2	-23.5
00101	5.0	-21.2	-22.5	-23.8	-21.9	-23.2	-24.5
00110	6.0	-22.2	-23.5	-24.8	-22.9	-24.2	-25.5
00111	7.0	-23.2	-24.5	-25.8	-23.9	-25.2	-26.5
01000	8.0	-24.2	-25.5	-26.8	-24.9	-26.2	-27.5
01001	9.0	-25.2	-26.5	-27.8	-25.9	-27.2	-28.5
01010	10.0	-26.2	-27.5	-28.8	-26.9	-28.2	-29.5
01011	11.0	-27.2	-28.5	-29.8	-27.9	-29.2	-30.5
01100	12.0	-28.2	-29.5	-30.8	-28.9	-30.2	-31.5
01101	13.0	-29.2	-30.5	-31.8	-29.9	-31.2	-32.5
01110	14.0	-30.2	-31.5	-32.8	-30.9	-32.2	-33.5
01111	15.0	-31.2	-32.5	-33.8	-31.9	-33.2	-34.5
10000	16.0	-32.2	-33.5	-34.8	-32.9	-34.2	-35.5
10001	17.0	-33.2	-34.5	-35.8	-33.9	-35.2	-36.5
10010	18.0	-34.2	-35.5	-36.8	-34.9	-36.2	-37.5
10011	19.0	-35.2	-36.5	-37.8	-35.9	-37.2	-38.5
10100	20.0	-36.2	-37.5	-38.8	-36.9	-38.2	-39.5
10101	21.0	-37.2	-38.5	-39.8	-37.9	-39.2	-40.5
10110	22.0	-38.2	-39.5	-40.8	-38.9	-40.2	-41.5
10111	23.0	-39.2	-40.5	-41.8	-39.9	-41.2	-42.5
11000	24.0	-40.2	-41.5	-42.8	-40.9	-42.2	-43.5
11001	25.0	-41.2	-42.5	-43.8	-41.9	-43.2	-44.5
11010	26.0	-42.2	-43.5	-44.8	-42.9	-44.2	-45.5
11011	27.0	-43.2	-44.5	-45.8	-43.9	-45.2	-46.5
11100 11101 11110 11111	These states should never be used. If sensitivities of this order are required (e.g. the Swedish Rural SPM specification), it is recommended that the Controlled Sensitivity setting be set to 20dB (10100) and external components selected to set the Input Amp gain to a higher figure. This action will prevent falsing by sub-harmonic frequencies.						

Table 4: Controlled Sensitivity Setting Information

4.3.1.2 German FTZ Specification (16kHz)

The FTZ system has a Must Decode level of -21dB (ref.) and a Must-Not Decode level of -27dB (ref.). Reference to Table 4 shows that Bandpass Filter Gain settings of 5dB, 6dB or 7dB will enable an MX641 channel to meet this level specification. Figure 5 illustrates the range of these various settings.

To meet the German FTZ specification, the input data (D5 to D0) must be:

	0 0 1 0 1	0	5.0dB
or	0 0 1 1 0	0	6.0dB
or	0 0 1 1 1	0	7.0dB

Note:

1. By selecting the middle setting, the greatest noise immunity is achieved.

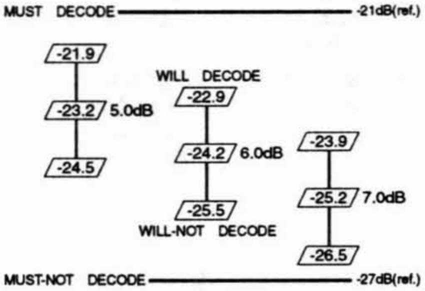

MUST DECODE
-21dB(ref.)
-21.9
WILL DECODE
-22.9
-23.2
5.0dB
-23.9
-24.2
6.0dB
-24.5
-25.2
7.0dB
-25.5
WILL-NOT DECODE
-26.5
MUST-NOT DECODE
-27dB(ref.)

Figure 5: German Specification - Possible Settings

4.3.1.3 French Specification (12kHz)

This system has a Must Decode level of -17.36dB (ref.) and a Must-Not Decode level of -23.8dB (ref.). Reference to Table 4 shows that Bandpass Filter Gain settings of 2dB, 3dB or 4dB will enable an MX641 channel to meet this level specification. Figure 6 illustrates the range of these various settings.

To meet the French SPM specification, the input data (D5 to D0) must be:

	0 0 0 1 0	1	2.0dB
or	0 0 0 1 1	1	3.0dB
or	0 0 1 0 0	1	4.0dB

Note:

1. By selecting the middle setting, the greatest noise immunity is achieved.

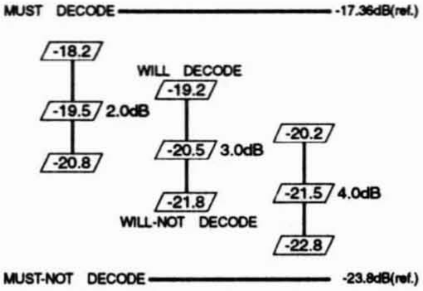

MUST DECODE
-17.36dB(ref.)
-18.2
WILL DECODE
-19.2
-19.5
2.0dB
-20.2
-20.5
3.0dB
-20.8
-21.5
4.0dB
-21.8
WILL-NOT DECODE
-22.8
MUST-NOT DECODE
-23.8dB(ref.)

Figure 6: French Specifications - Possible Settings

4.3.2 Fixed Sensitivity Setting

In this mode the sensitivity of each channel is set by the correct selection of the components around the Channel Input Amplifier. Note that the device sensitivity is directly proportional to the applied power supply (V_{DD}) and that the gain bandwidth product of the input opamp can attenuate the SPM signal gain at some input gain configurations.

4.3.2.1 Input Gain Calculation

The input amplifier, with external circuitry, is used to set the sensitivity of the MX641 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 7, the following steps will assist in the determination of the required gain/attenuation.

Step 1 Draw two horizontal lines from the Y-axis (Signal Level) in Figure 7. The upper line represents the required 'Must' decode level. The lower line represents the required 'Must-Not' decode level

Step 2 Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)). The point where the vertical line meets the X-axis indicates the minimum Input Amp gain required for reliable decoding of valid signals

Step 3 Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis. The point where the vertical line meets the X-axis will indicate the maximum allowable Input Amp gain. Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

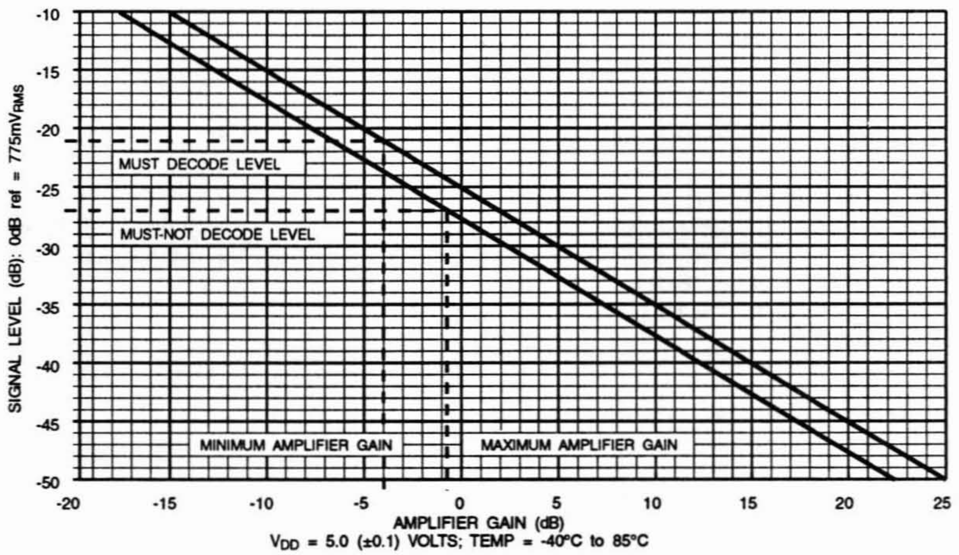


Figure 7: Input Gain Calculation Graph for use in the Fixed Sensitivity Mode

4.3.2.2 Input Gain Components

Refer to the gain components shown in Figure 2. The user should calculate and select external components (R1/R3/C3, R2/R4/C4 and R5/R7/C5, R6/R8/C6) to provide amplifier gains within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits. The graph in Figure 7 is for the calculation of input gain components for an MX641 using a V_{DD} of 5.0 (±0.1) volts.

It is recommended that the designed gain is near the center of the calculated range.

5. Applications

5.1.1 Input Configurations

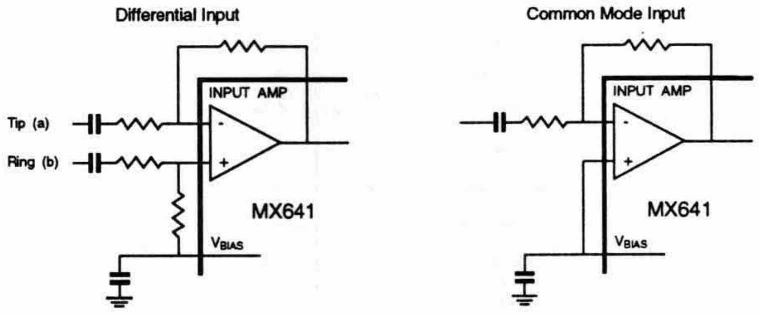


Figure 8: Input Configurations

5.1.2 Protection Against High Voltages

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX641 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX641 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

5.1.3 Aliasing

Due to the sampling nature of switched-capacitor filters used in the MX641, high frequency noise or unwanted signals can alias into the passband, disrupting detection. External components must be chosen carefully to avoid alias effects.

Possible Alias Frequencies:

12kHz Mode = 52kHz

16kHz Mode = 69kHz

If other filtering in the system has not attenuated these alias frequencies, capacitors should be employed across resistors R3, R4, R7 and R8 to provide anti-alias filtering.

The low-pass cutoff frequency should be chosen to be approximately 20kHz to 25kHz for a 12kHz system, or 25kHz to 30kHz for a 16kHz system.

$$\text{i.e.}\quad C = \frac{1}{2 \times \pi \times f_o \times R3}$$

When anti-alias capacitors are used, an allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

6. Performance Specification

6.1 Electrical Specifications

6.1.1 Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}-V_{SS})	-0.3		7.0	V
Voltage on any pin to V_{SS}	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
DW / P Packages				
Total allowable device dissipation at T_{AMB} 25°C			800	mW
Derating above T_{AMB} 25°C			10	mW/°C above T_{AMB} 25°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})	4.5	5.0	5.5	V
Operating Temperature	-40		85	
Xtal/Clock Frequency	3.558918		3.589368	MHz

6.1.3 Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB (ref.) = 775mV$_{RMS}$, Noise Bandwidth = 50kHz
Xtal/Clock Frequency = 3.579545MHz, System Setting = 12kHz or 16kHz

	Notes	Min.	Typ.	Max.	Units
Supply Current			2.0	5.0	mA
Input/Output Parameters					
Clock Out Load	17			15.0	pF
Logic Inputs					
Input Logic '1' (High)		3.5			V
Input Logic '0' (Low)				1.5	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	13	-5.0		5.0	µA
Input Current (V_{IN} = 0)	14	-15.0			µA

		Notes	Min.	Typ.	Max.	Units
Channel Outputs						
Output Logic '1'	I_{OH} = 120mA (Enabled)	1	4.6			V
Output Logic '0'	I_{OL} = 360mA (Enabled)	1			0.4	V
Output Leakage Current	High-Z Output	2	-5.0		5.0	µA
Input Amplifier						
D. C. Gain			60.0			dB
Bandwidth (-3dB)				100		Hz
Input Impedance			1.0			MΩ
Overall Performance						
12kHz Detect Bandwidth		3	11.82		12.18	kHz
12kHz Not-detect Frequencies	(Below 12kHz)	3			11.52	kHz
12kHz Not-detect Frequencies	(Above 12kHz)	3	12.48			kHz
16kHz Detect Bandwidth		3	15.76		16.24	
16kHz Upper Decode Band Edge	(Below 16kHz)	3			15.36	kHz
16kHz Lower Decode Band Edge	(Above 16kHz)	3	16.64			kHz
Level Sensitivity						
Controlled Sensitivity Mode		3,4,12,15	2.6	1.6	0.6	dB(ref.)
Preset Sensitivity Mode		3,4,5,16	-25.4	-26.4	-27.4	dB(ref.)
Signal Quality Requirements						
Signal-to-Noise	(Amp Input)	4,8,9,10	22.0	20.0		dB
Signal-to-Voice	(Amp Input)	4,8,9,11	-36.0	-40.0		dB
Signal-to-Voice	(Amp Output)	4,8,10,11	-1.0		-27.0	dB
Channel Outputs	(Ch1 and Ch2) Figure 4					
Mode Change Time		6			500	ns
Tone Follower Mode (Table 3)						
Response and De-Response Time		3, 4, 7			10.0	ms
Packet Mode (Table 3)						
Response and De-Response Time		3, 4, 7	40.0		48.0	ms

Note:

1. Tone Follower or Packet mode enabled; see Table 3
2. Tristate selected; see Table 3.
3. With adherence to Signal-to-Voice and Signal-to Noise specifications.
4. 12kHz and/or 16kHz system.
5. With Input Amp gain setting = 0dB.
6. Time taken to change between any two of the operational modes: Tone Follower, Packet or Tristate, and with a maximum capacitive load of 30pF on an output.
7. The time delay, after a valid serial data load (or after device powerup), before the condition of the outputs can be guaranteed correct.
8. Immunity to false responses and/or de-responses.
9. Common Mode SPM and balanced voice input signal.
10. With SPM and voice signal amplitudes balanced; to avoid false de-responses due to saturation, the peak-to-peak voice + noise level at the output of the Input Amp should be no greater than the dynamic range of the device. For this reason, the signal-to-voice figure at the AMP Output will vary with the sensitivity setting. The lowest signal-to-voice figure occurs at the highest sensitivity setting. (Table 4 27dB)

11. Maximum voice frequencies = 3.4kHz.
12. With the Input Amplifier gain at 0dB and the Bandpass Filter gain set at 0dB (Table 4); subtract 1.0dB from this specification for each extra single dB of Bandpass Filter gain programmed.
    Alternatively, with the input components as recommended in Figure 2, the sensitivity is as defined in Table 4.
13. Logic inputs with no internal pullup; Chip Select, Serial Data, Serial Clock, Output Enable, Output Select and Clock In pins.
14. Logic inputs with an internal pullup; Preset Level and System Select pins.
15. Preset Level = '0', System Select = don't care; Chip Select, Serial Clock and Serial Data inputs active; see Table 3.
16. Preset Level = '1', System Select = input active; Chip Select, Serial Clock and Serial Data inputs inactive; see Table 3
17. Maximum Clock Output Fan out = 4 (including master)

6.2 Timing

Parameter		Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock 'High' Pulse Width	250			ns
t_{PWL}	Serial Clock 'Low' Pulse Width	250			ns
t_{CYC}	Serial Clock Period	600			ns
t_{CSE}	Chip Select 'Low' to Clock 'High' Edge	450			ns
t_{DH}	Data Hold Time	50.0			ns
t_{DS}	Data Setup Time	250			ns

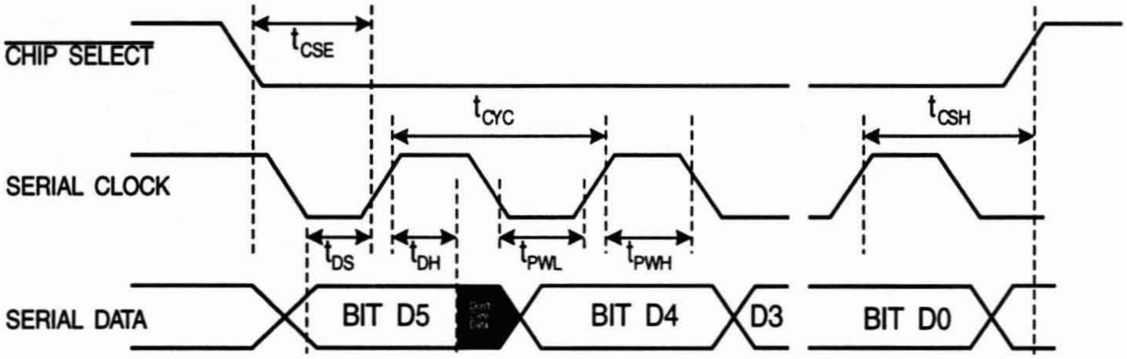
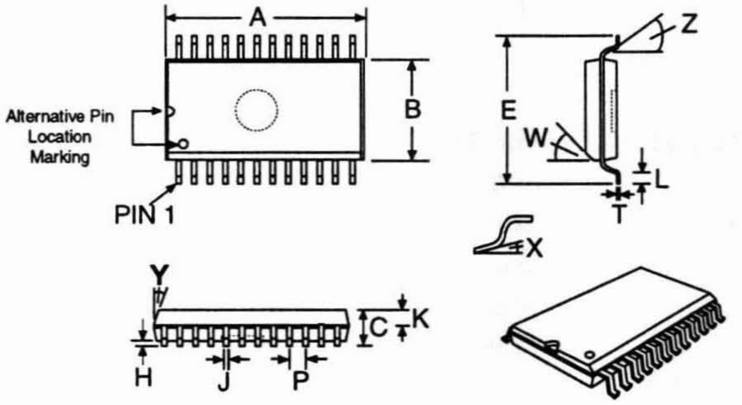


Figure 9: Data Load Timing for the Controlled Sensitivity Mode

6.3 Packages

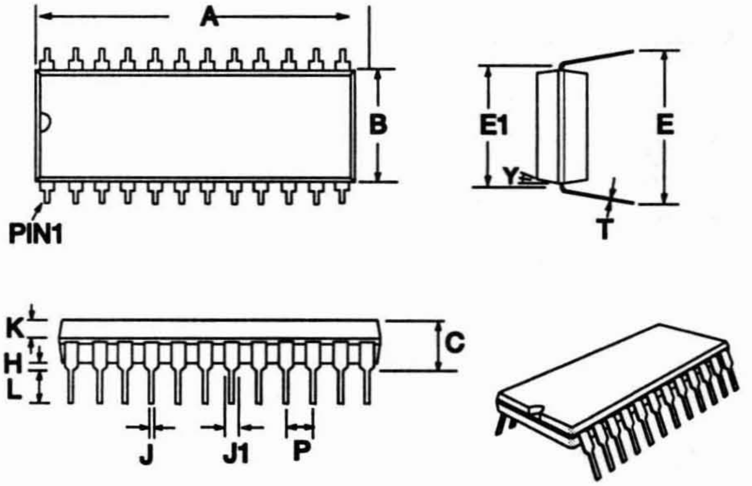


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin SOIC Mechanical Outline: order as part no. MX641DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: order as part no. MX641P

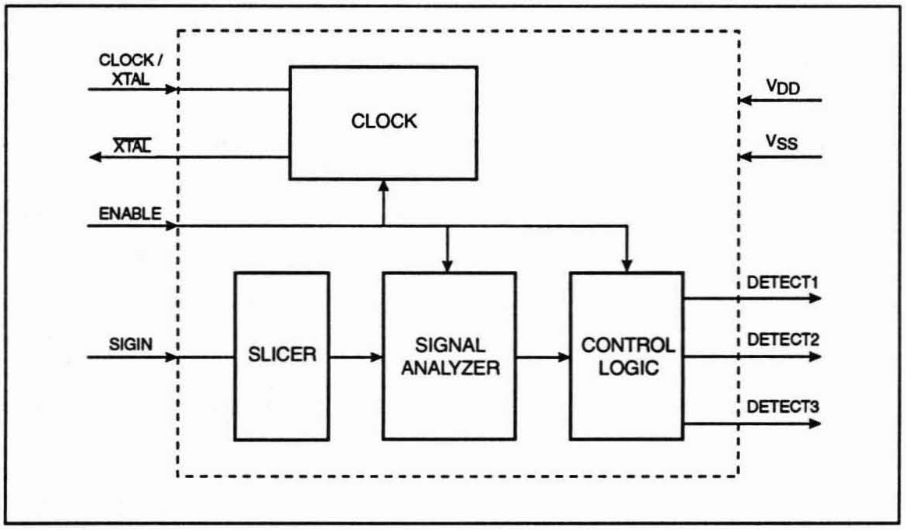
MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX643 Call Progress Tone Detector with Special Information Tones (SIT)

Preliminary Information

- **International Special Information Tone Identification**
- **Worldwide Tone Compatibility**
- **Single and Dual Tone Detected**
- **U.S. Busy-Detect Output**
- **Voice-Detect Output**
- **Wide Dynamic Range > 40dBm**
- **- 40°C to 85°C Operating Temp**
- **Low Supply Current (0.3mA/0.5mA)**
- **Low Supply Voltage (3.3V/5.0V)**
- **Standard 3.58MHz Clock Input**
- **Standard 8-pin DIP Package**



AVAILABLE PACKAGES

MX643P
8-pin PDIP

MX643DW
16-pin SOIC

The MX643 is a low power, low cost device that uses signal processing techniques to detect audible tone signals such as; Dial, Ring, Busy, Unobtainable, and other conditions found when placing a call throughout the world's telecom systems. The detection of these Call Progress stages is essential to the proper operation and application of automatic calling products.

The MX643 offers identification of International Special Information Tones (SIT), reducing the time needed for cadence verification under Obtainable conditions. In addition to the SIT feature, single and dual tone decoding are added for better cross-system Call Progress monitoring. The MX643 offers these features in addition to the same performance levels and features of the MX633 Call Progress Tone Detector such as; detection and identification of U.S. Busy tones, thereby reducing the need to measure the tone cadence to identify U.S. Busy. The decoding and indicating of speech, or other Non-Call Progress signals, thus reducing voice-falsing of Call Progress tones and adding Voice-Answer as a connect prompt.

Available in the industry standard 8-pin DIP, the MX643 is also available in a 16-pin SOIC making it pin compatible with the MX633DW (16-pin SOIC).

MX•COM,INC. MiXed Signal ICs

DATA BULLETIN

MX651

Telephone
Subscriber Pulse Metering & Anti Fraud Tone Processor

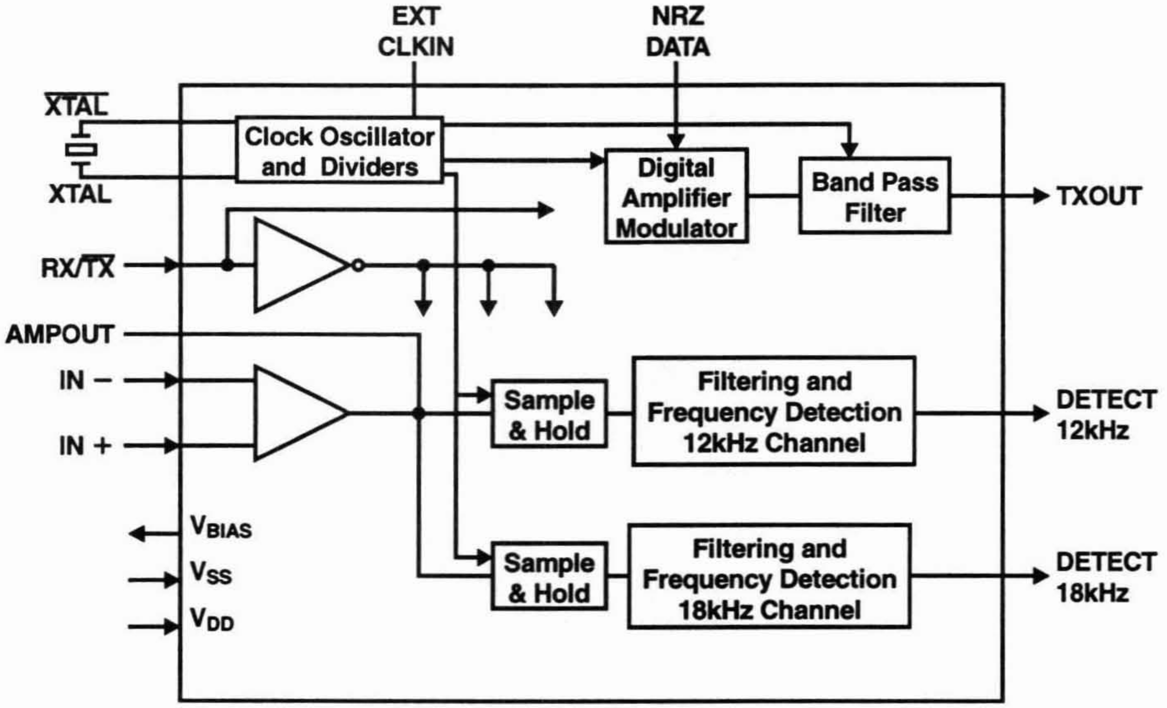
PRELIMINARY INFORMATION

Features

- Rapid 18kHz tone encoder-decoder can transfer NRZ data
  - Tx up to 166bps
  - Rx up to 62bps
- 12kHz Subscriber Pulse Metering Detector

Applications

- Meets European 12kHz SPM Frequency Specifications
- Payphone Applications
- Card Operated Telephone Installations
- Component Adjustable Input Sensitivity
- Low Power 3.3V/5.0V Operation



EXT CLKIN
NRZ DATA
XTAL
XTAL
Clock Oscillator and Dividers
Digital Amplifier Modulator
Band Pass Filter
TXOUT
RX/TX
AMPOUT
IN −
IN +
Sample & Hold
Filtering and Frequency Detection 12kHz Channel
DETECT 12kHz
VBIAS
VSS
VDD
Sample & Hold
Filtering and Frequency Detection 18kHz Channel
DETECT 18kHz

The MX651 is a low power integrated circuit which combines 12kHz Subscriber Pulse Metering (SPM) detection with 18kHz tone processing for anti-fraud purposes within a telephone system. Suitable for battery or line powered systems, the MX651 is protected from crosstalk and false decoding by employing high accuracy switched capacitor filters. By using simple logic or µProcessor control the MX651 will:

- Decode 12kHz SPM pulses (in the presence of high level voice and 18kHz signaling) and provide a logic output.
- Transmit an NRZ amplitude modulated 18kHz security tone to line.
- Decode an incoming modulated 18kHz security tone (in the presence of high level voice and 12 kHz SPM tones) and provide a logic output.

The MX651 is available in a 16-pin SOIC (MX651DW) and a 16-pin PDIP (MX651P) package.

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

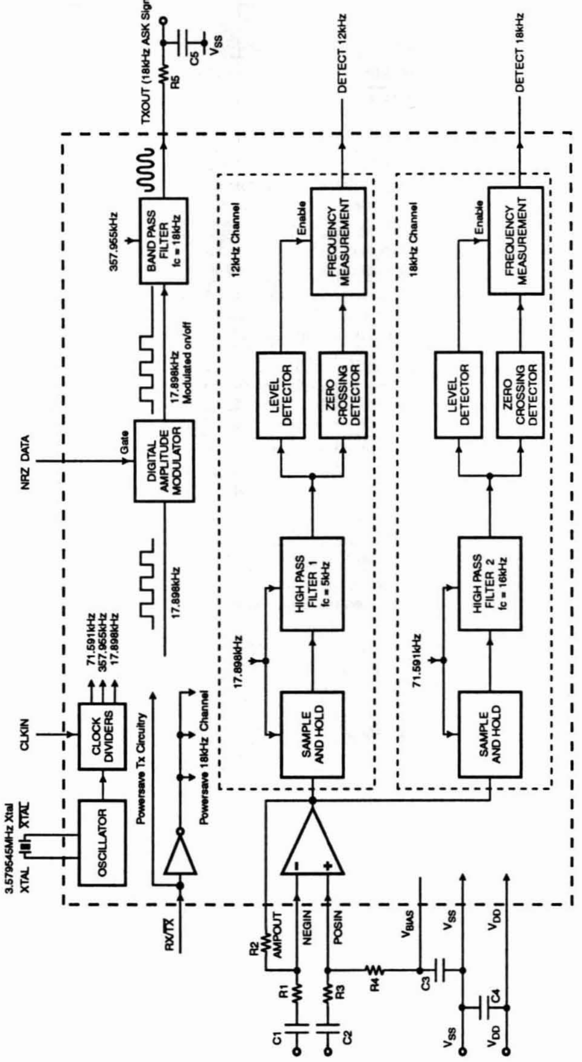
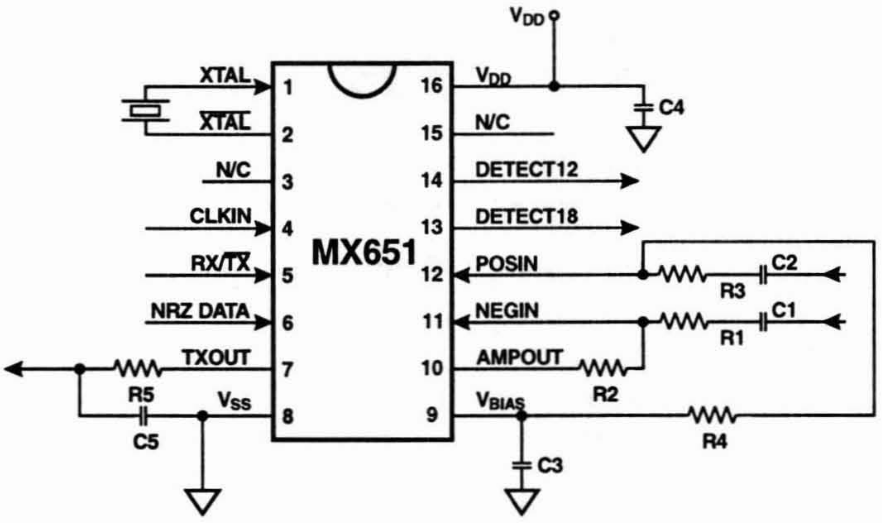

3.579545MHz Xtal
XTAL
XTAL
CLKIN
NRZ DATA
OSCILLATOR
CLOCK DIVIDERS
71.591kHz
357.955kHz
17.898kHz
Powersave Tx Circuitry
RX/TX
Powersave 18kHz Channel
17.898kHz
Gate
DIGITAL AMPLITUDE MODULATOR
17.898kHz Modulated on/off
357.955kHz
BAND PASS FILTER fc = 18kHz
TXOUT (18kHz ASK Signal)
R5
C5
V_SS
12kHz Channel
17.898kHz
SAMPLE AND HOLD
HIGH PASS FILTER 1 fc = 5kHz
LEVEL DETECTOR
ZERO CROSSING DETECTOR
Enable
FREQUENCY MEASUREMENT
DETECT 12kHz
18kHz Channel
71.591kHz
SAMPLE AND HOLD
HIGH PASS FILTER 2 fc = 16kHz
LEVEL DETECTOR
ZERO CROSSING DETECTOR
Enable
FREQUENCY MEASUREMENT
DETECT 18kHz
C1
R1
R2
AMPOUT
NEGIN
C2
R3
POSIN
R4
V_BIAS
C3
V_SS
V_SS
V_DD
C4
V_DD

Figure 1: Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	XTAL	input	Input to the on-chip oscillator inverter.
2	$\overline{\text{XTAL}}$	output	Inverted output of the on-chip oscillator.
4	CLKIN	input	A logic input which may be used when an external clock signal is available in place of a crystal. The external 3.579545MHz signal is applied to this pin and XTAL is tied to V_{DD}. When not used, this pin should be tied to V_{DD}.
5	RX / $\overline{\text{TX}}$	input	A logic input which controls the operating mode of the device. In Rx, the device detects the presence of 12kHz and 18kHz tones. In Tx, the18kHz detect function is disabled and 18kHz is transmitted from the TXOUT pin modulated ON -OFF by the NRZ Data pin.
6	NRZ DATA	input	A logic input used in Tx mode to ASK modulate the TXOUT pin. A logic high corresponds to no tone and logic low corresponds to 18kHz.
7	TXOUT	output	The Tx mode output. It is ASK modulated by the NRZ data input pin. It transmits 18kHz or no tone depending upon the state of the NRZ data input pin. This pin goes to a high impedance state when in Rx mode.
8	V_{SS}	power	Negative supply.
9	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$ It also forms the analog ground for the input differential amplifier. This pin must be bypassed by a capacitor mounted close to the device pins (see Figure 1).
10	AMPOUT	output	Output of the input amplifier. External components are used in conjunction with the amplifier to couple the line signal into the device. Both inputs are available to allow a differential configuration because a two wire input is assumed.
11	NEGIN	input	Inverting input to the input amplifier.
12	POSIN	input	Non-inverting input to the input amplifier.
13	DETECT 18kHz	output	Logic output of the 18kHz channel. Logic 0 when a 18kHz tone (within specified frequency and amplitude limits) has been detected for a minimum length of time.
14	DETECT 12kHz	output	Logic output of the 12kHz channel. Logic 0 when a 12kHz tone (within specified frequency and amplitude limits) has been detected for a minimum length of time.
16	V_{DD}	power	Positive Supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor (see Figure 1).
3, 15	N/C		No internal connection: leave open circuit.

3. External Components



VDD
XTAL
1
XTAL
2
N/C
3
CLKIN
4
RX/TX
5
NRZ DATA
6
TXOUT
7
R5
VSS
8
C5
MX651
16
VDD
C4
15
N/C
14
DETECT12
13
DETECT18
12
POSIN
R3
C2
11
NEGIN
R1
C1
10
AMPOUT
R2
9
VBIAS
R4
C3

R1, R3	See Note 1	1.1MΩ @ 3.3V 1.0MΩ @ 5.0V	±1% ±1%
R2, R4	See Note 1	270kΩ @ 3.3V 330kΩ @ 5.0V	±1% ±1%
C1, C2	See Note 1	33pF @ 3.3V 68pF @ 5.0V	±10% ±10%
C3, C4		0.1µF	±20%
R5		51kΩ	±1%
C5		100pF	±10%
XTAL	See Note 2	3.579545MHz	

Figure 2: Recommended External Components

External Components Notes

1. The device sensitivity is proportional to the power supply (V_{DD}) voltage. The input gain must compensate for this and also prevent input circuitry saturation. It is recommended that amplifier components (R1 to R4, C1 and C2) be used to set the gain between -10dB (if V_{DD} is 5.0V) and -13dB (if V_{DD} is 3.3V).
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-to-peak. Tuning fork type crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer

4. General Description

4.1 Overall Function

The MX651 is a dual channel tone detector for use in European, French, and other payphone systems where 12kHz SPM and 18kHz security tones are used.

4.1.1 SPM (12kHz) Detector

The SPM detector channel responds to a low level (50mV) 12kHz tone in the presence of a large security tone (16kHz - 20kHz) and speech.

The device responds after a period of continuous valid tone and so recognizes a valid SPM toneburst (minimum transmission duration, 40 - 50ms).

This function is permanently enabled.

4.1.2 Security Tone (18kHz) Detector (Rx Mode Only)

This demodulates the 18kHz ASK signal in the presence of the SPM signaling.

4.1.3 Security Tone Transmission (Tx Mode Only)

An 18kHz tone modulated ON - OFF by the NRZ data pin. A logic 0 gates the signal ON so that 18kHz is transmitted. A logic 1 gates the signal OFF so that no tone appears at the TXOUT pin.

4.2 Description of Blocks (Reference Figure 1)

4.2.1 Input Amplifier

This Input Amplifier is connected as a differential amplifier and is used to couple the signal into the device. It also attenuates the combined speech, SPM tone and security tone to prevent its output saturating. The signal gain should be -10dB at 5.0V supply and -13dB at 3.3V. (See Figure 2 for recommended component values).

4.2.2 Sample and Hold (12kHz Channel)

This samples the input signal at 17.898kHz and creates images of the incoming frequencies. The 12kHz SPM is translated to 5.898kHz and the security tone is translated to between 978Hz and 1182Hz. This simplifies the subsequent signal processing.

4.2.3 Filtering and Frequency Detection (12kHz Channel)

The output of the sample and hold circuit is passed to filter HPF1. This is a switched capacitor high pass filter which amplifies the frequency shifted SPM tone (about 5.9kHz) but rejects the frequency shifted security tone (about 1kHz). The filter also rejects any speech signals present. The filter output is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid SPM signal on the line. A valid signal sends the "DETECT 12kHz" pin to logic low.

4.2.4 Sample and Hold (18kHz Channel)

This samples the input signal at 71.592kHz. It is synchronized with the following high pass filter, which is a switched capacitor circuit with the same sampling rate. The sample and hold circuit stores the value of the input waveform value between sampling instants so that it is a suitable input for the filter.

Without the sample and hold circuit, speech or SPM tone components which are large compared with the security tone would interfere with the level discrimination at the filter output.

4.2.5 Filtering and Frequency Detection (18kHz Channel)

The output of the sample and hold circuit is passed to filter HPF2. This is a switched capacitor high pass filter which amplifies the security tone (about 16.92kHz - 19.08kHz) but rejects the SPM tone.

The filter output signal is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid security tone on the line. A valid signal sends the "DETECT 18kHz" pin to logic 0.

4.2.6 Clock Oscillator and Dividers

These circuits generate the internal clocks by division of the oscillator reference frequency. The crystal is connected as shown in Figure 2 without any need for other external components. When a crystal is used, the CLKIN pin should be left open circuit.

Alternatively, when a frequency of 3.579545MHz is externally available, the use of a crystal is unnecessary. The external frequency is applied to the CLKIN pin. In this case, the XTAL pin should be tied to V_{DD}.

In Tx, the dividers also generate a pulse train, frequency 18kHz, which is passed to the Tx circuitry (Gate ON - OFF and Band Pass Filter) for digital modulation and filtering.

4.2.7 (Gate ON-OFF) (Tx Only)

This circuit is a digital block. It performs ON - OFF modulation of the 18kHz pulse train generated from the crystal frequency by the digital dividers. It is controlled by the NRZ DATA pin and is used to encode NRZ data packets as pulsed 18kHz (ASK data). The modulated digital signal is passed to the Tx filter for wave shaping.

4.2.8 Band Pass Filter (Tx Only)

This is a 4th order band pass filter with center frequency 18kHz. It shapes the modulated digital pulse train from the previous block into a low distortion pulsed sinusoidal waveform. The resulting signal is the system acknowledgment security tone. It is transmitted by the subscriber equipment, via the telephone link, to the local exchange.

5. Application

5.1 Device Sensitivity versus V_{DD} - Input Amplifier Gain

The device sensitivity is proportional to V_{DD} because internal voltage references are derived from the power supply. Accordingly, input amplifier signal gain should be adjusted via external components. Figure 2 shows components recommended for 5.0V and 3.3V operation.

5.2 Alias Responses - False Decodes

The MX651 is designed to work in telephone systems where certain ranges of input frequencies are expected and other ranges are not. The 12kHz SPM channel works in the presence of speech and a tone in the range 16kHz - 20kHz. The security tone detector functions in the presence of an interfering tone in the range 11kHz - 13kHz. A significant tone at other frequencies may interfere with correct decoding of valid transmissions and should be avoided.

A small range of input frequencies could cause false decoding when no valid tone has been received. This is because of the frequency shifting property of the SPM channel and the sampled data filters in both channels.

The tone detectors in both the 12kHz and 18kHz channels will respond to 'other than normal' tones. Accordingly, such tones should be avoided.

5.2.1 12kHz Channel

The 12kHz tone detector response frequencies are described by the following two equations:

$$f_{12kHz\ plus} = [(n \times 17.898kHz) + 5.893kHz] \pm 0.185kHz$$

$$f_{12kHz\ minus} = [(n \times 17.898kHz) - 5.893kHz] \pm 0.185kHz$$

n	nominal plus detect frequency (kHz)	nominal minus detect frequency (kHz)
0	5.893	N/A
1	23.791	12.005
2	41.689	29.903
...	...	...

Note: A valid SPM input, in the range 11.82kHz - 12.18KHz, is met when; n = 1 and the nominal minus sign (-) detect frequency is calculated. The other inputs represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 42ms - 45ms of 5708Hz at 50mV could cause a false decode at the "DETECT 12kHz" pin.

5.2.2 18kHz Channel

The 18kHz tone detector response frequencies are described by the following two equations:

$$f_{18kHz\ plus} = [(n \times 71.591kHz) + 18.0kHz] \pm 1.08kHz$$

$$f_{18kHz\ minus} = [(n \times 71.591kHz) - 18.0kHz] \pm 1.08kHz$$

n	nominal plus detect frequency (kHz)	nominal minus detect frequency (kHz)
0	18	N/A
1	89.591	53.591
2	161.182	125.182
3	232.773	196.773
...	...	...

Note: A valid security tone input is met when, n = 0 and the nominal plus sign (+) detect frequency is calculated. The other inputs represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 5.8ms of 52.511kHz at 40mV could cause a false response at "DETECT18kHz" pin.

6. Performance Specifications

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Correct operation of the device outside these limits is not implied.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / P Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

Operating Limits

For the following conditions unless otherwise specified.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	3.0	5.5	V
Operating Temperature	-40	85	°C
Xtal Frequency	3.579008	3.580082	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, Noise and Distortion Measured in 50kHz Bandwidth
V_{DD} = 3.3V to 5.5V @ T_{AMB} = 25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		2.5	4.0	mA
I_{DD}	2		1.0	2.0	mA
Logic 1 Input Level	1, 3	3.5			V
Logic 0 Input Level	1, 3			1.5	V
Logic 1 Output Level at I_{OH} = -120µA	1	4.6			V
Logic 1 Output Level at I_{OL} = 360µA	1			0.4	V
AC Parameters					
Tx Output					
Tx Output Impedance (Tx mode)	4		1.0	2.5	kΩ
Tx Output Impedance (Rx mode)	4	300	500		kΩ
Output Frequency		17.82		18.18	kHz
Output Distortion	5			2	%
Signal Level	5, 6	3.0	3.4	3.7	V_{P-P}
Signal Level	5, 7	2.0	2.2	2.4	V_{P-P}
Response/De-response Times	8			100	µs
Rise/Fall Times	9			5	ms
Rx Input	10				
Rx Input Impedance		10.0			MΩ
Rx Input Amp Voltage Gain			500		V/V
12kHz (SPM) Channel Performance	11				
With Interfering Speech & Security Tone	12				
Input Signal Level	12			800	mV
Decode Min Signal Level	12			50	mV
No Decode Max Signal Level	12	25			mV
Response Delay	12, 13	40		50	ms
De-response Delay	12, 13	40		50	ms
Detect Bandwidth	12	11.82		12.18	kHz
Not Detect Frequencies (below 12kHz)	12			11.52	kHz
Not Detect Frequencies (above 12kHz)	12	12.48			kHz

	Notes	Min.	Typ.	Max.	Units
18kHz (Security Tone) Channel Performance	14				
With Interfering Speech & SPM Tone	15				
Input Signal Level	15			1.2	V
Decode Min Signal Level	15			40	mV
No Decode Max Signal Level	15	10			mV
Response/De-response Times	15, 16			8	ms
Detect Bandwidth	15	16.92		19.08	kHz
Not Detect Frequencies (below 18kHz)	15			16.25	kHz
Not Detect Frequencies (above 18kHz)	15	19.75			kHz

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
2. At V_{DD} = 3.3V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
3. CLKIN input signal may be sinusoidal.
4. Small signal impedance.
5. At output of smoothing network.
6. V_{DD} = 5.0V.
7. V_{DD} = 3.3V.
8. The time between a logic 1 - 0 transition at NRZ data input and the tone amplitude at TXOUT reaching 10% of its full value or between a 0 - 1 transition at NRZ data input and the tone amplitude falling to 90% of its full value.
9. The time for the 18kHz tone amplitude at TXOUT to rise from 10% to 90% or to fall from 90% to 10% of its full value.
10. Input amplifier signal gain set to -10dB for V_{DD} = 5.0V, -13dB for V_{DD} = 3.3V.
11. Maximum 10% distortion for incoming SPM tone, not including interfering speech or security tone (16kHz - 20kHz). Minimum SNR 22dB for incoming SPM tone before the input capacitor.
12. Signal levels at the amplifier input, i.e. before the input capacitor. 12kHz channel performance specified in the presence of the following interfering signals:
    - (a) A 1.2V continuous tone in the frequency range 16kHz - 20kHz
    - (b) An ordinary speech signal containing frequencies in the range 300Hz - 3400Hz of maximum instantaneous amplitude $8.0V_{P-P}$
13. The device responds after 40-50ms of continuous valid tone and de-responds after: a 40-50ms period of no-tone, tones less than 25mV or an out of band tone.
14. Maximum 10% distortion for incoming security tone, not including interfering SPM tone (11kHz - 13kHz). Minimum 20dB SNR for incoming security tone.
15. Signal level specified at the amplifier input, i.e. before the input capacitor. Performance specified in the presence of an interfering 800mV continuous tone in the frequency range 11kHz - 13kHz.
16. The device responds after 8ms of continuous valid tone and de-responds after any of: an 8ms period of no-tone, tone of 10mV or less, or an out of band tone.

6.2 System Timing

		Notes	Min	Max	Unit
Rx					
12KHz	Response Delay		40	50	ms
	De-response Delay		40	50	ms
18KHz	Response Time			8	ms
	De-response Time			8	ms
Tx					
	Transmit 0 Time	Note 1, 2		5.1	ms
	Transmit 1 Time	Note 1, 2		5.1	ms

Note:

1. Tx Transmit Times include both Response/De-response Times and Rise/Fall Times.
2. The Tx Transmit 0 and Transmit 1 Time must exceed 5.1ms.

6.2.1 Timing Diagrams

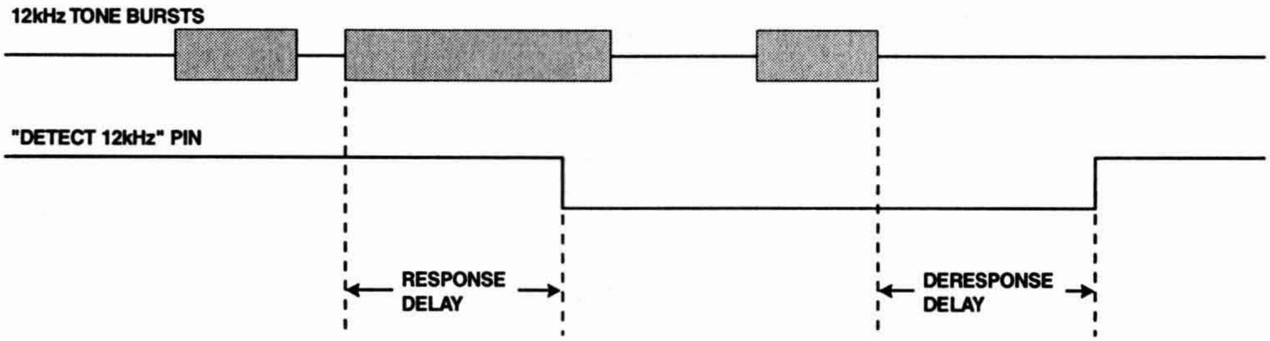

12kHz TONE BURSTS
"DETECT 12kHz" PIN
RESPONSE DELAY
DERESPONSE DELAY

Figure 3: SPM (12kHz) channel. Toneburst and tonegaps < the response and de-response delays are ignored

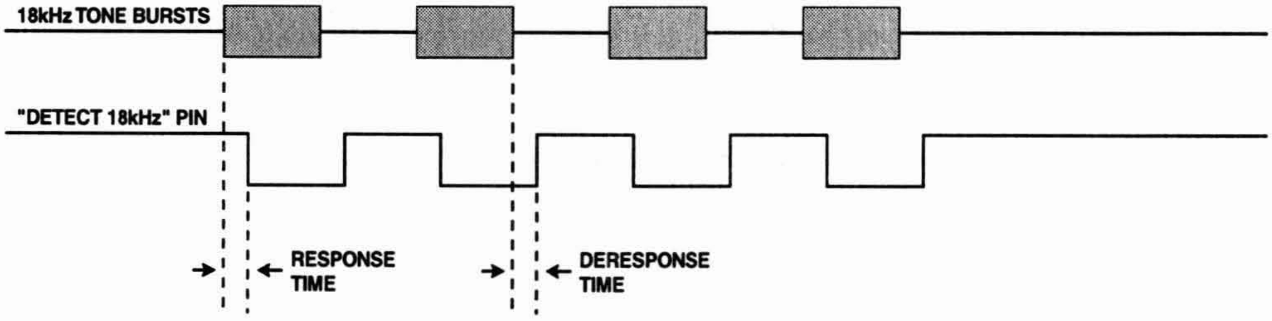

18kHz TONE BURSTS
"DETECT 18kHz" PIN
RESPONSE TIME
DERESPONSE TIME

Figure 4: Security tone (18kHz) channel. The response and de-response times are short to enable the device to recognize short ON-OFF bursts (20ms each)

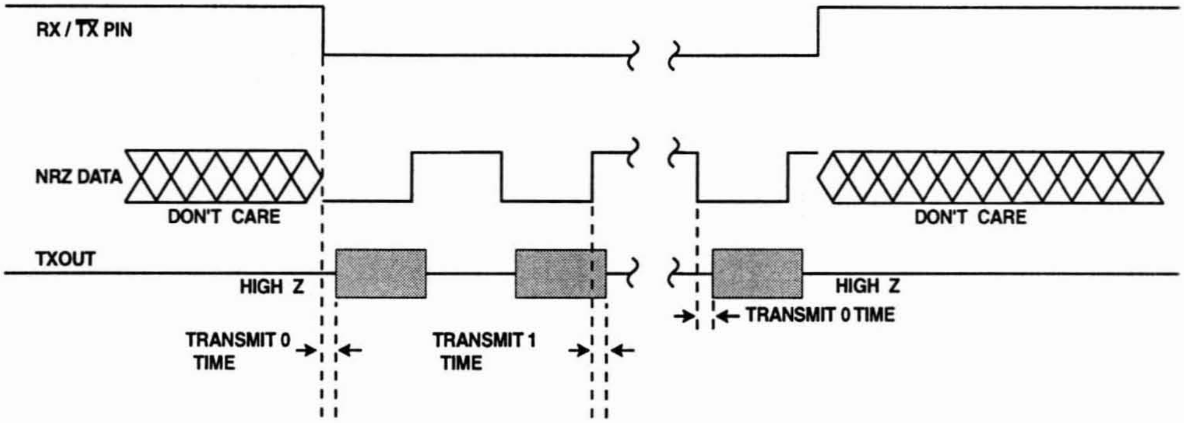
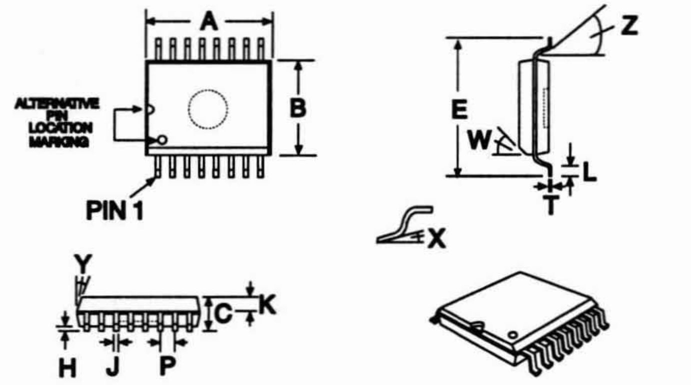

RX / $\overline{\text{TX}}$ PIN
NRZ DATA
DON'T CARE
DON'T CARE
TXOUT
HIGH Z
HIGH Z
TRANSMIT 0 TIME
TRANSMIT 1 TIME
TRANSMIT 0 TIME

Figure 5: Transmit Mode. TXOUT is modulated by the NRZ DATA pin. An 18kHz toneburst represents logic 0 and "no tone" represents logic 1. Data packets with symbol periods ≥ 6ms can be transmitted.

6.3 Packaging

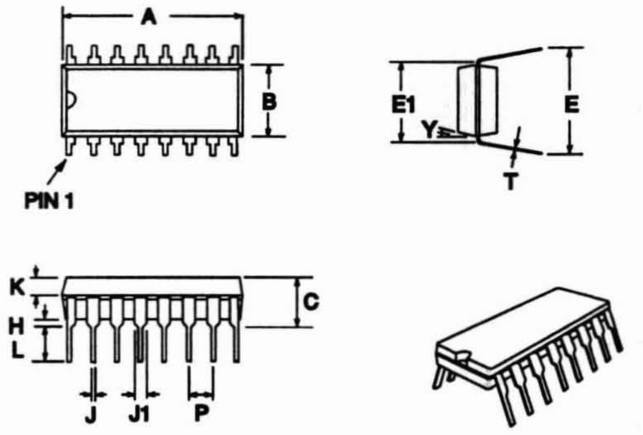

A
B
ALTERNATIVE PIN LOCATION MARKING
PIN 1
E
W
Z
L
T
X
Y
C
K
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: SOIC Mechanical Outline: ***Order as part no. MX651DW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: PDIP Mechanical Outline: ***Order as part no. MX651P***

MX•COM,INC. MiXed Signal ICs

DATA BULLETIN

MX663 Call Progress Decoder

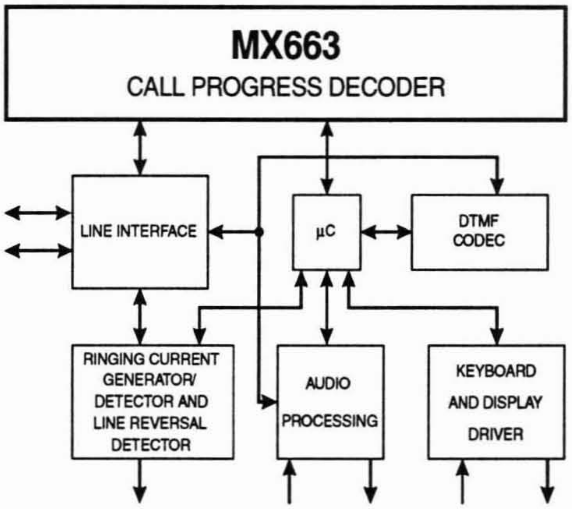
PRELIMINARY INFORMATION

Features

- **Worldwide Call Progress Tone Decoding:**
  Single and Dual Tones
  Fax and Modem
  Answer/Originate Tones
  SIT (Special Information Tones)
  Fast 'US Busy' Tone Detector
- **Adjustable Detection Threshold**
- **Voice Detector**
- **Low Power 3.3V/5.0V Operation**

Applications

- **Call Progress Monitoring**
  Automatic Call Placement
- **Machine Dialing**
- **Fax Tone Detection for Line Switching**



MX663
CALL PROGRESS DECODER
LINE INTERFACE
µC
DTMF CODEC
RINGING CURRENT GENERATOR/ DETECTOR AND LINE REVERSAL DETECTOR
AUDIO PROCESSING
KEYBOARD AND DISPLAY DRIVER

The MX663 decodes the standard audible tone signals provided by telecom systems worldwide to indicate Dial, Ringing, Busy, Unobtainable and other stages of a call attempt. It provides the key features needed for intelligent, full-function, call progress monitoring by applications involving machine dialing or automatic call placement. The MX663 also incorporates the following features:

- Single and dual tone decoding for better cross-system Call Progress monitoring.
- "US Busy" tone detector, saving time needed for "cadence verification" under Busy and Unobtainable conditions. This incorporates a separate 620Hz detector for improved response.
- A detector to indicate speech and non-call progress signals; this reduces voice falsing of call progress tones and adds Voice-Answer detection as a "connected" prompt.
- A fax and modem tone decoder.
- A separate, adjustable threshold, signal-level detector which reduces noise falsing.

The MX663 uses digital signal processing techniques to provide these advantages. It is a low cost, low power product with superior performance. The MX663 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 16-pin SOIC (MX663DW) or 16-pin PDIP (MX663P).

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MX COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

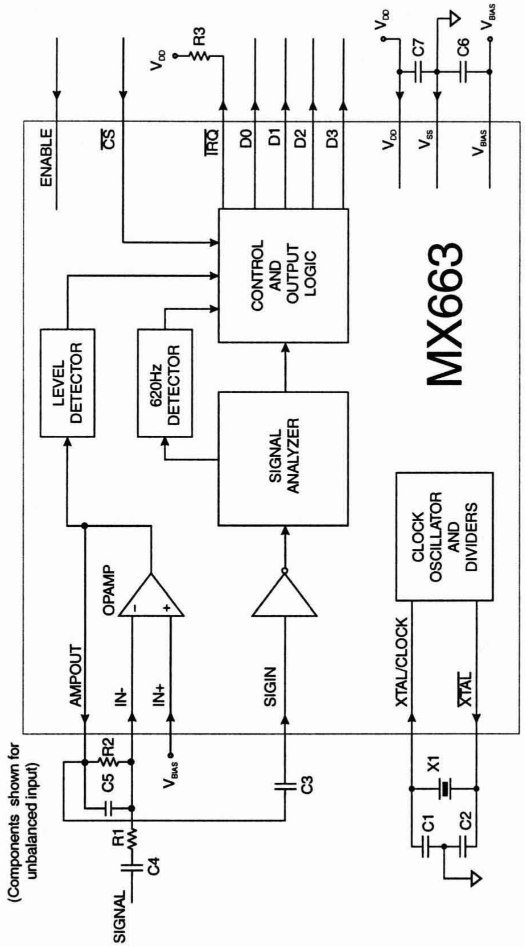

(Components shown for unbalanced input)
SIGNAL
C4
R1
C5
R2
AMPOUT
IN-
IN+
V_{BIAS}
OPAMP
LEVEL DETECTOR
620Hz DETECTOR
SIGIN
C3
SIGNAL ANALYZER
CONTROL AND OUTPUT LOGIC
ENABLE
$\overline{CS}$
V_{DD}
R3
$\overline{IRQ}$
D0
D1
D2
D3
V_{DD}
C7
V_{SS}
C6
V_{BIAS}
V_{DD}
V_{BIAS}
MX663
XTAL/CLOCK
$\overline{XTAL}$
CLOCK OSCILLATOR AND DIVIDERS
C1
C2
X1

Figure 1: Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{XTAL}$	output	Inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
3 4 5 6	D3 D2 D1 D0	output	D3, D2, D1 and D0 is a 4-bit parallel data word output to the µC. The transmission of data is under the control of the $\overline{CS}$ input. These 3-state outputs are held at high impedance when $\overline{CS}$ is at "1". See Figure 8 If $\overline{CS}$ is permanently at "0", D3, D2, D1 and D0 are permanently active. See Figure 4 and Figure 7.
7	$\overline{CS}$	input	The chip select pin activates the Data Bus "D0: 3" when held low. A µC can provide this input to allow the MX663 to reside on a shared Data Bus. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Figure 8
8	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. If $\overline{CS}$ is permanently at "0", the interrupt condition is a logic "0" pulse. See Figure 4 and Figure 7.
9	ENABLE	input	A low level input selects the powersave mode, all circuits are reset and disabled. D0 - D3 outputs become high impedance. A high level input enables all circuits.
10	V_{SS}	Power	Negative supply (ground).
11	SIGIN	input	Signal input. The signal to this pin should be ac coupled. The dc bias of this pin is set internally.
12	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in powersave mode, it should be bypassed to V_{SS} by a capacitor mounted close to the device pins. In powersave mode this pin is pulled towards V_{SS}.
13	IN+	input	Non-inverting input to the on-chip amplifier.
14	IN-	input	Inverting input to the on-chip amplifier.
15	AMPOUT	output	Output of the on-chip amplifier, this is internally connected to the input of the Level Detector.
16	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

Table 1: Signal List

3. External Components

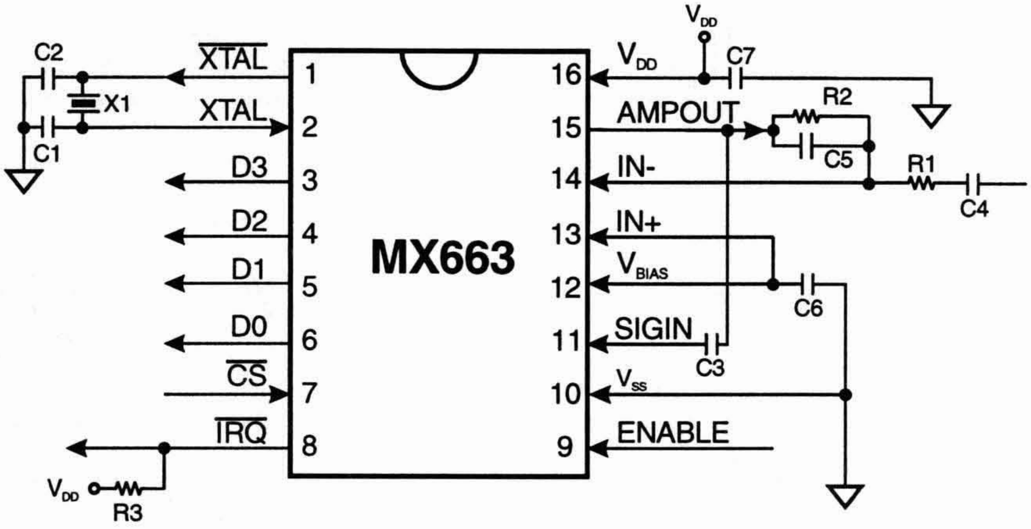

VDD
C2
C7
XTAL
1
16
VDD
X1
XTAL
2
15
AMPOUT
R2
C1
C5
D3
3
14
IN-
R1
C4
D2
4
13
IN+
MX663
D1
5
12
VBIAS
C6
D0
6
11
SIGIN
C3
CS
7
10
VSS
IRQ
8
9
ENABLE
VDD
R3

Figure 2: Recommended External Components

R1	Note 3	100kΩ	±10%
R2	Note 3	510kΩ	±10%
R3		20kΩ	±10%
C1		33pF	±20%
C2		33pF	±20%
C3		0.1µF	±20%

C4	Note 3	0.1µF	±20%
C5	Note 3	100pF	±20%
C6		0.1µF	±20%
C7		1µF	±20%
X1	Note 1, 2	3.579545MHz	±100ppm

Table 2: Recommended External Components

Notes

1. A standard Color Burst Crystal Frequency is recommended.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. Reference section 4.3.5.

4. General Description

4.1 Overall Function Description

The MX663 consists of a Call Progress Tone Detector, a 620Hz Detector and a Level Detector.

The MX663 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech and noise. False outputs caused by speech are a common feature with these products, and background noise may lead to a stuck "detect" output.

The MX663, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domain, with signal amplitude forming a small part in the decision process. This analysis includes checks on whether the signal has a "profile" which matches international standards for Call Progress tones, or a profile more likely to match that of speech, noise or other non-call-progress signals. It also adds checks on whether tones which include frequencies corresponding with the "US Busy" signals, Special Information Tones and Fax/Modem Tones have been detected.

4.2 Glossary

Call Progress Tones: The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signaling.

Call Progress Band: The nominal range 340Hz to 700Hz within which the MX663 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.

620Hz Detection: The nominal range 590Hz to 650Hz. Single tones in this range, or dual tones having a material frequency component within this range (e.g. 480 + 620Hz) will be detected.

Non Call Progress Signal: A signal falling within the nominal range (a) 190Hz to 895Hz, but NOT within the Call Progress Band, or (b) within the nominal range 190Hz to 895Hz, but NOT meeting the DETECTION REQUIREMENTS when the signal falls in the Call Progress Band.

Subject to the duration and other characteristics of such signals, the MX663 will usually interpret these as a Non Call Progress Signal (e.g. speech or other signal activity).

Special Information Tone: The nominal frequencies 950Hz or 1400Hz or 1800Hz.

Fax/Modem Low Tone: The nominal frequency 1250Hz.

Fax/Modem High Tone: The nominal frequency 2150Hz.

Minimum Input Signal: The minimum signal level for the specified tone decoding performance. The lower level at which absence of an input signal will be registered is not specified. However, a separate signal level detector makes amplitude information available.

No Signal: A signal falling outside the nominal range 180Hz to 2280Hz or the absence of an input signal. Either will be detected as a No Signal condition.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

4.3 Block Diagram Description (Reference Figure 1)

4.3.1 SIGIN

The input signal is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at. Accordingly, the input signal should be capacitively coupled to SIGIN.

4.3.2 Call Progress Detector: Signal Analyzer

The analyzer samples the call progress signal at 9.322kHz. An external Anti-Alias Filter can be configured using the on-chip opamp. The frequency range, quality and consistency of the input signal is analyzed by this functional block. To be classified as a call progress signal the input signal frequencies should lie between 340Hz and 700Hz, the signal to noise ratio must be 16dB or greater and the signal must be consistent over a period of at least 145ms. These decode criteria are continuously monitored and the assessment is updated every 7ms. See section 4.3.5.

Because the analyzer time samples the input signal (SIGIN), signals above the operating band (2300Hz) can alias, appear inband, and therefore be detected. Accordingly, applying signals above (2300Hz) should be avoided. Such signals may be inadvertently generated by other sources such as digital clocks, switching power supply, crosstalk, etc.

4.3.3 620Hz Detector

The detector is designed to aid detection of "US Busy" tone. The bandwidth of the 620Hz Detector is 60Hz and the signal must be consistent over a period of at least 145ms for detection to occur. This assessment is updated every 55ms.

4.3.4 Control and Output Logic

This block categorizes the nature of the signal into various decoded output states and controls the four outputs. See the Truth Table in section 4.3.7.

4.3.5 Level Detector and OPAMP

The OPAMP is configured as an amplifier with external components R1, R2, C4 and C5. The level detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold which is defined inside the MX663 as shown in the gain calculations below.

The detector output goes to the Control and Output Logic block. The data output is gated with the level detector's output. The data output is valid only if the level detector output is true. The level detector output can be forced true by connecting IN+ to V_{BIAS} and IN- to V_{SS} through a 100kΩ resistor. An interrupt is produced if the output data changes state.

Gain Calculations:

1. Set gain so an input signal level is amplified above the threshold level of $250mV_{P-P}$.

$$\text{Gain} > \frac{250mV_{P-P}}{V_{IN}}$$

where V_{IN} is the input signal level at C4 in mV_{P-P}.

In simplified form to assist with component value selection:

1. DC Gain = -R2/R1
2. C5 and R2 form a low-pass filter to attenuate out of band signals applied to SIGIN. The low pass filter's band edge is determined by the following: The recommended R2 and C5's component values are selected so than f(-3dB) = 3120Hz .

$$f(-3dB) = \frac{1}{2 \cdot \pi \cdot R2 \cdot C5}$$

3. C4 is a DC blocking capacitor, large enough to avoid affecting the AC gain in the frequency band of interest.
4. The following formula defines the ac gain as a function of frequency, R1, R2 and C5 component values.

   AC gain, Av(f)

$$|Av(f)| = \frac{R1}{R2 \cdot \sqrt{1 + (2 \cdot \pi \cdot f \cdot R2 \cdot C5)^2}}$$

4.3.6 Xtal/Clock Oscillator

If the on-chip Xtal oscillator is to be used, then external components X1, C1 and C2 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the $\overline{\text{XTAL}}$ pin should be left unconnected.

4.3.7 Decode Output Truth Table

D3	D2	D1	D0	Conditions
0	0	0	0	No Signal
0	0	0	1	Call Progress Dual Tones: Will detect 350+440, 400+450, 440+480 Hz tones
0	0	1	0	Non Call Progress Signal, e.g. Voice Activity
0	0	1	1	Call Progress Dual Tone including 620Hz Detection: Will detect 480+620 Hz tones
0	1	0	0	Special Information Tone: Will detect 950, 1400 and 1800 Hz tones
0	1	0	1	Call Progress Single Tone: Will detect 400, 425, 440 and 450 Hz tones
0	1	1	0	Will detect a single tone lying outside the Call Progress Band and within the Non Call Progress signal range
0	1	1	1	Call Progress Single Tone including 620Hz Detection: Will detect 600 and 620 Hz tones
1	0	0	0	Fax/modem High Tone: Will detect 2100 and 2200 Hz tones
1	0	0	1	Reserved for future use
1	0	1	0	Reserved for future use
1	0	1	1	Reserved for future use
1	1	0	0	Fax/modem Low Tone: Will detect 1200 and 1300 Hz tones
1	1	0	1	Reserved for future use
1	1	1	0	Reserved for future use
1	1	1	1	Reserved for future use

Table 3: Decode Truth Table

5. Application

5.1 General

Apply a reset after power-up by taking the ENABLE pin low. This places the device in a powersave mode and resets the internal circuits. It also places the data word output (D0-D3) in a high impedance state, regardless of the level on the $\overline{CS}$ pin.

From this mode the device can be returned to normal operation without any additional settling time, when using the component values recommended in Figure 2. The tone response times remain the same and are given in section 6.1.

An interrupt is produced when the decode state is changed. This interrupt is reset by $\overline{CS}$ going to logic "0". When $\overline{CS}$ is permanently at "0", the interrupt condition is a 5 μs logic "0" pulse on the $\overline{IRQ}$ pin. When $\overline{CS}$ is set to logic "1", the data word output (D0-D3) goes into a high impedance state.

5.2 Signal Category Reference

Signal Category	Sub-Category	Output Code $D_{3:0}$
No Signal		0 0 0 0
Voice and Non-Call Progress Signal		0 X 1 0
	Not Single Tone	0 0 1 0
	Single Tone outside of CP band	0 1 1 0
Call Progress Signal		0 X X 1
	Dual Tone without 620Hz	0 0 0 1
	Dual Tone with 620Hz	0 0 1 1
	Single Tone not 620Hz	0 1 0 1
	Single Tone 620Hz	0 1 1 1
Special Information Tone (SIT Tone)	N/A	0 1 0 0
FAX/MODEM	Low	1 1 0 0
	High	1 0 0 0
Unused Codes	Reserved for future use	1 0 0 1, 1 0 1 0, 1 0 1 1, 1 1 0 1, 1 1 1 0, 1 1 1 1

Table 4: Signal Category

5.3 Typical Response

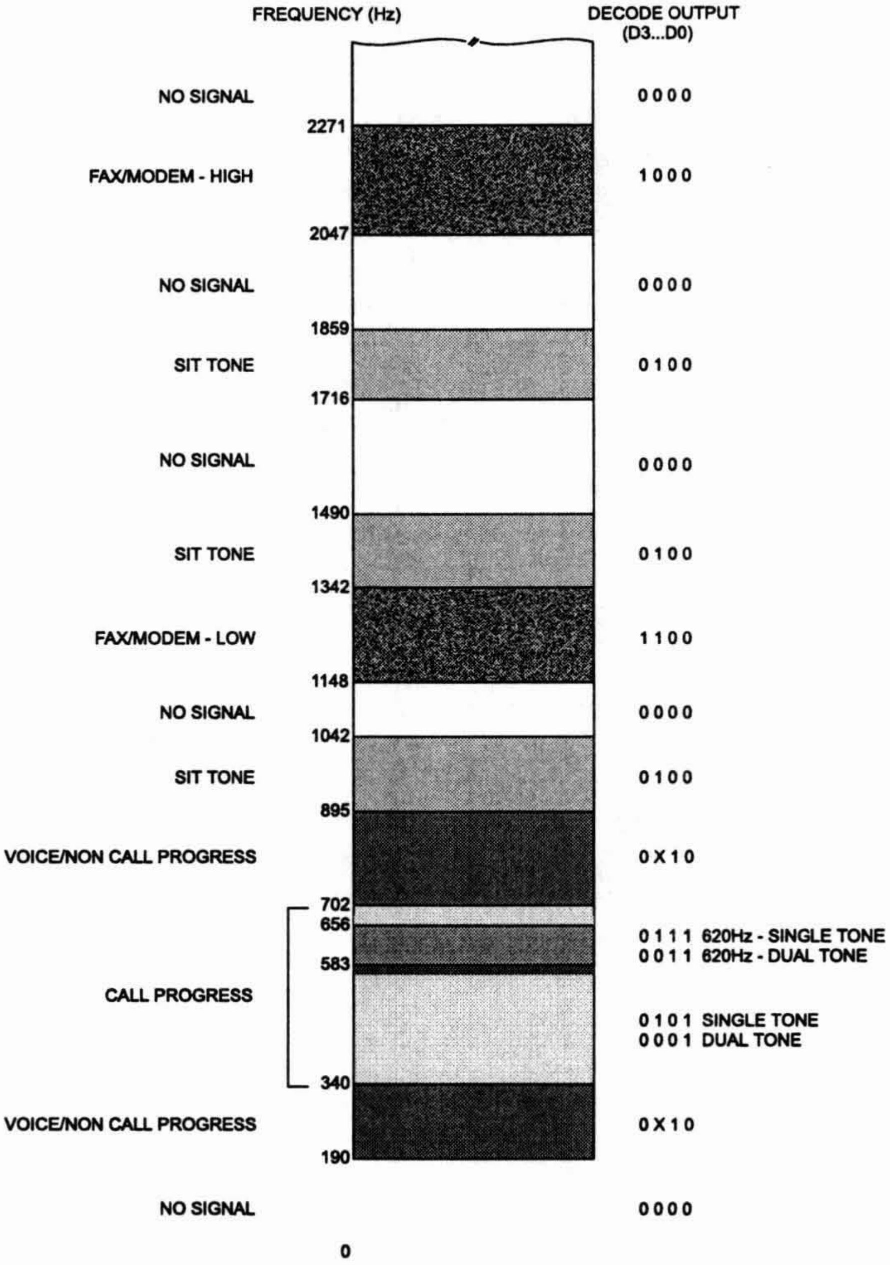


Figure 3: Typical Response Chart

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P / DW Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		3.57	3.59	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz (Color Burst Crystal)
V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C.
0dB = 775 mV_{RMS}, S/N = 20dB, Noise Bandwidth = 5kHz Band Limited Gaussian

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
all powersaved		1, 2		30		μA
V_{DD} = 3.3V		1		0.5	1	mA
V_{DD} = 5.0V		1		1.0	2	mA
Logic Interface						
Input Logic '1'			70%			V_{DD}
Input Logic '0'					30%	V_{DD}
Input Leakage Current	Logic '1' or '0'		-1.0		1.0	μA
Input Capacitance					7.5	pF
Output Logic '1'	I_{OH} = 120μA		90%			V_{DD}
Output Logic '0'	I_{OL} = 360μA				10%	V_{DD}
'Off' State Leakage Current		3			10.0	μA
AC Parameters						
SIGIN Pin						
Input Impedance		4		0.35		MΩ
Minimum Input Signal Level				-40.0		dB
Input Signal Dynamic Range			40.0			dB
Level Detector						
Signal Level Detection Threshold	measured at AMPOUT pin	5		-19.0		dB
OPAMP						
Input Impedance		6	10.0			MΩ
Voltage gain				500		V/V
Xtal/Clock Input						
Pulse Width	'High' or 'Low'	7	40.0			ns
Input Impedance	at 100Hz		10.0			MΩ
Gain	input = 1 mV_{RMS} at 1kHz		20.0			dB

Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. Enable input at V_{SS}, $\overline{CS}$ input at V_{DD}.
3. $\overline{IRQ}$ pin, D0 to D3 pins.
4. Small signal impedance over the frequency range 100Hz to 2300Hz and at 5.0V.
5. Input signal level is multiplied by the voltage gain (-R2/R1). The overall signal at AMPOUT should be larger than 250mV_{P-P}, for V_{DD} = 5.0V. This threshold is proportional to V_{DD}.
6. Open loop, small signal low frequency measurements.
7. Timing for an external input to the XTAL/CLOCK pin.

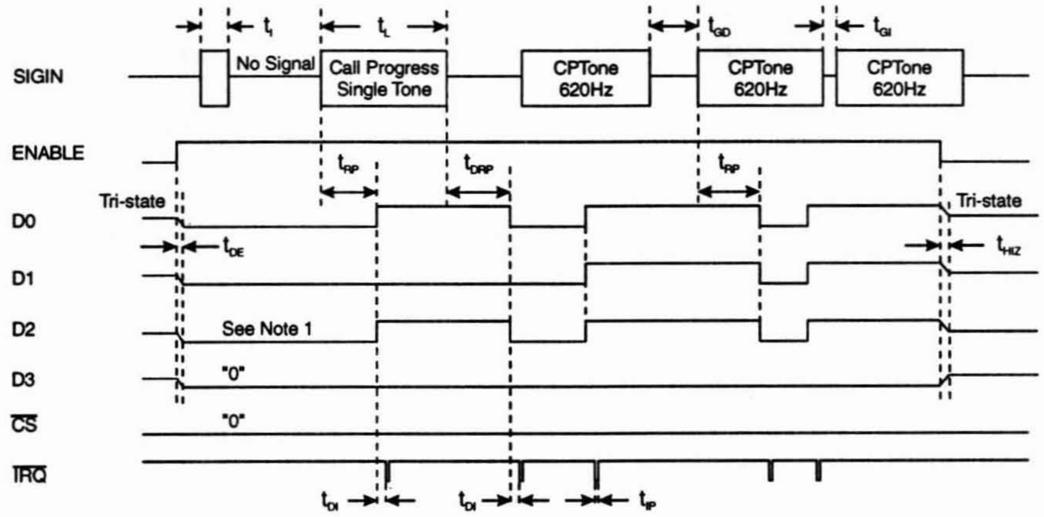
6.2 Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{RP}	Call Progress Tone Response Time	1			145	ms
t_{DRP}	Call Progress Tone De-response Time	1			145	ms
t_{NRP}	Non Call Progress Signal Response Time		145			ms
t_{NDRP}	Non Call Progress Signal De-response Time			80		ms
t_I	Burst Length Ignored	1			70	ms
t_L	Burst Length Detected	1	145			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1, 2, 3,			20	ms
t_{GD}	Call Progress Tone Gap Length Detected	1, 2	40			ms
t_{NG}	Non Call Progress Signal Gap Length Ignored	4		80		ms
t_{DI}	Data available to Interrupt pulse				430	µs
t_{DE}	"$\overline{CS}$ -Low " to Data Valid				0.2	µs
t_{HIZ}	"$\overline{CS}$ -High" to Output Tri-state				1.0	µs
t_{IR}	Interrupt Reset Time				0.2	µs
t_{IP}	Interrupt Low Pulse		4.0	5.0	6.0	µs

Notes:

1. Timing also applies to Special Information Tones and Fax/modem Tones.
2. Only applies to burst of the same frequency.
3. For Special Information Tones and Fax/Modem tones, t_{GI} is 15ms maximum.
4. If the gap > 90ms, a NO Signal state will be detected.

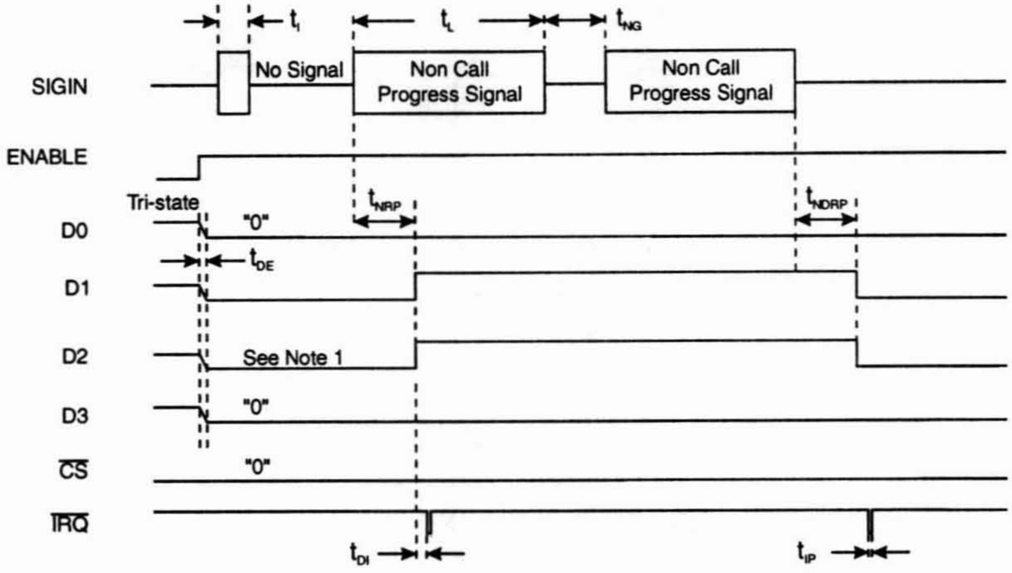


t_I
t_L
t_{GD}
t_{GI}
SIGIN
No Signal
Call Progress Single Tone
CPTone 620Hz
CPTone 620Hz
CPTone 620Hz
ENABLE
t_{RP}
t_{DRP}
t_{RP}
Tri-state
Tri-state
D0
t_{DE}
t_{HIZ}
D1
D2
See Note 1
D3
"0"
$\overline{CS}$
"0"
$\overline{IRQ}$
t_{DI}
t_{DI}
t_{IP}

Note

1. D2 is '1' only when the Call Progress signal, or a Non Call Progress signal, is a single frequency tone.

Figure 4: Timing Diagram: Call Progress Tone(s)


t_I
t_L
t_NG
SIGIN
No Signal
Non Call Progress Signal
Non Call Progress Signal
ENABLE
Tri-state
t_NRP
t_NDRP
D0
"0"
t_DE
D1
D2
See Note 1
D3
"0"
CS
"0"
IRQ
t_DI
t_IP

Note:

1. D2 is '1' only when the Call Progress signal, or a Non Call Progress signal, is a single frequency tone.

Figure 5: Timing Diagram: Non Call Progress Signal

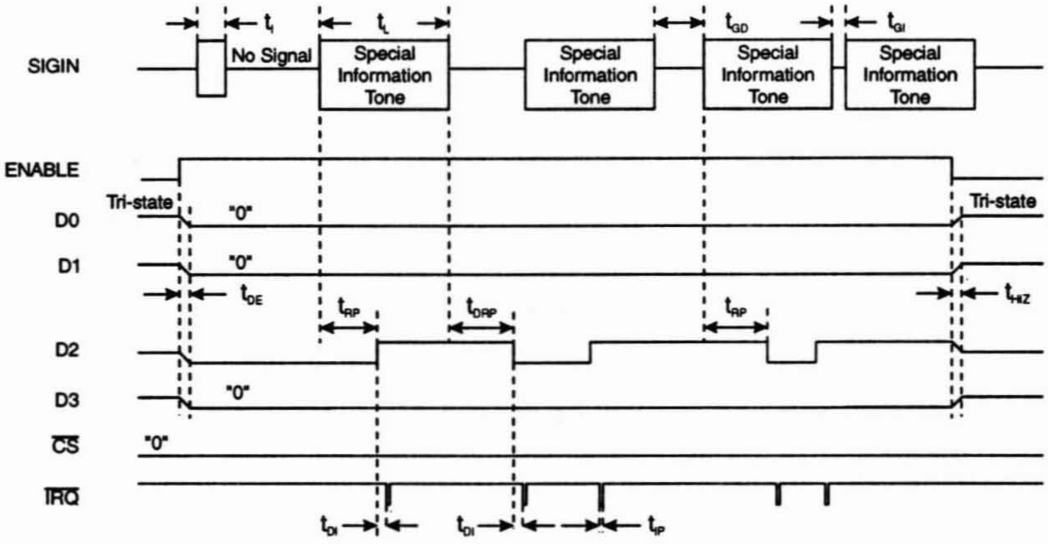

t_I
t_L
t_GD
t_GI
SIGIN
No Signal
Special Information Tone
Special Information Tone
Special Information Tone
Special Information Tone
ENABLE
Tri-state
Tri-state
D0
"0"
D1
"0"
t_DE
t_HZ
t_RP
t_DRP
t_RP
D2
D3
"0"
CS
"0"
IRQ
t_DI
t_DI
t_IP

Figure 6: Timing Diagram: Special Information Tones

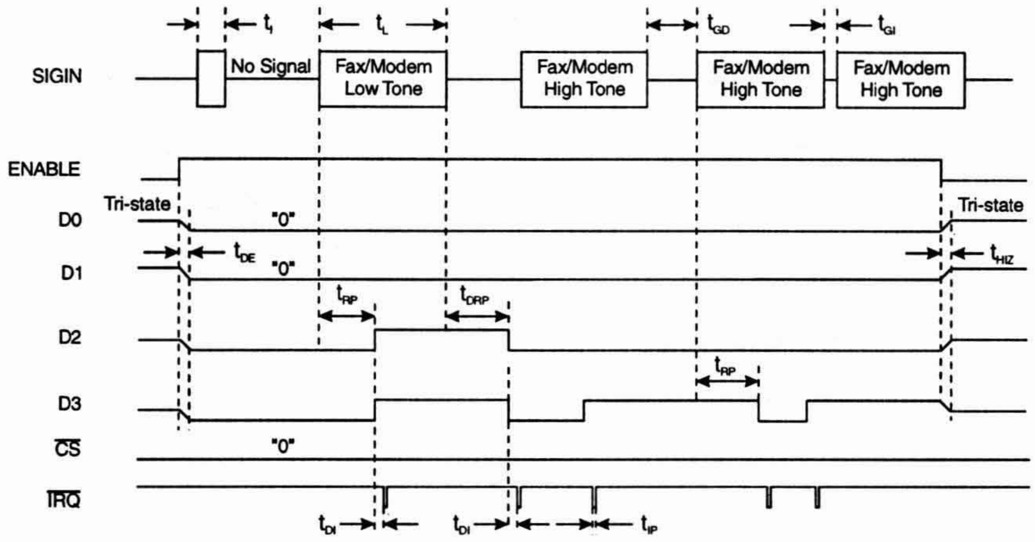

SIGIN
ENABLE
D0
D1
D2
D3
CS
IRQ
Tri-state
"0"
"0"
"0"
No Signal
Fax/Modem Low Tone
Fax/Modem High Tone
Fax/Modem High Tone
Fax/Modem High Tone
t_I
t_L
t_GD
t_GI
t_DE
t_HIZ
t_RP
t_DRP
t_RP
t_DI
t_DI
t_IP
Tri-state

Figure 7: Timing Diagram: Fax/Modem Tones

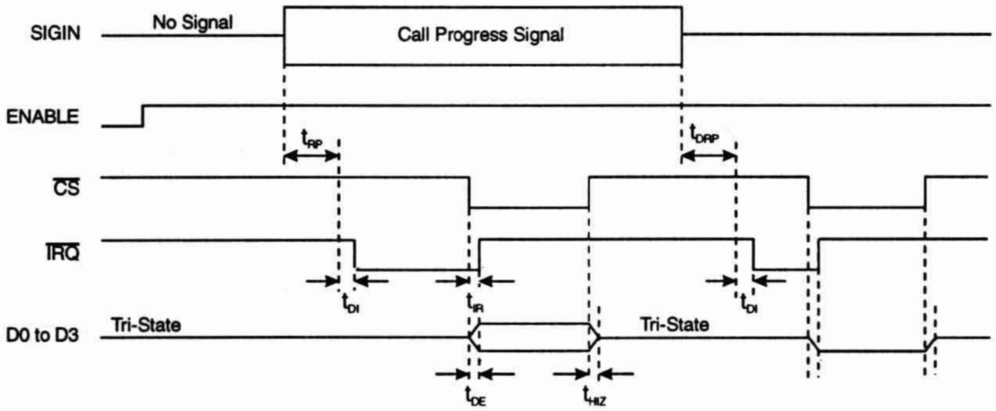
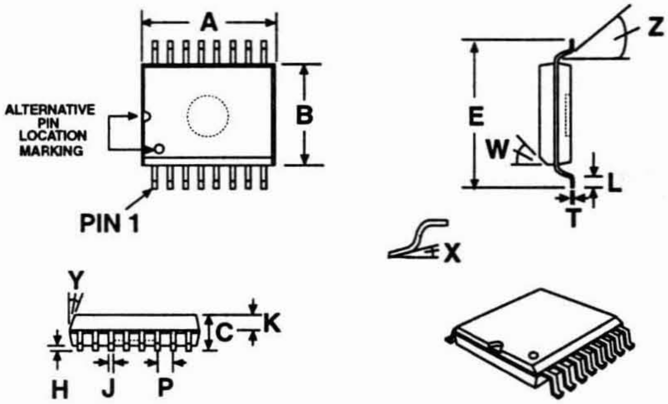

SIGIN
No Signal
Call Progress Signal
ENABLE
t_RP
t_DRP
CS
IRQ
t_DI
t_IR
t_DI
D0 to D3
Tri-State
Tri-State
t_DE
t_HIZ

Figure 8: Bus Timing

6.3 Packaging

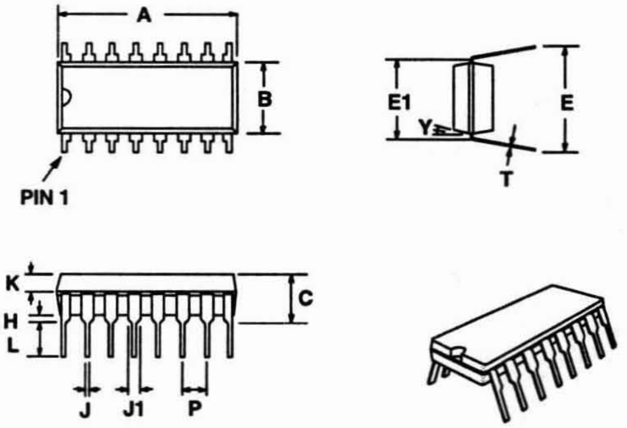


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin SOIC Mechanical Outline: ***Order as part no. MX663DW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin PDIP Mechanical Outline: ***Order as part no. MX663P***

MX•COM,INC. MiXed Signal ICs

DATA BULLETIN

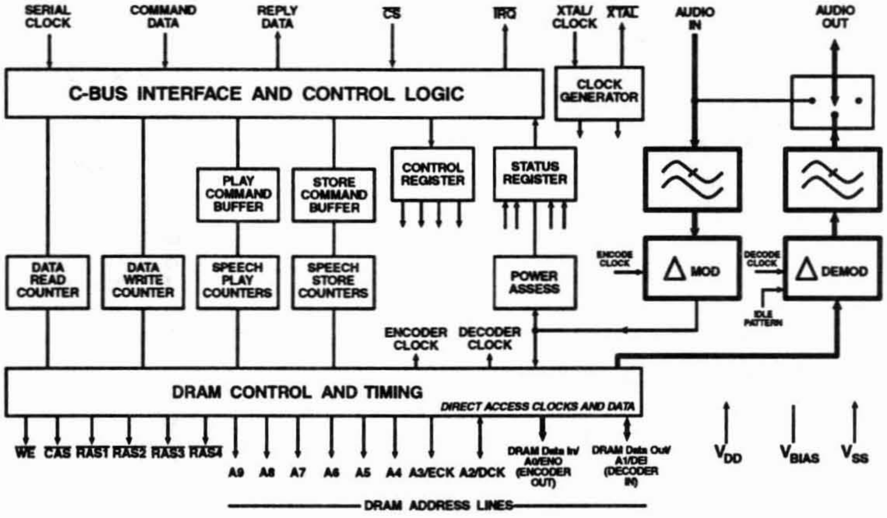
MX802 DVSR CODEC

Features

- **DVSR (Data/Voice Storage and Retrieval) Codec**
- **CVSD Codec Encoder and Decoder**
- **Control and Timing Circuitry for 4Mbits of external DRAM**
- **Low Power Operation**
- **Member of DBS800 Family (C-BUS Compatible)**

Applications

- **Answering Machines where an incoming speech message is stored for later recall**
- **Busy Buffering, in which an outgoing speech message is stored temporarily**
- **Automatic transmission of pre-recorded alarm or status messages.**
- **Time Domain Scrambling of Speech messages**
- **VOX control of transmitter functions**
- **Temporary Data Storage, such as buffering of over-air data transmissions**


SERIAL CLOCK
COMMAND DATA
REPLY DATA
$\overline{\text{CS}}$
$\overline{\text{IRQ}}$
XTAL/ CLOCK
$\overline{\text{XTAL}}$
AUDIO IN
AUDIO OUT
C-BUS INTERFACE AND CONTROL LOGIC
CLOCK GENERATOR
PLAY COMMAND BUFFER
STORE COMMAND BUFFER
CONTROL REGISTER
STATUS REGISTER
DATA READ COUNTER
DATA WRITE COUNTER
SPEECH PLAY COUNTERS
SPEECH STORE COUNTERS
POWER ASSESS
ENCODE CLOCK
Δ MOD
DECODE CLOCK
Δ DEMOD
IDLE PATTERN
ENCODER CLOCK
DECODER CLOCK
DRAM CONTROL AND TIMING
DIRECT ACCESS CLOCKS AND DATA
$\overline{\text{WE}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS1}}$
$\overline{\text{RAS2}}$
$\overline{\text{RAS3}}$
$\overline{\text{RAS4}}$
A9
A8
A7
A6
A5
A4
A3/ECK
A2/DCK
DRAM Data In/ A0/ENO (ENCODER OUT)
DRAM Data Out/ A1/DEI (DECODER IN)
V_{DD}
V_{BIAS}
V_{SS}
DRAM ADDRESS LINES

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder as well as control and timing circuitry for up to 4Mbits of external DRAM. As a member of the DBS800 series, it also contains interface and control logic for the "C-BUS" serial interface.

When used with external DRAM, theMX802 had four primary functions: Speech Storage, Speech layback, Data Storage, and Data Retrieval. The Speech Storage and Playback may be performed concurrently with data storage or retrieval.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control, and refresh signals to interface to external DRAM.

The MX802 may also be used without DRAM (as a "stand alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All signals are controlled by "C-BUS" commands from the system microcontroller.

The MX802 may be used with a 5.0V power supply and is available in the following packages:
24-pin PLCC (MX802LH), 28-pin PLCC (MX802LH8), and 28-pin PDIP (MX802P).

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MXCOM, Inc. reserves the right to change specifications at any time without notice.

1 Block Diagram

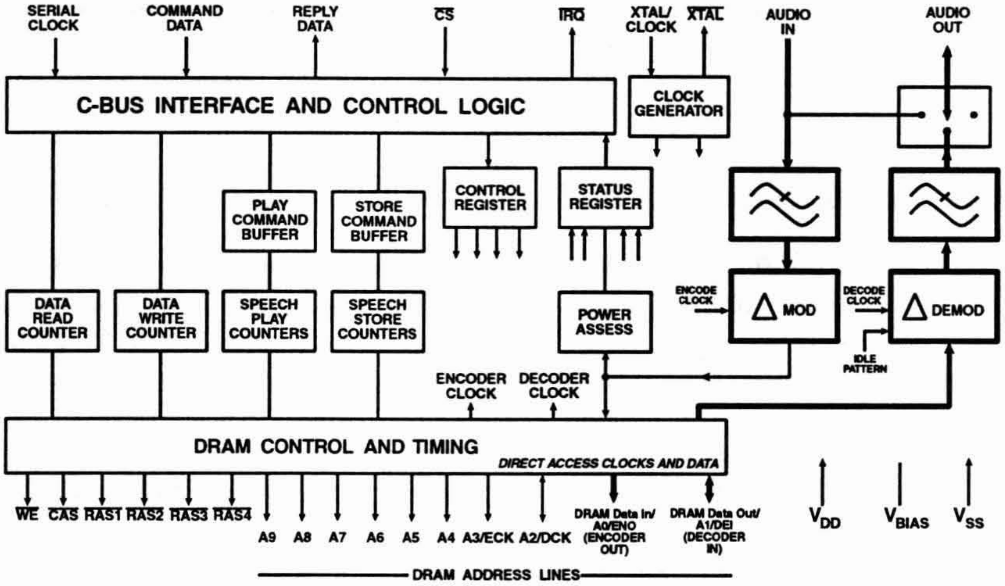

SERIAL CLOCK
COMMAND DATA
REPLY DATA
$\overline{CS}$
$\overline{IRQ}$
XTAL/ CLOCK
$\overline{XTAL}$
AUDIO IN
AUDIO OUT
C-BUS INTERFACE AND CONTROL LOGIC
CLOCK GENERATOR
PLAY COMMAND BUFFER
STORE COMMAND BUFFER
CONTROL REGISTER
STATUS REGISTER
DATA READ COUNTER
DATA WRITE COUNTER
SPEECH PLAY COUNTERS
SPEECH STORE COUNTERS
POWER ASSESS
ENCODE CLOCK
Δ MOD
DECODE CLOCK
Δ DEMOD
IDLE PATTERN
ENCODER CLOCK
DECODER CLOCK
DRAM CONTROL AND TIMING
DIRECT ACCESS CLOCKS AND DATA
$\overline{WE}$
$\overline{CAS}$
$\overline{RAS1}$
$\overline{RAS2}$
$\overline{RAS3}$
$\overline{RAS4}$
A9
A8
A7
A6
A5
A4
A3/ECK
A2/DCK
DRAM Data In/ A0/ENO (ENCODER OUT)
DRAM Data Out/ A1/DEI (DECODER IN)
V_{DD}
V_{BIAS}
V_{SS}
DRAM ADDRESS LINES

Figure 1: Block Diagram

2 Signal List

J/LH8	LH	Signal	Description
1		$\overline{\text{RAS2}}$	$\overline{\text{Row Address Strobe 2}}$ This pin should be connected to the Row Address Strobe input of the second 1Mbit DRAM chip (if used).
2	1	$\overline{\text{RAS1}}$	$\overline{\text{Row Address Strobe 1}}$ This pin should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	$\overline{\text{Write Enable}}$	($\overline{\text{WE}}$) The DRAM of Read/Write control pin.
4		$\overline{\text{Xtal}}$	This is the output of the 4.0MHz on –chip clock oscillator. External components are required at the output when a Xtal is used. A Xtal cannot be used with the 24-pin version.
5	3	Xtal/Clock	This is the input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device. See Table 5 for Sampling Rate Variations.
6	4	$\overline{\text{IRQ}}$	$\overline{\text{Interrupt Request}}$ The output of this pin indicates an interrupt condition to the microcontroller by going to logic'0'. This 'wire-or able' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open drain output. It therefore has a low impedance pulldown to logic '0' when active and a high impedance when inactive. Conditions indicated by this function are Power Reading Ready, Play Command Complete, and Store Command Complete.
7	5	Serial Clock	This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used to transfer timing commands and data to and from the DVSR Codec. See timing diagrams. Clock requirements vary for different MX802 functions.
8	6	Command Data	This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first, and LSB (bit 0) last, synchronized to the Serial clock. See Timing diagrams.
9	7	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$: The C-BUS data transfer control function, this input is provided by the microcontroller. Command Data transfer sequences are initiated, completed, or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
10	8	Reply Data	This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output s held at high impedance when not sending data to the microcontroller. See Timing diagrams.
11	9	V_{BIAS}	This is the output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C1. See Figure 2.
12	10	Audio Out	This is the Analog signal out.
13	11	Audio In	This is the audio (speech) input. The signal to this pin must be AC coupled by capacitor C4 and decoupled to V_{SS} by HF capacitor C6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	V_{SS}	Negative Supply (GND)
15	13	Encoder Out (ENO)	DRAM Data In/A0/Direct Access -- This is connected to the DRAM data input and address line A0. With no DRAM used, this output is available in a Direct Access mode as the Delta Encoder digital data Output. Direct Access control is achieved by Control Register byte 1, bit 7.

J/LH8	LH	Signal	Description
16	14	Decoder In (DEI)	DRAM Data Out/A1/Direct Access --: This is connected to the DRAM data output and address line A1. With no DRAM used, this pin is available in a Direct Access mode as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1, bit 6.
17	15	Decoder Clock (DCK):	DRAM A2/Direct Access -- This is the DRAM address line A2. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Decoder Clock Input. Direct Access control is achieved by Control Register byte 1, bit 6.
18	16	Encoder Clock (ECK)	DRAM A3/Direct Access: This is the DRAM address line A3. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Encoder Clock Output. Direct Access control is achieved by Control Register byte1, bit 6.
19	17	DRAM A4	DRAM address line 4.
20	18	DRAM A5	DRAM address line 5.
21	19	DRAM A6	DRAM address line 6.
22	20	DRAM A7	DRAM address line 7.
23	21	DRAM A8	DRAM address line 8.
24		RAS4	$\overline{\text{Row Address Strobe 4}}$: This pin should be connected to the Row Address Strobe input of the fourth 1Mbit DRAM chip (if used).
25		$\overline{\text{RAS3}}$	$\overline{\text{Row Address Strobe 3}}$: This pin should be connected to the Row Address Strobe input of the third 1Mbit DRAM chip (if used).
26	22	DRAM A9	This is DRAM address line A9. This pin is not connected when a 256kbit DRAM is used. Note: To simplify PCB layout, the DRAM address inputs A0-A8 may be connected in any physical order to the DVSR Codec output pins A0-A8.
27	23	$\overline{\text{CAS}}$	$\overline{\text{Column Address Strobe}}$: This is the DRAM Column Address Strobe pin. It should be connected to the $\overline{\text{CAS}}$ pins of all DRAM chips.
28	24	V_{DD}	Positive supply. A single, stable +5 volt supply is required. Levels and voltages within the DVSR Codec are dependent upon this supply.

Table 1: Signal List

3 External Components

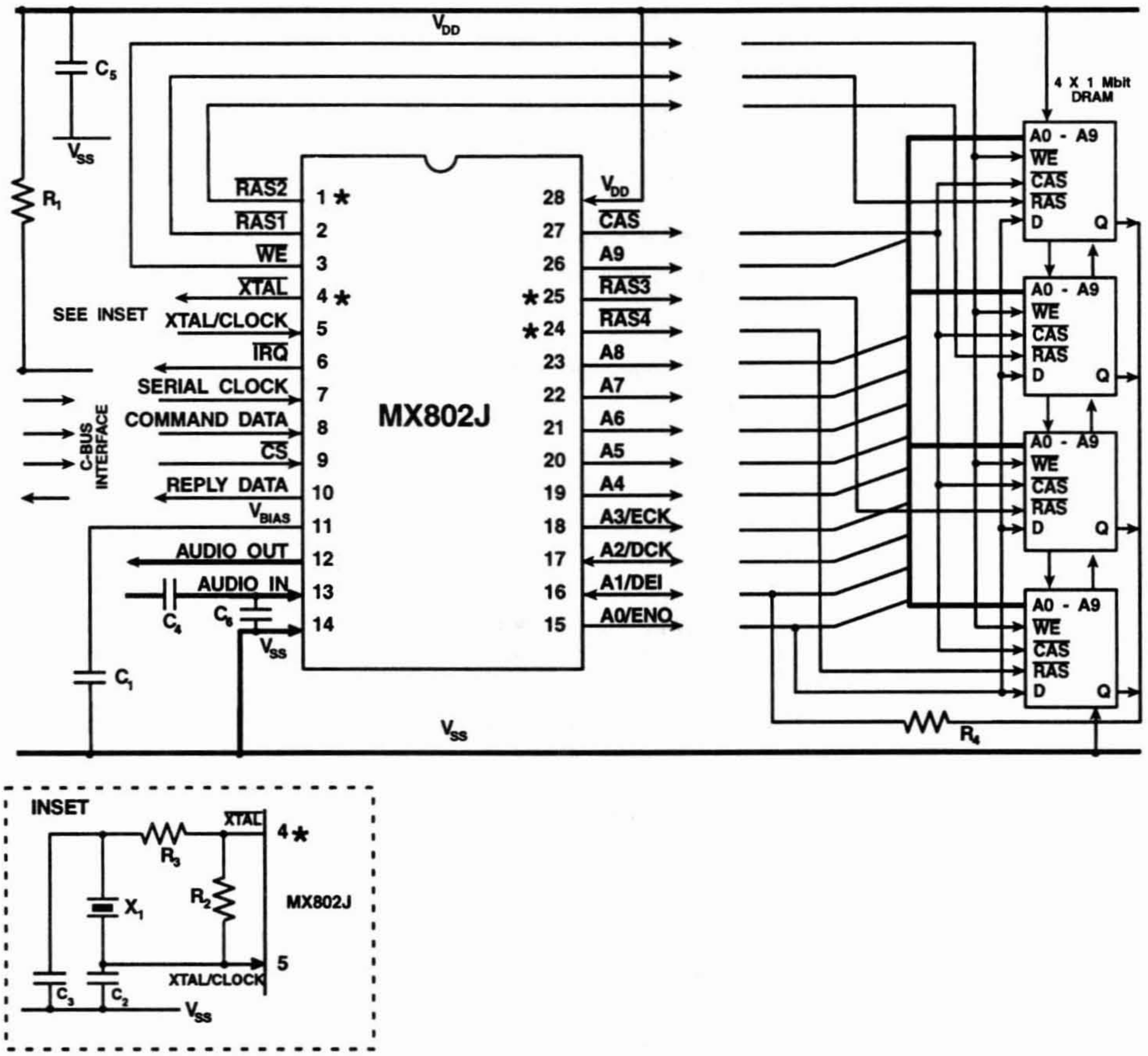

VDD
C5
VSS
R1
4 X 1 Mbit DRAM
RAS2
RAS1
WE
XTAL
SEE INSET
XTAL/CLOCK
IRQ
SERIAL CLOCK
COMMAND DATA
CS
REPLY DATA
VBIAS
AUDIO OUT
AUDIO IN
C4
C6
VSS
C1
C-BUS INTERFACE
MX802J
1 *
2
3
4 *
5
6
7
8
9
10
11
12
13
14
28
27
26
* 25
* 24
23
22
21
20
19
18
17
16
15
VDD
CAS
A9
RAS3
RAS4
A8
A7
A6
A5
A4
A3/ECK
A2/DCK
A1/DEI
A0/ENO
A0 - A9
WE
CAS
RAS
D
Q
R4
VSS
INSET
XTAL
4 *
R3
X1
R2
MX802J
5
XTAL/CLOCK
C3
C2
VSS

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		22.0kΩ	±5%
R2		1.0MΩ	±10%
R3	1		±10%
R4		1.0kΩ	±10%
C1		1.0µF	±10%
C2		33.0pF	±20%
C3		33.0pF	±20%

Component	Notes	Value	Tolerance
C4		1.0µF	±20%
C5		1.0µF	±20%
C6		.001µF	±20%
X1		4.00MHz	
X1		4.032MHz	
X1		4.096MHz	

Table 2: Recommended External Components

Recommended External Component Notes:

1. Xtal circuitry shown in inset is in accordance with the MX-COM Standard and DBS 800 Crystal Application Note.
2. External Xtal circuitry is not applicable to the 24-pin/lead version of this device. Only an externally derived clock input can be used.
3. Functions whose pins are marked with and asterisk (*) in Figure 2 are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.
4. Table 5 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.
5. Resistor R1 is used as the DBS800 system common pull-up for the C-BUS Interrupt Request $\overline{\text{IRQ}}$ line.

   The optimum value will depend on the circuitry connected to the $\overline{\text{IRQ}}$. Up to 8 peripherals may be connected to this line.
6. Recommended DRAM parameters:
   256kbit x 1 or 1Mbit x 1 Dynamic Random Access Memory with "$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$" refresh mode.
   Maximum Row address time = .200us.
   Example DRAM types:
   256kbit (262,144 bits)
     Texas Instruments (TMS4256-20)
     Hitachi (HM51256-15)
   1Mbit (1,048,576 bits)
     Texas Instruments (TMS4C1024-15)
     Hitachi (HM511000-15)
7. Figure 2 shows connections to 4x1 Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0-A8 may be connected in any order to the MX802 DVSR Codec output pins A0-A8. Connections to 256kbit DRAM are similar, but A9 I left unconnected.
8. When using the MX802 "stand alone" 9Direct Access), no DRAM sections should be connected.

4 General Description

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder as well as control and timing circuitry for up to 4Mbits of external DRAM. As a member of the DBS800 series, it also contains interface and control logic for the "C-BUS" serial interface.

When used with external DRAM, theMX802 had four primary functions: Speech Storage, Speech layback, Data Storage, and Data Retrieval. The Speech Storage and Playback may be performed concurrently with data storage or retrieval.

Speech Storage:	Speech signals present at the Audio Input may be digitized by the CVSD encoder. The resulting bit stream is stored in DRAM. This process also provides readings of the speech signal power level. These readings are used by the system microcontroller for pause reduction.
Speech Playback:	Digitized speech may be read from DRAM and converted back into analog from by the CVSD decoder.
Data Storage:	Digital data derived via the C-BUS from the Modem or system data may be stored in DRAM.
Data Playback:	Digital data may be read from DRAM and sent over the C-BUS to the system microcontroller.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control, and refresh signals to interface to external DRAM.

The MX802 may also be used without DRAM (as a "stand alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All signals are controlled by "C-BUS" commands from the system microcontroller.

4.1 Controlling Protocol

Control of the functions of the MX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions of data to and from the system microcontroller (See Figure 4). The use and content of these instructions is detailed in the following pages.

Command Assignment	Address/Command (A/C) byte		Data Bytes
	Hex	Binary	
		MSB LSB	
General Reset	01	00000001	
Write to Control Register	60	01100000	+2 byte instruction to Control Register
Read Status Register	61	01100001	+1 byte reply from Status Register
Store 'N' pages. Start page 'X'	62	01100010	+2 bytes command – Immediate
Store 'N' pages. Start page 'X'	63	01100011	+2 bytes Command – Buffered
Play 'N' pages. Start page 'X'	64	01100100	+2 bytes Command – Immediate
Play 'N' pages. Start page 'X'	65	01100101	+2 bytes Command – Buffered
Write Data. Start page 'P'	66	01100110	+2 bytes 'P' + Write Data
Read Data. Start page 'P'	67	01100111	+2 bytes 'P' + Read Data
Write Data – continue	68	01101000	+Write Data
Read Data -- Continue	69	01101001	+Read Data

Table 3: C-BUS Address/Commands

4.1.1 Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by further instruction/data reply.

Control and configuration is by writing instructions form the microcontroller to the Control Register (60_H). Reporting of MX802 configurations is by reading the Status Register (61_H).

4.1.2 Operation with DRAM

The MX802 can operate with up to 4Mbits of Dynamic Ram (DRAM). When used with DRAM, the MX802 performs four main functions under the control of the commands received over the C-BUS interface from the microcontroller:

Stores Speech	The MX802 stores speech by digitally encoding the analog input signal and writing the resulting digital data into the associated DRAM.
Plays Speech	The MX802 plays back stored speech by reading the digital data stored in the DRAM and decoding it to provide and analog output signal.
Writes Data	The MX802 writes data sent ver the C-BUS from the microcontroller to DRAM.
Reads Data	The MX802 reads data from DRAM, sending it to the microcontroller over the C-BUS.

Data is directed to and from DRAM by the on-chip DRAM Controller.

4.1.3 Speech

The CVSD encoder and decoder sampling rates are independently set via the Control Register (See Table 4, Table 5, and Table 6) to 16, 25, 32, 50, and 64kbps. This allows the user to choose between speech quality and storage time while providing for time compression or expansion of the speech signals.

The DVSR Codec can handle from 256kbits to 4Mbits of DRAM, giving, in the case of the 32kbps sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into 'pages' of 1024 bits each, corresponding to 32ms at 32kbps sampling rate.

A 256 kbit DRAM contains	256 'pages'
A 1 Mbit DRAM contains	1024 'pages'
A 4 Mbit DRAM contains	4096 'pages'

When used without DRAM, the decoder sampling rate (8-64kbps) is determined by an external clock source applied to the Decoder Clock pin.

4.1.3.1 Store and Play Speech Commands

Speech storage and playback may take place simultaneously. These commands are transmitted, via C-BUS, to the MX802 in the following form:

STORE OR PLAY "N" (1024-bit) PAGES (of decoded speech data) STARTING AT PAGE "N".

"N" can be any number between 0 and F (1-16 pages). "X" can be any number from 405 (4Mbit DRAM), as shown below. Preceded by A/C, this command writes 16 bits (byte 1 or byte0) of data from the microcontroller to the Store or Play command Buffer.

MSB				BYTE 1							BYTE2				LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N								X							

4.1.3.2 Speech Store Commands

4.1.3.2.1 62_H STORE "N" PAGES – START PAGE "X" (immediate) 63_H STORE "N" PAGES – START PAGE "X" (buffered)

The digitized speech from the CVSD encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete pages stored since the start of the execution of the command.

As soon as the command has terminated, the following events take place:

1. The Store Command Complete bit in the Status Register (Table 7) is set.
2. An Interrupt Request ($\overline{IRQ}$) is sent, if enabled, to the microcontroller.
3. The next speech storage command (if present) is immediately taken from the Store Command Buffer and execution f the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register:

4.1.3.2.2 61H READ STATUS REGISTER (Table 8)

To provide continuity of speech commands, both Store and Play Commands can be presented to the MX802 in one of two formats: immediate or buffered.

An immediate command will be started on completion of its loading, irrespective of the condition of the current command.

A buffered command will begin after the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps even though the microcontroller may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the status register will be cleared.

4.1.3.3 Speech Playback

Speech playback is controlled by similar commands using the Speech Play counters and Play Command Buffer:

4.1.3.3.1 64_H PLAY "N" PAGES – START PAGE "X" (immediate)
65_H PLAY "N" PAGES – START PAGE "X" (buffered)

As soon as the Play Command had completed, the "Play Command Complete" bit in the Status Register is set, and an Interrupt Request is generated (if enabled).

If no "next" command is waiting in the Play Command Buffer when a speech play command finishes, a continuous idle code (0101…0101) will be fed to the delta decoder.

Speech data is stored or recovered at the selected Encode or Decode sample rate (Table 5). Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play Command received from the microcontroller, or by a General Reset (01_H).

4.1.3.4 Store/Play Speech Synchronization (Table 6)

This capability is provided primarily for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

4.1.3.4.1 No Speech Sync Set:

Store and Play operations may take place completely independently.

4.1.3.4.2 Store after Play:

The next buffered store command will start on completion of a play command, while the next play command sequence (if any) continues normally.

4.1.3.4.3 Play after Store:

The next buffered play command will start on completion of a store command, while the next store command sequence (if any) continues normally.

These actions will continue while Speech Sync bits are set.

4.1.4 Data Handling

For the purpose of storing data sent via C-BUS from the microcontroller, the memory (DRAM) is divided into "data pages" of 64 bits (8 bytes).

A 256kbit DRAM contains 4096 data pages.
A 1Mbit DRAM contains 16384 data pages.
4Mbit DRAM contains 65536 data pages.

In accordance with C-BUS timing specifications, data is handled 8 bits (1 byte) at a time, although any number of 8-bit blocks of data may be written to or read from the DRAM by a single command.

Data transfer is terminated by the Chip Select line going to a logic "1."

4.1.4.1 C-BUS Data Transfer Limitations

For those commands which transfer data over the C-BUS between DRAM and the microcontroller (Write and Read data), the C-BUS serial clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing store and play commands.
250kHz if no speech Store or Play commands are active.

This limitation is due to the rate at which data goes into and out of the DRAM. All other commands and replies (Control, Status, Reset) may use a maximum clock rate of 500kHz. See Figure 4.

4.1.4.2 Read Data

4.1.4.2.1 67_H READ DATA -- START PAGE "P"

This command sets the Data Read Counter to "P," page, and then reads data bytes from successive DRAM locations, sending them to the microcontroller as Reply Data bytes. The Data Read Counter is incremented by 1 for each bit read.

4.1.4.2.2 69_H READ DATA CONTINUE

This command reads data bytes from successive DRAM locations determined by the Data Read Counter, incrementing the counter by 1 for each bit read.

4.1.4.3 Write Data

4.1.4.3.1 66_H WRITE DATA -- START PAGE "P"

This command sets the Data Write Counter to "P" page, and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the C-BUS.

The Start Page, "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data page addresses from 0 to 65535 (4Mbits DRAM).

4.1.4.3.2 68_H WRITE DATA CONTINUE

This command writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the C-BUS.

4.1.4.4 DRAM Speech Capacity

28-pin/lead versions of the MX802 may be used with a single 256kbit DRAM, or with up to 4 x 1Mbit of DRAM. 24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different encode and decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 4 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reversed sequence (see Control Register for details).

DRAM Size	Available bits	Speech Pages	Nominal Sample Rates (kbps)				
			16	25	32	50	64
256kbps	262144	256	16.0	10.0	8.0	5.0	4.0
1024kbps	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbps	2097152	2048	131.0	84.0	65.0	42.0	32.0
3Mbps	3145738	3072	196.0	126.0	98.0	63.0	49.0
4Mbps	4194304	4096	262.0	168.0	131.0	84.0	65.5

Table 4: Sampling Clock Rates vs. Speech Storage/Playback Times

4.1.4.5 Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 5 shows the range of sampling rates available for different Xtal/clock input frequencies and the counter ratios used to produce them. Consideration should be given to the effect of different Xtal/clock frequencies upon the audio frequency performance of the device.

Control Register Byte 0, Bits				Internal Counter Division Ratio	Xtal Clock Frequency (MHz)		
5	4	3	Dec.		4.0	4.032	4.096
2	1	0	Enc.				
0	1	1		256	15.625	15.75	16.0
1	0	0		160	25.0	25.20	25.60
1	0	1		128	31.25	31.50	32.0
1	1	0		80	50.0	50.4	51.20
1	1	1		64	62.50	63.0	64.0

Table 5: Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use, it should be noted that

a. A 4.032MHz Xtal/clock input will produce an accurate 1200-baud rate for the MX809 MSK Modem.

b. A 4.096MHz Xtal/clock input will generate exactly 16kbps, 32kbps and 64kbps Codec sampling clock rates.

4.2 Write to Control Register

4.2.1 General Reset

Upon power-up the bits in the MX802 registers will be random (either 0 or 1). A General Reset Command (01_H) will be required to reset all devices on the C-BUS. It has the following effect on the MX802:

Control Register	Set to 00_H
Status Register	Set to 00_H
Clear Store and Play Command Buffers	

4.2.2 Direct Access

External circuitry is allowed direct access to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the MX802 to be used as a Delta Modulation voice encoder and decoder.

Input audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

Analog output switching remains under the control of the Control Register, but the decoder sampling clock rate (8kbps to 64kbps) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (byte 0, bits 5, 4, 3) should be set to binary 1,1,1, where the required rate approximates to a multiple of 25kbps.

Both the encoder internal sampling clock rate and input switching (Table 7) remain under the control of the Control Register. The encoder internal sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

4.2.3 Play Counter

The Play Counter direction may be set to run backward as well as forward. This can be used in a scrambling system by replaying speech data in reverse order.

4.2.4 DRAM Control

A logic “1” will disable the DRAM Control Timing circuits and associated counters. The C-BUS Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic “1” when the MX802 is used in the Direct Access Mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to logic “1.”

4.2.5 Codec Powersave

A logic “1” puts the Delta Codec and filters into Powersave Mode with V_{BIAS} maintained. The Clock Generator, C-BUS Interface, and DRAM Control and Timing remain active.

4.2.6 Command Interrupt Enable

A logic “1” set at the relevant bit will enable Interrupt Requests to the microcontroller when that command operation is complete.

4.2.7 Store and Play Speech Synchronization

This is intended primarily for Time Domain Scrambling.

4.2.8 Decoder and Encoder Control

This individually sets decoder and encoder sampling clock rates, as well as the source of the audio output.

Setting			**Function**
Byte 1			**First Byte for Transmission**
MSB **Bit 7**			**Not used – Set to '0'**
Bit 6			**Direct Access**
1			Encoder Data out to A0/ENO Encoder Clock to A3/ECK Decoder Input from A1/DEI Decoder Clock from A2/DCK
0			Normal DVSR Operation
Bit 5			**Play Counter**
1			Decrement
0			Increment
Bit 4			**DRAM Control**
1			Disable DRAM
0			Enable DRAM
Bit 3			**Codec Powersave**
1			Powersave MX802
0			MX802 Enable
Bit 2			**Store Command Interrupt**
1			Enable Interrupt
0			Disable
Bit 1			**Play Command Interrupt**
1			Enable Interrupt
0			Disable
Bit 0			**Power Reading Interrupt**
1			Enable Interrupt
0			Disable
Setting			**Function**
Byte 0			**Last Byte for Transmission**
MSB Bit 7	Bit 6		Store/Play Speech Sync.
0	0		No Sync
0	1		No Sync
1	0		Sync – Play after Store
1	1		Sync – Store after Play
Bit 5	Bit 4	Bit 3	Decoder Control
0	0	0	Idle (32kbps); Aud O/P from LPF
0	0	1	Idle (32kbps); Aud bypass
0	1	0	Idle (32kbps); Aud O/P at high Z
0	1	1	On-Sampling Rate 16kbps
1	0	0	On-Sampling Rate 25kbps
1	0	1	On-Sampling Rate 32kbps
1	1	0	On-Sampling Rate 50kbps
1	1	1	On-Sampling Rate 64kbps
Bit 2	Bit 1	Bit 0	Encoder Control
0	0	0	I/P at VBIAS; F/Idle (32kbps)
0	0	1	I/P at high Z; F/Idle (32kbps)
0	1	0	I/P at high Z; F/Idle (64kbps)
0	1	1	On-Sampling Rate 16kbps
1	0	0	On-Sampling Rate 25kbps
1	0	1	On-Sampling Rate 32kbps
1	1	0	On-Sampling Rate 50kbps
1	1	1	On-Sampling Rate 64kbps

Table 6: Control Register

4.3 Encoder and Decoder Control : Analog Input and Output Control

The Control Register, Byte 0: bits 0 to 5, are used together with the codec Powersave Bit (Byte 1: bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

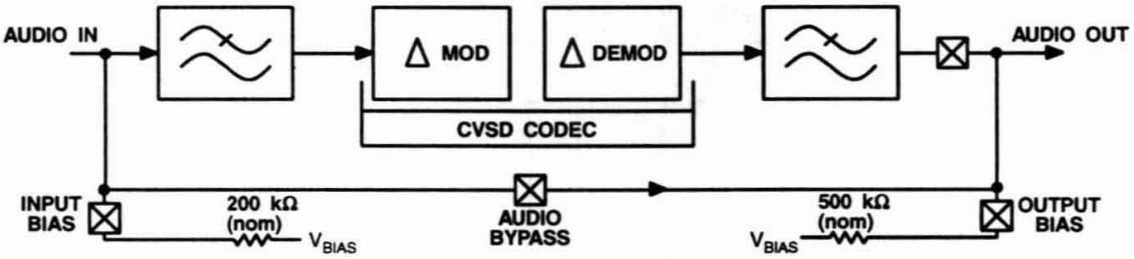


Figure 3: Analog Control (with reference to Figure 1)

Control Register				Circuit Switches				
Codec Powersave Bit	Decoder Control			Audio Bypass	Audio Out	Output Bias	*OFF = Switch Open* *ON = Switch ON*	Note
0	0	0	0	OFF	ON	OFF	Decoder idling fed with "1010101…" pattern at 32kbps.	1
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate.	1
—	—	—	—	—	—	—		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits powersaved.	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
—	—	—	—	-	—	-		
1	1	1	1	OFF	OFF	ON		
	Encoder Control				Input Bias			2
0	0	0	0		ON		Encoder running at 32kbps but Encoder Data O/P forced to idle pattern "01010…"	
0	0	0	1		OFF			
0	0	1	0		OFF			
0	0	1	1		OFF		Encoder running at selected sampling rate	
-	—	—	—		—			
0	1	1	1		OFF			
1	0	0	0		ON		Encoder circuits powersaved.	
-	-	-	-		-			
1	1	1	1		ON			

Table 7: Analog Control (with reference to Figure 3)

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.
2. The input bias switch is operated by the Control Register Codec Powersave and Encoder Control bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the encoder control bits are set to 0, so that input bias can be established quickly prior to operation.

4.3.1 Time Compression of Speech

The 25kbps and 50kbps sampling rate options are provided for time compression and subsequent expansion of speech signals.

For example, 1.0 seconds of speech stored at 50kbps may be transmitted in 0.8 seconds if played out at 64kbps, and finally restored to its original speed at the receiver by storing at 64kbps and playing out at 50kbps. A similar result (with a degraded SINAD) may be achieved by using 25kbps and 32kbps sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400 Hz, the effective end-to-end bandwidth is 0.8 x 3400 Hz, which is approximately 2700 Hz.

4.4 Read Status Register

4.4.1 Interrupts

If enabled by the Control Register, an Interrupt Request (IRQ) is produced by the MX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete

When an Interrupt is produced, the Status Register must be read to determine the source of the interrupt. This action will clear the IRQ output.

The Store Command Complete bit (and an interrupt) is set on completion of a Store Command. This bit is cleared by loading the next Store Command, or by a General Reset Command (01_H).

The Play Command Complete bit (and an interrupt) is set on completion of a Play Command. This bit is cleared by loading the next Play Command, or by a General Reset Command (01_H).

The Power Reading Ready bit (and an interrupt) is set for every 1024 voice-data bits (1 page) from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset Command (01_H).

4.4.2 Power Register

The power assessment element shown in Figure 1 assesses the input signal power for each encoded "page" (every 1024 encoder output bits) by counting the number of "compand bits" (000 or 111 sequences in the output bit stream) produced during that page (see Table 8) with typical encoder input power levels (dB).

At the end of each "page" the power reading ready bit of the status register is set, and an interrupt request is generated (if enabled). The resulting count is converted to a 5-bit quasi-logarithmic form. The Power Register reading is interpreted as follows:

00000 represents 0 compand bits
00001 represents 1 compand bit
11111 represents 512 compand bits, the maximum.

This power reading is placed in the status register to be read by the microcontroller. Figure 4 shows this output, indicating the input power level.

Reading					Function	
MSB						
Bit 7					Power Reading	
1					Ready	
Bit 6					Store Command	
1					Complete	
Bit 5					Play Command	
1					Complete	
					Power Register	
4	**3**	**2**	**1**	**0**	Power	Compand Bits/pg.
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0db	448
1	1	1	1	1		512

Table 8: Status Register

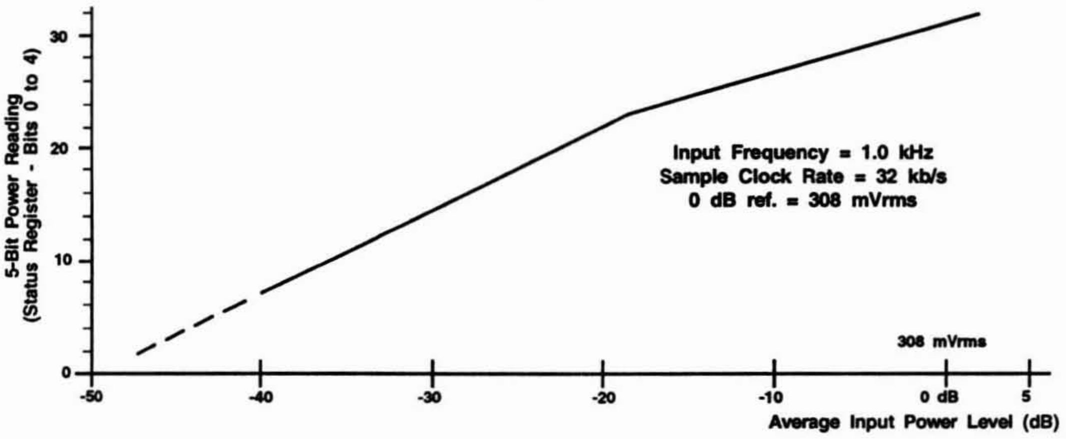


Figure 4: Typical Power Readings vs. Input Levels

5 Application – Codec Performance

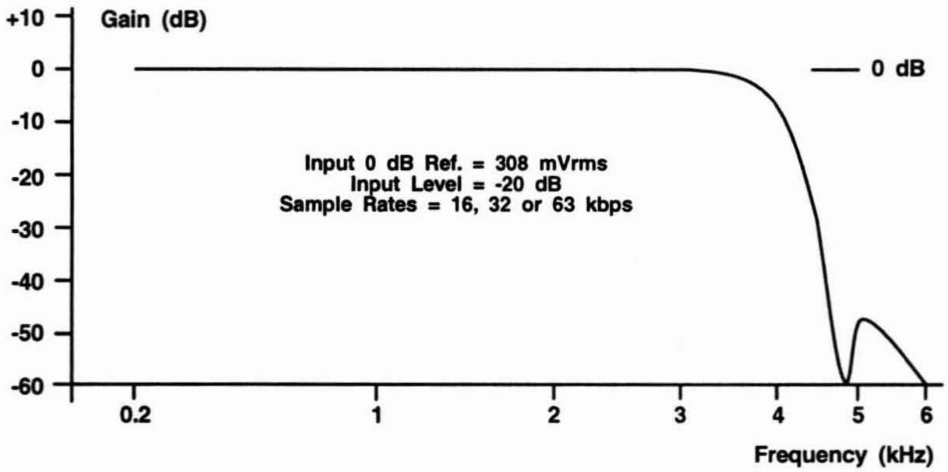


Figure 5: Typical Overall;; (Encoder + Decoder) Frequency Response

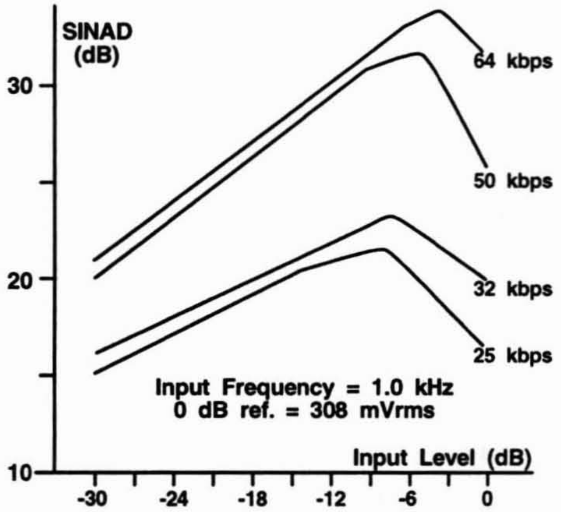


Figure 6: SINAD vs. Input Level at Different Sample Rates

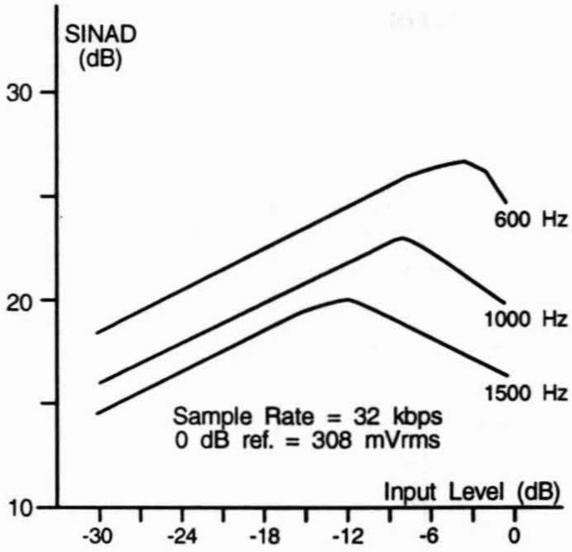


Figure 7: SINAD vs. Input Level at Different Frequencies

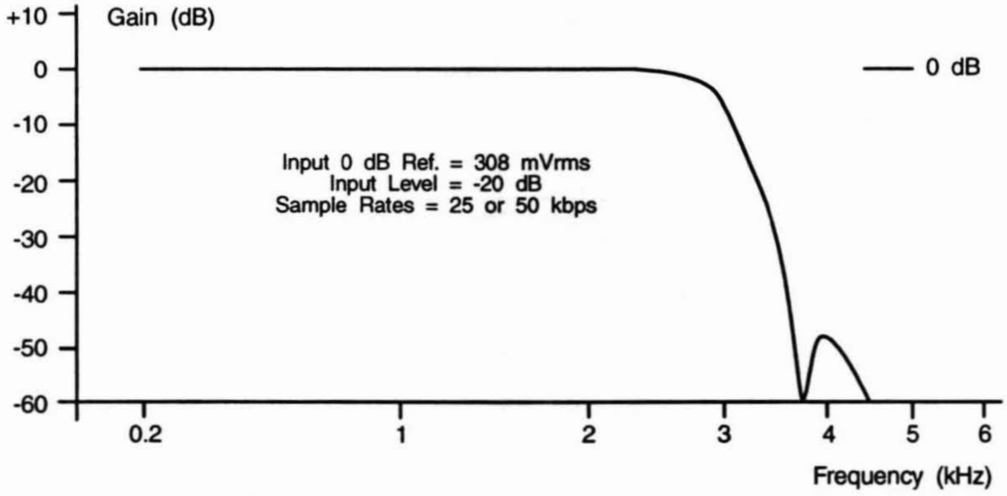


Figure 8: Typical Overall (Encoder + Decoder) Frequency Response

6 Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
J / LH / LH8 Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 9: Absolute Maximum Ratings

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.0		MHz

Table 10: Operating Limits

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.0MHz, Audio Level 0dB ref. = 308mV_{RMS}
Standard test signal f_0 = 820Hz, Sample Rate 31.25kbps

Static Values	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Current					
I_{DD} (enabled)	1		7.0	10.0	mA
I_{DD} (powersave)	1		2.0	4.0	mA
Digital Interface					
Input Logic Level					
Logic 1 Input Level	2	3.5			V
Logic 0 Input Level	2			1.5	V
Output Logic Level					
Output Logic 1 (I_{OH} = 120µA)					
(I_{OH} = -120µA)	7	4.6			V
(I_{OH} = -50µA)	3	4.6			V
(I_{OH} = 20µA)	9	4.6			V
Output Logic 0					
(I_{OL} = 20µA)	9			0.4	V
(I_{OL} = 100µA)	3			0.4	V
(I_{OL} = 360µA)	7, 8			0.4	V
Digital Input Current					
VIN = Logic 1 or 0	2			1.0	µA
Leakage Current into $\overline{\text{IRQ}}$ 'OFF' Output	4			4.0	µA
Digital Input Capacitance	2			7.5	pF
Analog Impedance					
Input Impedance	12		500		KΩ
Output Impedance			1.5		kΩ
Dynamic Values					
Encoder					
Analog signal Input Levels	5	-24.0		4.0	dB
Passband	10, 11		3400		Hz
Decoder					
Analog Signal Output Levels	5	-24.0		4.0	dB
Passband	10, 11	300		3400	Hz

Static Values	Notes	Min.	Typ.	Max.	Units
Encoder/Decoder (Full Codec)					
Passband	10, 11	300		3400	Hz
Passband Gain	11		0		dB
Passband Ripple	11	-3.0		3.0	dB
Stopband		6.0		10	kHz
Stopband Attenuation			50.0		dB
SINAD Level			23.0		dB
Output Noise (Input Short Circuit)			-50		dBp
Idle Channel Noise (Forced)			-55		dBp
Xtal/Clock Frequency	6		4.0		MHz

Table 11: Operating Characteristics

Operating Characteristics Notes:

1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, Chip Select, A1/DE1, and A2/DCK inputs
3. $\overline{CAS}$, $\overline{WE}$, and A0 to A9 inputs.
4. When the $\overline{IRQ}$ output is at V_{DD}.
5. The optimum range levels for a good Signal to Noise ratio.
6. Audio frequency response will vary with respect to Xtal/Clock frequency.
7. Reply Data output.
8. $\overline{IRQ}$ output.
9. RAS output.
10. Passband is reduced to (typically) 2700Hz when a sample rate of 25kbps or 50kbps is used.
11. Measured with a –20dB input level to avoid a codec slope-overload.
12. For optimum noise performance this input should be driven from a source impedance of less that 100Ω.

6.1.4 Timing

C-BUS Timing		Min.			Typ.	Max.	Units
		a	b	c			
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	4.0	8.0			µs
t_{CHS}	Last Serial Clock Rising Edge to Chip Select High	4.0	4.0	8.0			µs
t_{HIZ}	Chip Select High to Reply Data High – Z					2.0	µs
t_{CSOFF}	Chip Select High	2.0	4.0	8.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0	8.0	16.0			µs
t_{CK}	Serial Clock Period	2.0	4.0	8.0			µs
Direct Address Timing							
t_{CH}	Decoder or Encoder Clock High	1.0					µs
t_{CL}	Decoder or Encoder Clock Low	1.0					µs
t_{SU}	Decoder Data Set Up Time	0.45					µs
t_{H}	Decoder Data Hold Time	0.60					µs
t_{PCO}	Encoder Clock High to Encoder Data Valid					0.75	µs
$t_{SU} + t_{H}$ = Data True Time							

Table 12: Timing Information

Notes:

1. Minimum Timing Values
   a. For all commands except "Read Data" and "Write Data" Commands.
   b. For all "Read Data" and Write Data" commands when no "Speech Store" or "Speech Play" commands are active.
   c. For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.
2. Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first and LSB (bit0) last. Reply data is read from the peripheral MSB (bit7) first and LSB (bit0) last.
3. To allow for different microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.
4. Data is clocked into and out of the peripheral on the rising Serial clock edge.
5. Loaded commands are acted upon at the end each command.

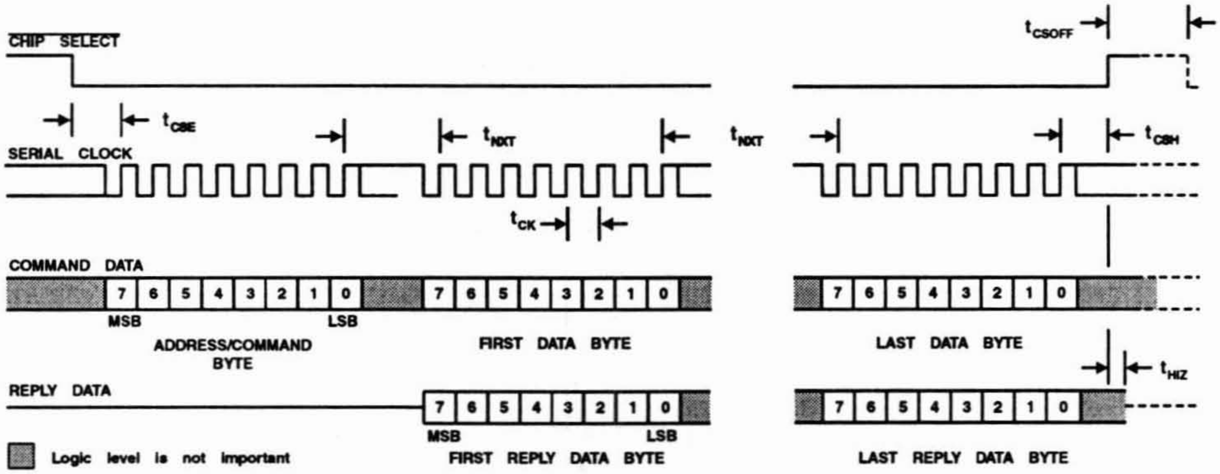

CHIP SELECT
t_{CSOFF}
t_{CSE}
t_{NXT}
t_{NXT}
t_{CSH}
SERIAL CLOCK
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
Logic level is not important

Figure 9: C-BUS Timing Information

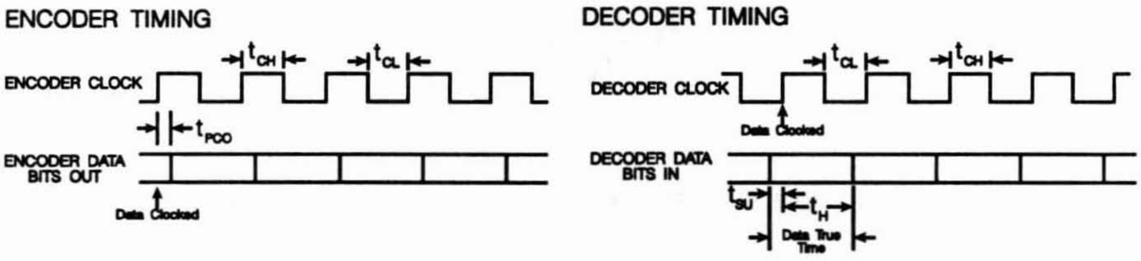
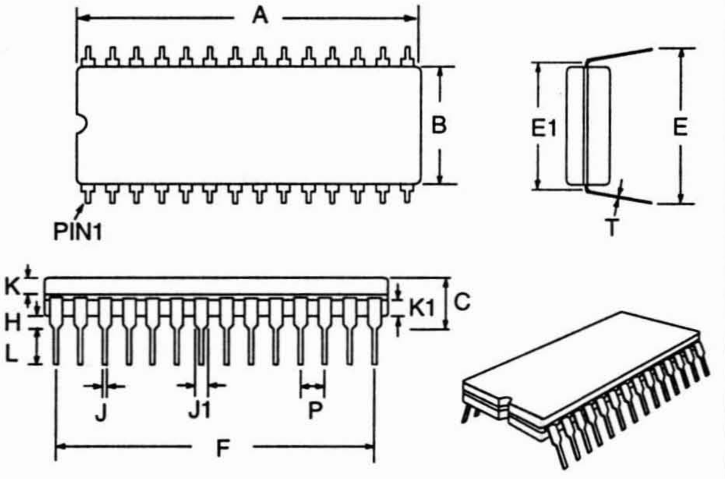

ENCODER TIMING
t_{CH}
t_{CL}
ENCODER CLOCK
t_{PCO}
ENCODER DATA BITS OUT
Data Clocked
DECODER TIMING
t_{CL}
t_{CH}
DECODER CLOCK
Data Clocked
DECODER DATA BITS IN
t_{SU}
t_H
Data True Time

Figure 10: Codec Direct Access Timing

6.2 Packages

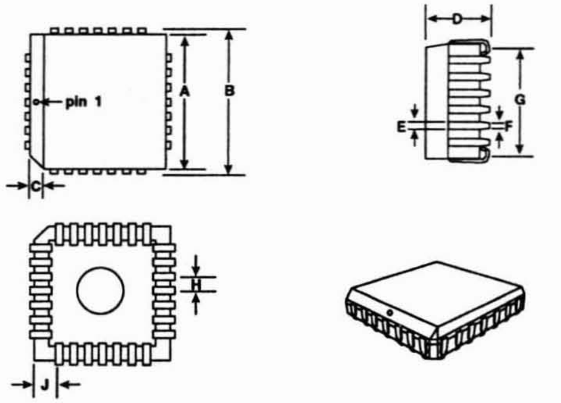


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.58)		1.460 (37.08)
B	0.510 (12.94)		0.530 (13.45)
C	0.165 (4.19)		0.230 (5.84)
E	0.640 (16.26)		0.715 (18.14)
E1	0.608 (15.43)		0.618 (15.70)
F		1.300 (33.02)	
H	0.015 (0.38)		0.050 (1.27)
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0090 (0.228)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 28-pin CERDIP Mechanical Outline: ***Order as part no. MX802J***

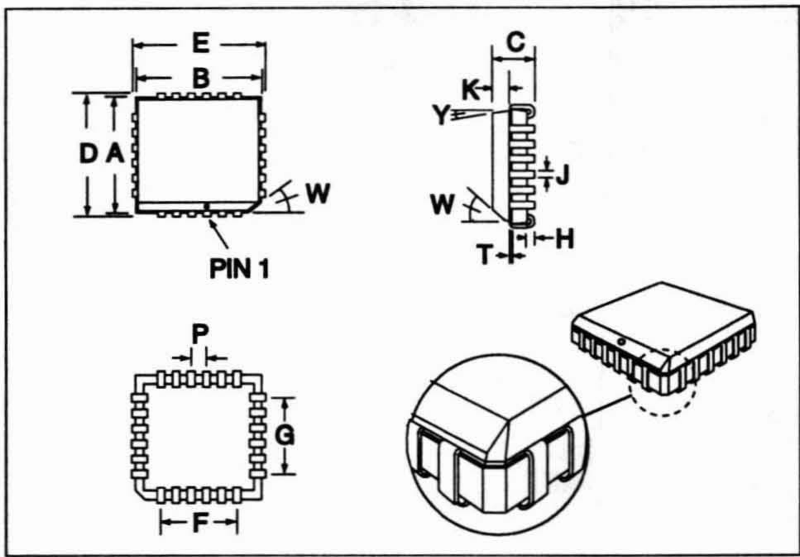


Package Tolerances

DIM.	MIN.	MAX.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 28-pin PLCC Mechanical Outline: ***Order as part no. MX802LH8***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin PLCC Mechanical Outline: ***Order as part no. MX802LH***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX803A Audio Signaling Processor

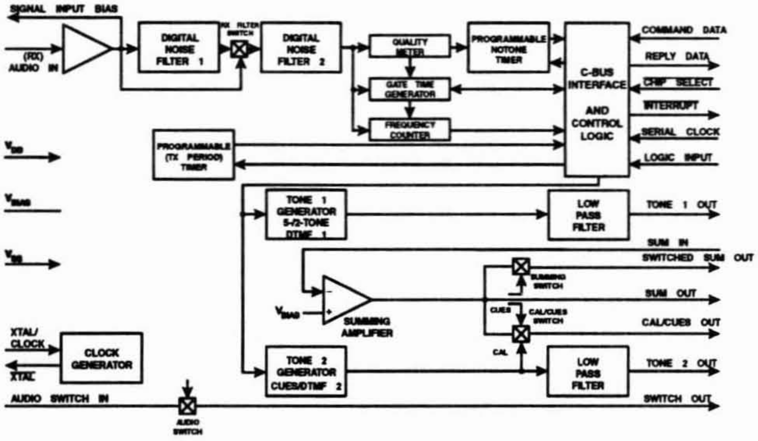
PRELIMINARY INFORMATION

Features

- **Full Duplex Audio Signaling Processor**
  - **Single Tone**
  - **Selective Call systems**
- **Tone Decoder with programmable NOTONE timer.**
- **Two Individual tone encoders and a programmable TX Period Timer.**
- **Low Power CMOS Device**
- **On-Chip programmable amplifier.**
- **C-BUS Compatible**

Applications

- **Signaling Systems supported**
  - **SelCall (CCIR, EEA, ZVEI I / II /III)**
  - **2-Tone SelCall**
  - **DTMF Encode**
- **Inband Tone Signaling capability for LMR and other Radio Systems.**


SIGNAL INPUT BIAS
(RX) AUDIO IN
DIGITAL NOISE FILTER 1
RX FILTER SWITCH
DIGITAL NOISE FILTER 2
QUALITY METER
GATE TIME GENERATOR
FREQUENCY COUNTER
PROGRAMMABLE NOTONE TIMER
C-BUS INTERFACE AND CONTROL LOGIC
COMMAND DATA
REPLY DATA
CHIP SELECT
INTERRUPT
SERIAL CLOCK
LOGIC INPUT
V_{DD}
V_{BIAS}
V_{SS}
PROGRAMMABLE (TX PERIOD) TIMER
TONE 1 GENERATOR 5-/2-TONE DTMF 1
LOW PASS FILTER
TONE 1 OUT
SUM IN
SWITCHED SUM OUT
SUMMING SWITCH
SUM OUT
V_{BIAS}
SUMMING AMPLIFIER
CUES
CAL/CUES SWITCH
CAL/CUES OUT
CAL
XTAL/ CLOCK
XTAL
CLOCK GENERATOR
TONE 2 GENERATOR CUES/DTMF 2
LOW PASS FILTER
TONE 2 OUT
AUDIO SWITCH IN
AUDIO SWITCH
SWITCH OUT

The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Sub-system) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

The MX803A is available in 24-pin CDIP (MX803AJ), 24-pin PLCC (MX803ALH), and 24-pin SOIC (MX803ADW) packages.

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- 4.2 DBS800 Systems .... 3 - 472
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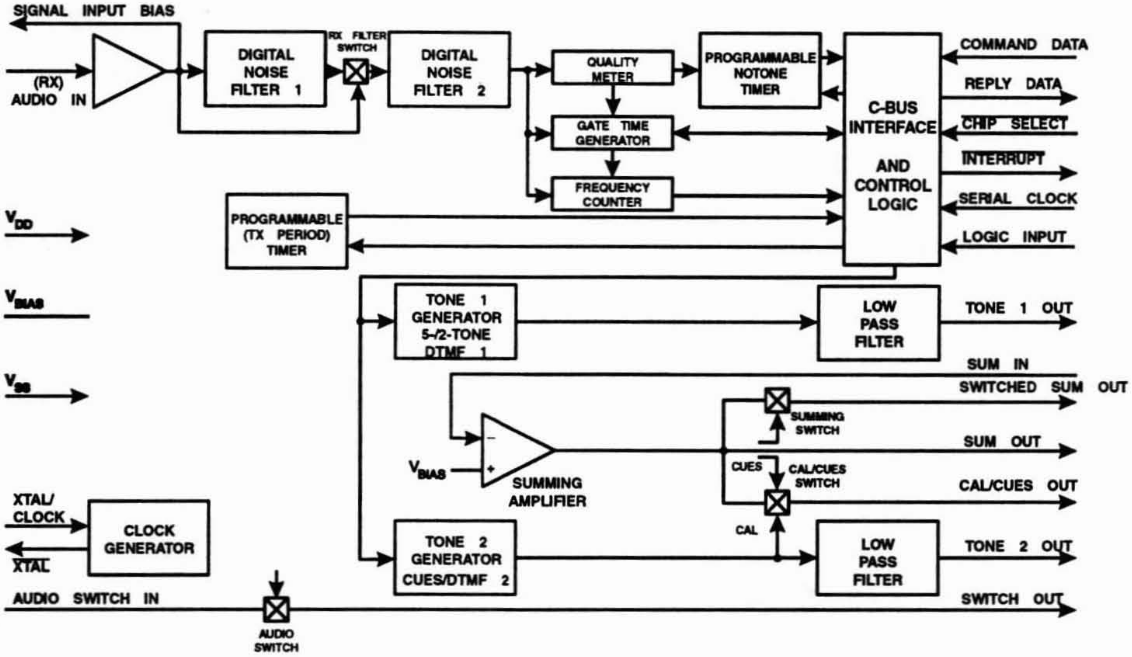
MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram


SIGNAL INPUT BIAS
(RX) AUDIO IN
DIGITAL NOISE FILTER 1
RX FILTER SWITCH
DIGITAL NOISE FILTER 2
QUALITY METER
GATE TIME GENERATOR
FREQUENCY COUNTER
PROGRAMMABLE NOTONE TIMER
C-BUS INTERFACE AND CONTROL LOGIC
COMMAND DATA
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LOGIC INPUT
V_{DD}
V_{BIAS}
V_{SS}
PROGRAMMABLE (TX PERIOD) TIMER
TONE 1 GENERATOR 5-/2-TONE DTMF 1
LOW PASS FILTER
TONE 1 OUT
SUM IN
SWITCHED SUM OUT
SUMMING SWITCH
SUM OUT
V_{BIAS}
SUMMING AMPLIFIER
CUES
CAL/CUES SWITCH
CAL/CUES OUT
CAL
XTAL/ CLOCK
XTAL
CLOCK GENERATOR
TONE 2 GENERATOR CUES/DTMF 2
LOW PASS FILTER
TONE 2 OUT
AUDIO SWITCH IN
AUDIO SWITCH
SWITCH OUT

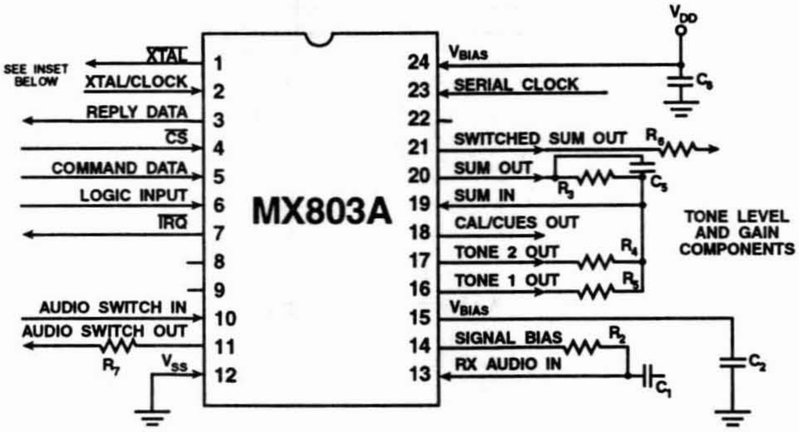
Figure 1: Block Diagram

2. Signal List

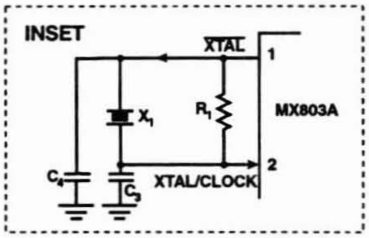
Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	Output	Output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	Xtal/Clock	Input	Input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2.
3	Reply Data	Output	C-BUS serial data output to the μC. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the μC. See Figure 8 and Figure 9.
4	$\overline{\text{CS}}$	Input	C-BUS data loading control function. This input is provided by the μC. Data transfer sequences are initiated, completed or aborted by the chip select signal. See Figure 8 and Figure 9.
5	Command Data	Input	C-BUS serial data input from the μC. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Figure 8 and Figure 9.
6	Logic Input	Input	This "real-time" input is available as a general purpose logic input port which can be read from the Status Register. See Table 3. G/Purpose Timer Period Expired NOTONE Timer Period Expired RX Tone Measurement Complete These interrupts are inactive during relevant powersave conditions and can be disabled by bits 5 and 6 in the Control Register.
7	$\overline{\text{IRQ}}$	Output	Output of this pin indicates an interrupt condition to the μC by going to a logic "0." This is a "wire-or-able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the μC. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The system IRQ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below:
10	Audio Switch In	Input	Input to the stand-alone on-chip Audio Switch. This function is enabled/disabled by Bit 7 of the Control Register
11	Audio Switch Out	Output	Output of the stand-alone on-chip Audio Switch..
12	V_{SS}	Power	Negative supply (GND).
13	Rx Audio In	Input	Received audio tone signaling input. This input must be ac coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2.
14	Signal Input Bias	Input	External components are required between this input and the RX Audio In pin. See Figure 2.
15	V_{BIAS}	Output	Internal circuitry bias signal, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C2. See Figure 2..
16	Tone 1 Out	Output	Tone 1 Generator (2-/5-tone Selcall or DTMF 1) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 1 Register (Table 5). See Figure 2.
17	Tone 2 Out	Output	Tone 2 Generator (2-/5-tone Selcall, CUES or DTMF 2) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 2 Register (Table 5). See Figure 2.

Pin No.	Name	Type	Description
18	CAL/CUES Out	Output	An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from the Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the TX Tone Generator 2 Register (Table 5). When Tone Generator 2 is set to Notone, the CAL input is pulled to V_{BIAS}; during a powersave of Tone Generator 2 it is held at V_{SS}.
19	Sum in	Input	Input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figure 2 and Figure 3
20	Sum Out	Output	Output of the on-chip summing amplifier. Combined tones (1 and 2) are available at this output. See Figure 2 and Figure 3.
21	Switched Sum Out	Output	This is the combined tone output available for transmitter modulation. The switch allows control of the MX803A output. Control of this switch is by Bit 4 of the Control Register. See Figure 2 and Figure 3.
23	Serial Clock	Input	C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the MX803A. See Figure 8 and Figure 9.
24	V_{DD}	Power	Positive supply. A single +5 volt power supply is required. Levels and voltages within this Audio Signaling Processor are dependent upon this supply..
8, 9, 22	N/C		No Internal Connection. These pins may be connected to V_{SS} to improve screening and reduce noise levels around the MX803A.

3. External Components



SEE INSET BELOW
XTAL
XTAL/CLOCK
REPLY DATA
CS
COMMAND DATA
LOGIC INPUT
IRQ
AUDIO SWITCH IN
AUDIO SWITCH OUT
R7
VSS
1
2
3
4
5
6
7
8
9
10
11
12
MX803A
24
23
22
21
20
19
18
17
16
15
14
13
VBIAS
SERIAL CLOCK
SWITCHED SUM OUT
SUM OUT
SUM IN
CAL/CUES OUT
TONE 2 OUT
TONE 1 OUT
VBIAS
SIGNAL BIAS
RX AUDIO IN
VDD
C6
R6
R3
C5
R4
R5
R2
C1
C2
TONE LEVEL AND GAIN COMPONENTS



INSET
XTAL
1
X1
R1
MX803A
2
C4
C3
XTAL/CLOCK

R1		1.0MΩ	±10%
R2		2.0MΩ	±10%
R3	Note 2, 3	100kΩ	±10%
R4	Note 2, 3	82.0kΩ	±10%
R5	Note 2, 3	122kΩ	±10%
R6	Note 2	100kΩ	±10%
R7	Note 2, 5	100kΩ	±10%

C1		0.1μF	±20%
C2		1.0μF	±20%
C3	Note 4	33.0pF	±20%
C4	Note 4	33.0pF	±20%
C5	Note 3	22.0pF	±20%
C6		1.0μF	±20%
X1	Note 1, 4	4.00MHz	

Figure 2: Recommended External Components

Notes:

1. Xtal/clock components described are recommended in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillator Circuits (April 1990). For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. System Components whose values are calculated to allow the MX803A to operate with other DBS 800 microcircuits. Figure 3 shows these components used in the system signal paths.
3. R3, R4, R5 and C5 are tone mixing components calculated to provide a 3dB tone differential (twist) for use in a DTMF configuration. Single tone output levels are set independently.
4. When X1 > 5.00MHz, C3 = C4 = 18pF
5. R7 provides modulation level and matching outputs for the MX803A.

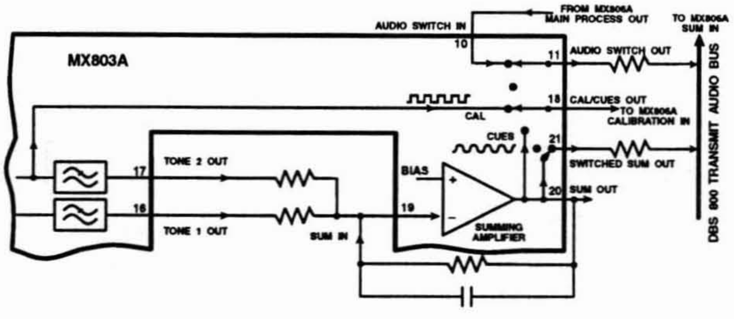


Figure 3: Example of Signal Switching in a DBS800 microcircuit

4. General Description

4.1 DESCRIPTION

The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Sub-system) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

A general purpose logic input, interfacing directly with the Status Register, is provided. This may be used as an auxiliary method of routing digital information to the µC via C-BUS. Output frequencies are produced from data loaded to the MX803A. A programmable, general purpose, on-chip timer sets the tone transmit periods. A Dual-Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This process can also be used for level correction.

Tones produced by the MX803A can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator. Received tones are measured and their frequency indicated to the µC in the form of a received data word. A poor quality or incoherent tone will indicate Notone.

4.2 DBS800 Systems

The Digitally-Integrated Baseband Subsystem (DBS800) is a family of low power ICs which provide a comprehensive range of audio processing and signaling functions for use within LMR and other Radio Systems. Each DBS800 IC may be used as part of a complete audio system, or each IC may operate as a stand alone. The system and ICs are partitioned in such a way that radio designers can easily select the device or devices appropriate to their needs.

The DBS800 family consists of the following ICs:

4.2.1 MX802 DVSR Codec

This is a full-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller. The MX802 also provides on-chip input and output audio filtering.

4.2.2 MX803A Audio Signaling Processor

This provides an inband tone signaling ability to LMR and other Radio Systems.

4.2.3 MX805A Sub-Audio Signaling Processor

This provides a sub-audio and digital signaling (NRZ) ability to LMR and other Radio Systems.

4.2.4 MX806A Audio Processor

This is a half duplex audio processor providing all DBS800 system audio signal conditioning and filtering capabilities for the system transmit and receive paths.

4.2.5 MX809 MSK Modem

This is an intelligent, half-duplex 1200bps MSK/FFSK Modem with software programmable byte-synchronization system and checksum generation and checking.

4.2.6 MX812 VSR Codec

This is a half-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller

4.3 C-BUS Control

C-BUS is the controlling hardware and software interface for all members of the DBS800 family. It enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

The C-BUS physically consist of 5 lines. These lines are Serial Clock, Command Data, Reply Data, Chip Select ($\overline{CS}$), and Interrupt Request ($\overline{IRQ}$). A description of each may be found in section 2.

5. Application

Control of the MX803A Audio Signaling Processor's operation is by communication between the µC and the MX803A internal registers on the C-BUS using Address/Commands (A/Cs) and appended instructions or data. See Figure 8. The use and content of these instructions is detailed in the following sections.

For additional application information contact MX•COM, Inc.

5.1 MX803A Internal Registers

Control Register	30_H	Write only, control and configuration of the MX803A.
Status Register	31_H	Read only, reporting of device functions.
RX Tone Frequency Register	32_H	Read only, indicates frequency of the last received input.
RX Notone Timer	33_H	Write only, setting of the RX Notone period.
TX Tone Generator 1 Register	34_H	Write only, setting the required output frequency from TX Tone Generator 1.
TX Tone Generator 2 Register	35_H	Write only, setting the required output frequency from TX Tone Generator 2.
General Purpose Timer Register	36_H	Write only, setting of a general purpose sequential time period.

5.2 Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an A/C byte followed by further instruction/data or a status/data reply.

Instructions and data are loaded and transferred via C-BUS in accordance with the timing information given in Figure 8 and Figure 9. Table 1 shows the list of A/C bytes relevant to the MX803A.

Command Assignment	**Address/Command (A/C) Byte**		**Data Bytes**
	Hex	Binary	
		msb lsb	
General Reset	01	00000001	
Write to Control Register	30	00110000	+ 1 byte instruction to Control Register
Read Status Register	31	00110001	+ 1 byte reply from Status Register
Read RX Tone Frequency	32	00110010	+ 2 bytes reply from RX Tone Register
Write to Notone Timer	33	00110011	+ 1 byte instruction to Notone Register
Write to TX Tone Gen. 1	34	00110100	+ 2 bytes instruction to TX Tone Gen. 1
Write to TX Tone Gen. 2	35	00110101	+ 2 bytes instruction to TX Tone Gen. 2
Write to G/Purpose Timer	36	00110110	+ 1 byte instruction to G/Purpose Timer

Table 1: C-BUS Address/Commands

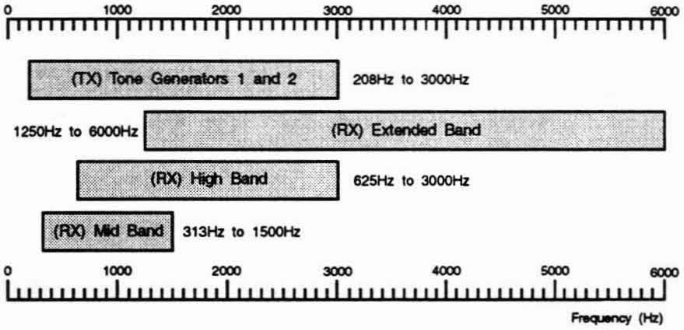


Figure 4: MX803A Frequencies

5.2.1 Write to Control Register

A/C 30_H, followed by 1 byte of Command Data

Audio Switch: Enables or Disables the stand-alone on-chip Audio Switch.

General Purpose Timer: This should be set up before interrupts are enabled since a General Reset command will set the timer period to 00_H - 0ms (permanent interrupt).

Interrupt Enable Instructions: Status bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection: Bits 2 and 3 set the required frequency range. See Figure 4.

Summing Switch: Used to Enable or Disable the switch that controls the MX803A output.

Interrupt Designation: Decoder Interrupts

- Notone Timer and RX Tone Measurement

Transmitter Interrupt

- G/Purpose Timer Interrupt

Setting		Control Bits
MSB		**Transmitted First**
Bit 7		**Audio switch**
1		Enable
0		Disable
Bit 6		**G/Purpose Timer Interrupt**
1		Enable
0		Disable
Bit 5		**Decoder Interrupts**
1		Enable
0		Disable
Bit 4		**Summing Switch**
1		Enable
0		Disable
Bit 3	**Bit 2**	**Band Selection**
0	0	High Band
0	1	Mid Band
1	0	Extended Band
1	1	Do not use this setting
Bit 1		**Set to**
0		0
Bit 0		**Set to**
0		0

Table 2: Control Register

5.2.2 Read Status Register

A/C 31_H, followed by 1 byte of Reply Data

Interrupt Requests (IRQ): Interrupts on this device are available to draw the attention of the μC to a change in the condition of the bit in the status register. However, bits are set in the status register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by polling the register.

General Purpose Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New G/Purpose Timer information
3. General Reset command

Notone Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New Notone Timer information
3. General Reset command

RX Tone Measurement: Set to a logic "1" when the RX Tone Measurement is complete. Cleared to a logic "0" by:

1. Reading the Status Register
2. General Reset command

Setting	**Status Bits**
MSB	**Received First**
Bit 7	**Set to**
0	0
Bit 6	**Set to**
0	0
Bit 5	**Set to**
0	0
Bit 4	**Set to**
0	0
Bit 3	**Logic Input Status**
1	1
0	0
Bit 2	**G/Purpose Timer Period**
1	Expired
	(Interrupt Generated)
Bit 1	**Notone Timer Period**
1	Expired
	(Interrupt Generated)
Bit 0	**RX Tone Measurement**
1	Complete
	(Interrupt Generated)

Table 3: Status Register

5.2.3 TX Tone Generator Registers 1 and 2

Each TX Tone Generator is controlled individually by writing a two-byte command to the relevant TX Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

5.2.3.1 Write to TX Tone Generator 1 Register

A/C 34_H, followed by 2 bytes of Command Data

MSB (loaded first)							**Bit Numbers**								**LSB (loaded last)**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'A'. 'A' is used in the formulas below to set the TX Tone 1 frequency ($f_{TONE}1$).												

Table 4: Tx Tone Generator 1

5.2.3.1.1 SETTING TX TONE GENERATOR 1

The binary number produced by Bits 0 to 12 (MSB) is designated "A." If "A" = all logic "0" TX Tone Generator 1 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled
Bits14 and15(MSB) must be logic 0

5.2.3.2 Write to TX Tone Generator 2 Register

A/C 35_H, followed by 2 bytes of Command Data

MSB (loaded first)			**Bit Numbers**												**LSB (loaded last**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CAL/CUES	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'B'. 'B' is used in the formulas below to set the TX Tone 2 frequency ($f_{TONE}2$).												

Table 5: Tx Tone Generator 2

Write to TX Tone Generator 2 Register Notes:

Programming Tone Generator 2 to Notone will place the CAL/CUES output at V_{BIAS} via a 40kΩ internal resistor.

Programming Tone Generator 2 to Powersave will place the CAL/CUES output at V_{SS}.

If both Tone Generators are Powersaved, the Input Amplifier is also Powersaved

5.2.3.2.1 SETTING TX TONE GENERATOR 2

The binary number produced by bits 0 to 12 (MSB) is designated "B." If "B" = all logic "0" then TX Tone Generator 2 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled
Bit 14 at logic 1 = Squarewave CAL Output
0 = Sinewave CUES Output
Bit 15 (MSB) must be a logic "0."

5.2.3.3 Calculations

As seen in Table 4 and Table 5, a binary number ("A" or "B" - bits 0 to 12) is loaded to the respective TX Tone Generator. The formulas described below are used to produce the required output frequency.

Required TX Tone output frequency = f_{TONE} 1 or 2
Xtal/clock frequency = f_{XTAL}
Input Data Word (bits 0 to 12) = "A" or "B"

$$f_{TONE} = \frac{f_{XTAL}}{4 \times \text{'A' or 'B'}} \text{ Hz} \quad \text{or} \quad \text{Input 'A' or 'B'} = \frac{f_{XTAL}}{4 \times f_{TONE}} \text{ Hz}$$

5.2.3.4 Tx Tone Frequencies

With reference to Table 4 and Table 5, while Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters. See section 7.

5.2.4 Read RX Tone Frequency Register

A/C 32_H, followed by 2 bytes of Reply Data

5.2.4.1 Measurement of RX Signal Frequency S_{IN}

The input audio signal, S_{IN}, is measured in the Frequency Counter over a specified measurement period (9.125ms or 18.250ms).

The measuring function counts the number of complete input cycles occurring within the count period and then the number of measuring clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The RX Tone Frequency Register will now indicate the signal frequency S_{IN} in the form of 2 bytes (1 and 0) as illustrated in Figure 6.

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other crystal values).

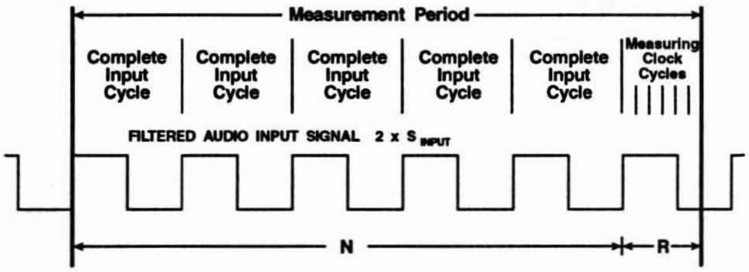


Figure 5: Measurement of an Rx Frequency

5.2.4.2 The Integer (N) - Byte 1

This is a binary number representing twice the number of complete input audio cycle periods. It is counted during the specified measurement period (t), when (t) is:

High Band Decode = 9.125ms
Mid Band Decode = 18.250ms
Extended Band Decode = 9.125ms

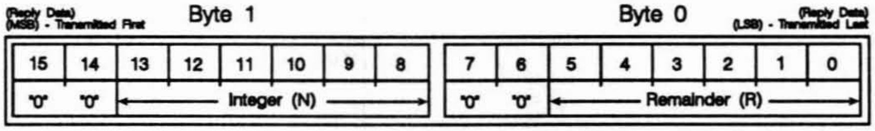
Note: See section 5.2.4.4 for calculation of measurement period (t) using a Xtal other than 4.032MHz.

5.2.4.3 The Remainder (R) - Byte 0

This is a binary number representing the remainder part, R, of twice the Input Signal Frequency. R = "the number of specified measuring-clock cycles" required to complete the specified measurement period (See 5.2.4.2). The clock cycle frequency (f) is:

High Band Decode = 56.00kHz
Mid Band Decode = 28.00kHz
Extended Band Decode = 56.00kHz

Note: See section 5.2.4.4 for calculation of clock cycle frequency (f) using a Xtal other than 4.032MHz.



RX Frequency Register

Figure 6: Format of the Rx Tone Frequency Register

5.2.4.4 f_{XTAL} Scaling Factors

The following formulas allow the calculation of the Integer N (see section 5.2.4.2) and the Remainder R (see section 0) using any Xtal value.

$$t \text{ scaled} = t \times \left(\frac{4.032}{f_{XTAL}}\right) \qquad f \text{ scaled} = f \times \left(\frac{f_{XTAL}}{4.032}\right)$$

5.2.5 Frequency Measurement

The following formulas show the derivation of the Rx frequency S_{IN} from the measured data bytes (N and R)

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other Xtal values.

5.2.5.1 High Band Measurement

S_{IN} - High Band

In the measurement period of 9.125ms, there are N cycles at $2S_{IN}$ and R clock cycles at 56.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{56000} = 9.125\text{ms}$$

$$\text{from which } S_{IN} = \frac{28000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 9.125 \times 10^{-3}$ cycles

N_{HIGH} is the lower integer value of the decimal number:

$$N = \text{INT}(9.125 \times 10^{-3} \times 2S_{IN})$$

R_{HIGH} is the lower integer value of the decimal number:

$$R = \text{INT}\left(9.125 \times 10 - 3 - \frac{N}{2S_{IN}}\right) \times 56000$$

5.2.5.2 Mid Band Measurement

S_{IN} - MID Band

In the measurement period of 18.250ms, there are N cycles at $2S_{IN}$ and R clock cycles at 28.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{28000} = 18.250\text{ms}$$

$$\text{from which } S_{IN} = \frac{14000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 18.250ms.
Clock Frequency = 28.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 18.250 \times 10^{-3}$ cycles

N_{MID} is the lower integer value of the decimal number:

$N = \text{INT}(18.250 \times 10^{-3} \times 2S_{IN})$

R_{MID} is the lower integer value of the decimal number:

$$R = \text{INT}\left(18.250 \times 10^{-3} - \frac{N}{2S_{IN}}\right) \times 28000$$

5.2.5.3 Extended Band Measurement

S_{IN} - Extended Band

In the measurement period of 9.125ms, there are N cycles at $2S_{IN}$ and R clock cycles at 56.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{56000} = 9.125\text{ms}$$

$$\text{from which } S_{IN} = \frac{28000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 9.125 \times 10^{-3}$ cycles

$N_{EXTENDED}$ is the lower integer value of the decimal number:

$N = \text{INT}(9.125 \times 10^{-3} \times 2S_{IN})$

$R_{EXTENDED}$ is the lower integer value of the decimal number:

$$R = \text{INT}\left(9.125 \times 10 - 3 - \frac{N}{2S_{IN}}\right) \times 56000$$

5.2.6 Write to RX Notone Timer Register

A/C 33_H, followed by 1 byte of Command Data

5.2.6.1 Operation of the RX Notone Timer

A NOTONE period is that period when no signal or a consistently bad quality signal is received. The NOTONE Timer is employed to indicate to the µC that a NOTONE situation has existed for a predetermined period.

The NOTONE Timer period is "primed" by writing to the NOTONE Timer Register (33_H) using the instructions and information (1 data byte) given in Table 6. This timer register can be written-to and set in any mode of the MX803A except "Notone Timer Powersave." Priming the timer sets the timing period; this period will not be allowed to start until at least one frequency (tone) measurement has been successfully completed.

The NOTONE Timer is a one-shot timer that is reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down. On completion of this timer period, the NOTONE Timer Period Expired bit in the Status Register and an Interrupt are set.

Upon detection of the Interrupt, the Status Register should be read by the µC to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

1. By a read of the Status Register.
2. New NOTONE Timer Information
3. General Reset Command

The timer is set to 00_H by a General Reset command.

Setting				**Function / Period**			
MSB							
7	**6**	**5**	**4**	**Transmitted Bit 7 first**			
0	0	0	0	these 4 bits must be 0			
				period (ms)			
3	**2**	**1**	**0**	**High Band**	**%**	**Mid Band**	**%**
0	0	0	0	0		0	
0	0	0	1	20	±1	40	±1
0	0	1	0	40	±1	80	±1
0	0	1	1	60	±1	120	±1
0	1	0	0	80	±1	160	±1
0	1	0	1	100	±1	200	±1
0	1	1	0	120	±1	240	±1
0	1	1	1	140	±1	280	±1
1	0	0	0	160	±1	320	±1
1	0	0	1	280	±1	360	±1
1	0	1	0	200	±1	400	±1
1	0	1	1	220	±1	440	±1
1	1	0	0	240	±1	480	±1
1	1	0	1	260	±1	520	±1
1	1	1	0	280	±1	560	±1
1	1	1	1	300	±1	600	±1

Table 6: RX Notone Timer Settings

5.2.6.2 NOTONE TIMER CIRCUITRY

The following situations may be encountered by the Notone Timer Circuitry

5.2.6.2.1 No Signal

The Notone timer can only start its run down on completion of a valid frequency measurement.

5.2.6.2.2 No signal after a valid Tone measurement

The timer will start to run down when the last RX Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.3 Signal fades after a valid Tone measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.4 Signal appears after the Timer has started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

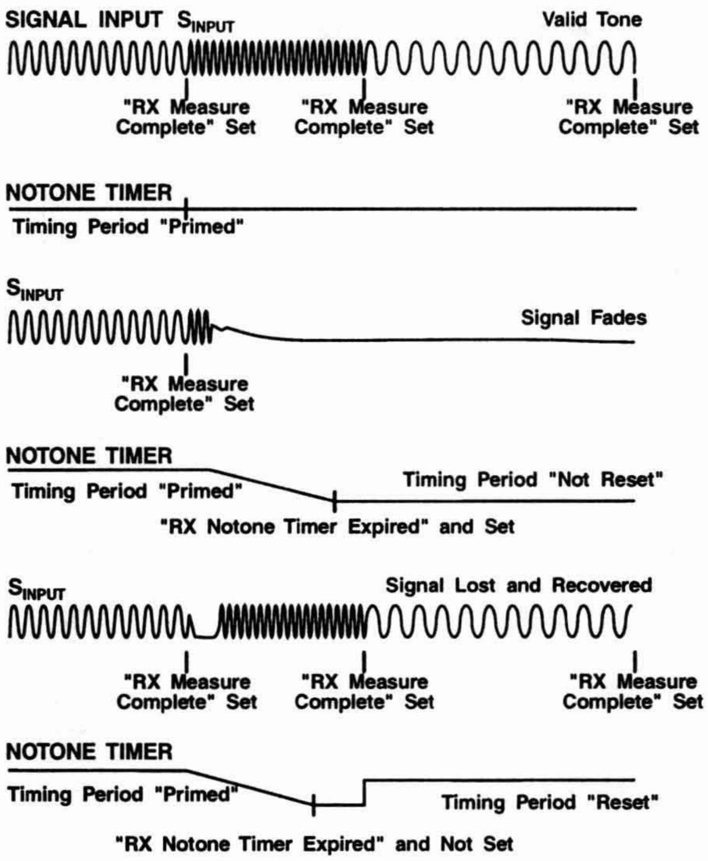

SIGNAL INPUT S_{INPUT}
Valid Tone
"RX Measure Complete" Set
"RX Measure Complete" Set
"RX Measure Complete" Set
NOTONE TIMER
Timing Period "Primed"
S_{INPUT}
Signal Fades
"RX Measure Complete" Set
NOTONE TIMER
Timing Period "Primed"
Timing Period "Not Reset"
"RX Notone Timer Expired" and Set
S_{INPUT}
Signal Lost and Recovered
"RX Measure Complete" Set
"RX Measure Complete" Set
"RX Measure Complete" Set
NOTONE TIMER
Timing Period "Primed"
Timing Period "Reset"
"RX Notone Timer Expired" and Not Set

Figure 7: Notone Timing

5.2.7 Write to General Purpose Timer Register

A/C 36_H, followed by 1 byte of Command Data

5.2.7.1 Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the MX803A, can be used within the DBS 800 system to indicate time-elapsed periods of between 10-150ms in the High Band or 20-300ms in the Mid Band to the µC. Setting of the timer is by loading a single byte data word via the C-BUS (See Table 7) to the MX803A through the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (bit 2) in the Status Register and the Interrupt are set.

The General Purpose Timer Expired bit is cleared:

1. By a read of the Status Register
2. New G/P Timer information
3. General Reset Command.

When the programmed time period has expired, this timer will reset, restart itself and continue sequencing until:

1. New G/P Timer information is written
2. A General Reset Command is received.

The General Purpose Timer Expired bit and the interrupt will remain set until cleared.

The timer is set to 00_H (0ms) by a General Reset command.

Setting				**Function / Period**			
MSB							
7	**6**	**5**	**4**	**Transmitted Bit 7 first**			
0	0	0	0	these 4 bits must be 0			
				Reset Timer and Start Timing period (ms)			
3	**2**	**1**	**0**	**High Band**	**%**	**Mid Band**	**%**
0	0	0	0	0		0	
0	0	0	1	10	±1	20	±1
0	0	1	0	20	±1	40	±1
0	0	1	1	30	±1	60	±1
0	1	0	0	40	±1	80	±1
0	1	0	1	50	±1	100	±1
0	1	1	0	60	±1	120	±1
0	1	1	1	70	±1	140	±1
1	0	0	0	80	±1	160	±1
1	0	0	1	90	±1	180	±1
1	0	1	0	100	±1	200	±1
1	0	1	1	110	±1	220	±1
1	1	0	0	120	±1	240	±1
1	1	0	1	130	±1	260	±1
1	1	1	0	140	±1	280	±1
1	1	1	1	150	±1	300	±1

Table 7: General Purpose Timer Settings

5.3 Powersave

Various sections of the MX803A can be placed independently into a power-economical condition. Table 8 gives a summary of these states available to the MX803A.

Powersaved Section	**Instruction Source**		**Table**
Tone Encoder 1	TX Tone Gen. 1 Reg. (34_H)	All bits = "0"	Table 4
Tone Encoder 2	TX Tone Gen. 2 Reg. (35_H)	All bits = "0"	Table 5
Input Amplifier	This action is automatic when both Tone Encoders are in the Powersave condition		

Table 8: MX803A Powersave Functions

5.3.1 Powersave Conditions

Xtal/Clock and C-BUS: This circuitry is always active, on all DBS 800 ICs, under any depowered/powersaved conditions

5.4 Interrupt Request $\overline{\text{IRQ}}$

An Interrupt (IRQ), when enabled, is provided by the MX803A to indicate the following conditions to the µC.

	Notone Timer Period Expired	**G/Purpose Timer Period Expired**	**Rx Tone Measurement Complete**
Enabled	By control Resister bit 5	By control Resister bit 6	By control Resister bit 5
Set	When the preset Notone Flag is set	When the General Purpose Timer has timed out.	When an RX Frequency Measurement has been successfully completed
Identified	By Status Register bit 1	By Status Register bit 2	By Status Register bit 0
Cleared	By reading the Status Register	By reading the Status Register	By reading the Status Register

Table 9: Interrupt Request

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status bits are transferred to the µC via the C-BUS Reply Data line and the internal Status bits are cleared.

5.5 Operational Recommendations

Following initial system power-up, a General Reset command should be sent.

5.5.1 Receive Sequence

1. Send Control Command for RX: Select Midband/Highband and Digital Filter length.
2. Disable transmitters if desired by writing to Tone Frequency registers.
3. Prime the Notone timer by sending the required period byte.
4. Enable/disable interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt is set to the µC.
6. The µC examines the Status Register. If tone measurement is complete, it reads in the RX Tone Frequency in the form N + R (Figure 6).
7. RX Tone Measurement Complete interrupts are periodically sent to the µC unless Notone is detected, in which case a Notone Interrupt is sent.

5.5.2 Transmit Sequence

1. Set Tone Frequency Generators to Notone during the transmitter initialization period.
2. Send Control Command for TX: Select Sum/Switched Sum Out and Audio Switch states.
3. Send General Purpose (GP) Timer information for the Notone transmitter initialization period. This will initiate the timer.
4. Enable/disable interrupts as desired.
5. µC waits for "GP Timer Expired," reads the Status Register to check interrupts due to timer, and resets the Status Bit. If required, the µC sends the next timer period followed by the next tone(s) frequency information. A new timer period sent will reset the timer, otherwise the timer is self-resetting.
6. The µC monitors the interrupts and repeats steps 5 and 6 as required.
7. After last loaded tone, µC turns off Tone Generator(s).

5.6 General Reset

Upon power-up the bits in the MX803A registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to reset all microcircuits on the C-BUS. It has the following effect on the MX803A:

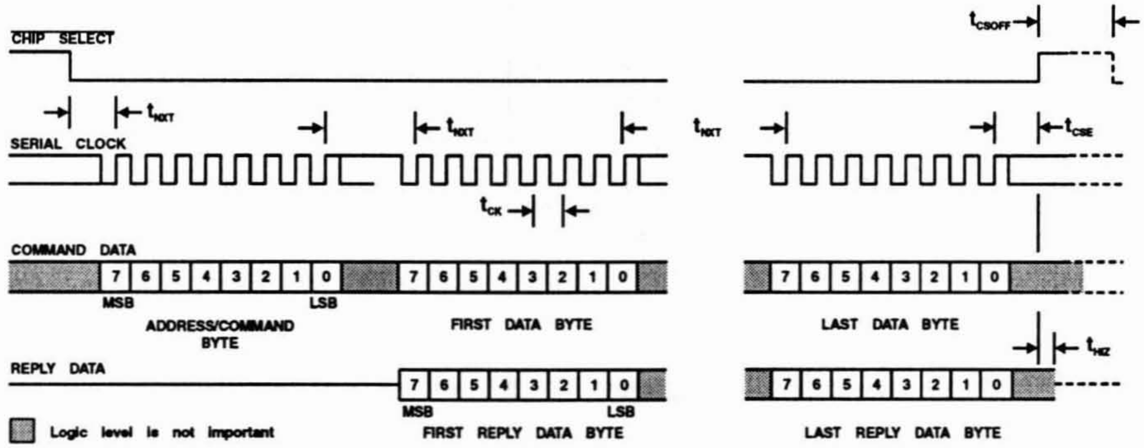
Control Register	Set as 00_H
Status Register (bits 0, 1, 2)	Set as 00_H
Notone Timer	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen. Purpose Reg.	Set as 00_H

Table 10: General Reset effect on MX803A

This sets the MX803A to Encoder High Band (625Hz to 3000Hz) with interrupts disabled and both timers set to 00_H. Both timers should be set up before interrupts are enabled to prevent initial, undesired interrupts.

6. Timing Information

Figure 8 shows timing parameters for two-way communication between the µC and the MX803A on the C-BUS.



CHIP SELECT
t_{CSOFF}
SERIAL CLOCK
t_{NXT}
t_{NXT}
t_{NXT}
t_{CSE}
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
▨ Logic level is not important

Figure 8: C-BUS Timing

Parameter		Min	Typ	Max	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{CSOFF}	Chip Select High	2.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs
t_{CH}	Decoder or Encoder Clock High	500			ns
t_{CL}	Decoder or Encoder Clock Low	500			ns
t_{CDS}	Command Data Set-Up Time	250			ns
t_{CDH}	Command Data Hold Time	0			ns
t_{RDS}	Reply Data Set-Up Time	250			ns
t_{RDH}	Reply Data Hold Time	50.0			ns
t_{HIZ}	Chip Select High to Reply Data High - Z			2.0	µs

Table 11: Timing Information

Timing Information Notes

1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX803A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX803A and into the µC on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing µC serial interface formats, the MX803A will work with either polarity Serial Clock pulses.

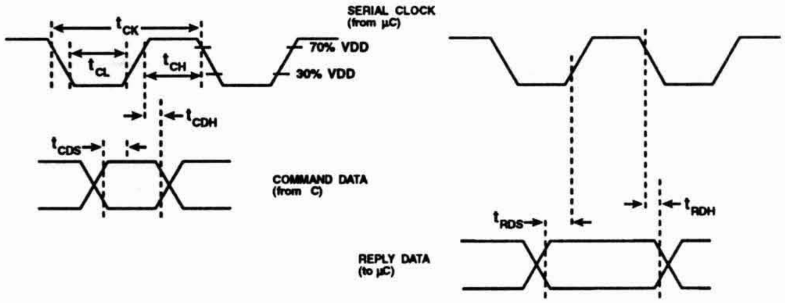


Figure 9: Timing Relationship for C-BUS Information Transfer

7. Performance Specification

7.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside of the operating limits is not suggested.

General	**Min.**	**Max.**	**Units**
Supply Voltage (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / J / LH Packages			
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C
Total allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		4.5	5.5	V
Temperature		-40	85	°C
Xtal/Clock Frequency			4.0	MHz

Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0 @ T_{AMB} = 25°C Xtal = 4MHz (refer to section 5.2.4.4 for Xtal Scaling factor)
Audio level 0dB ref. = 308mV_{RMS} @ 1kHz (60% deviation, FM)
Noise Bandwidth = 5.0kHz Band-Limited Gaussian

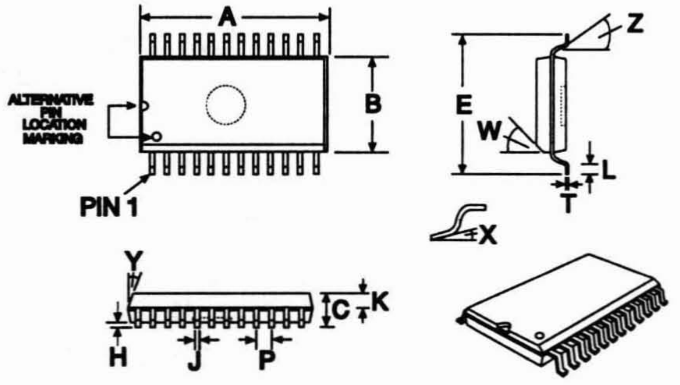
	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Decoder + Both Timers			2.0		mA
Decoder, Both Timers + One TX only			4.0		mA
All Functions Enabled			5.0		mA
Analog Impedance					
RX Audio Input			20.0		MΩ
Summing Amp Input			20.0		MΩ
Switch			1.0		kΩ
Tones 1 and 2 Outputs			10.0		kΩ
CAL/CUES Output			5.0		kΩ
Summing Outputs			10.0		kΩ
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5			V
Input Logic "0"	1			1.5	V
Output Logic "1" (I_{OH} = -120µA)	2	4.6			V
Output Logic "0" (I_{OL} = 360µA)	3			0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3			4.0	µA
Input Capacitance	1			7.5	pF
I_{OX} (V_{OUT} = 5V)	4			4.0	µA
Overall Performances					
RX - Decoding					
High Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			30.0	ms
Tone-to-Noise Ratio = 0dB	5,6,10			40.0	ms
Frequency					
Band		625		3000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%

	Notes	Min.	Typ.	Max.	Units
Mid-Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	7,10			60.0	ms
Tone-to-Noise Ratio = 0dB	6,7,10			80.0	ms
Frequency					
Band		313		1500	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
Extended Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			20.0	ms
Frequency					
Band		1250		6000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
TX - Encoders 1 and 2					
Tone Frequency		208		3000	Hz
Period ($1/f_{TONE}$) Error				1.0	µs
Tone Amplitude		-1.5		1.5	dB
Total Harmonic Distortion				5.0	%
Rise Time to 90%			$3/f_{TONE}$		ms
Fall Time to 10%	8			5.0	ms
Frequency Change Time			$3/f_{TONE}$		ms
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0		150	ms
Mid-Band		20.0		300	ms
RX Notone					
Timing Period Range					
Hi-Band		20.0		300	ms
Mid-Band		40.0		600	ms
Xtal/Clock Frequency (f_{XTAL})			4.0	6.0	MHz

Operating Characteristics Notes:

1. Device control pins: Serial Clock, Command Data, and $\overline{\text{CS}}$.
2. Reply Data output.
3. Reply Data and $\overline{\text{IRQ}}$ outputs.
4. Leakage current into the "Off" $\overline{\text{IRQ}}$ output.
5. Measurement period = 9.198ms.
6. Decode Probability = 0.993.
7. Measurement period = 18.396ms.
8. When set to Powersave.
9. For a good input signal.
10. Inversely proportional to Xtal frequency, i.e. Spec. x $\frac{4\text{MHz}}{f_{\text{XTAL}}}$. So, for a 6MHz clock a 30ms tone response time becomes 20ms.

7.2 Packaging

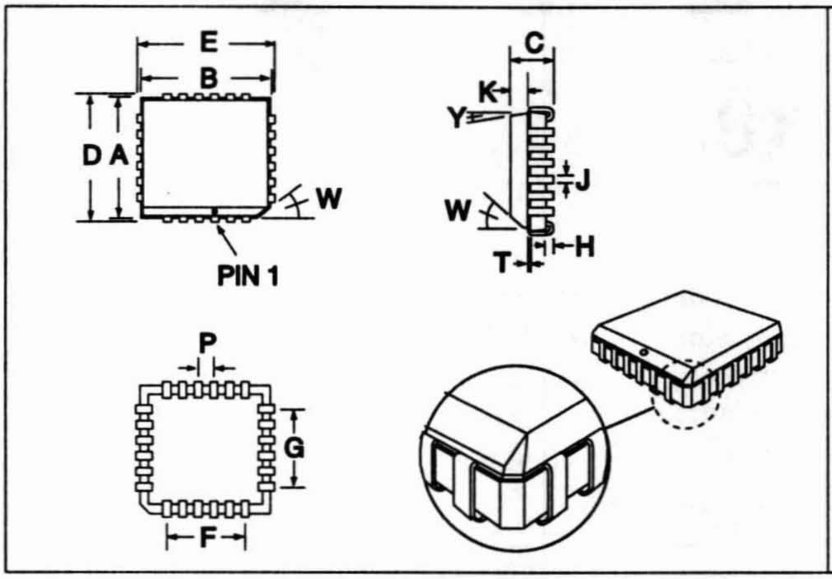


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin SOIC Mechanical Outline: order as part no. MX803ADW

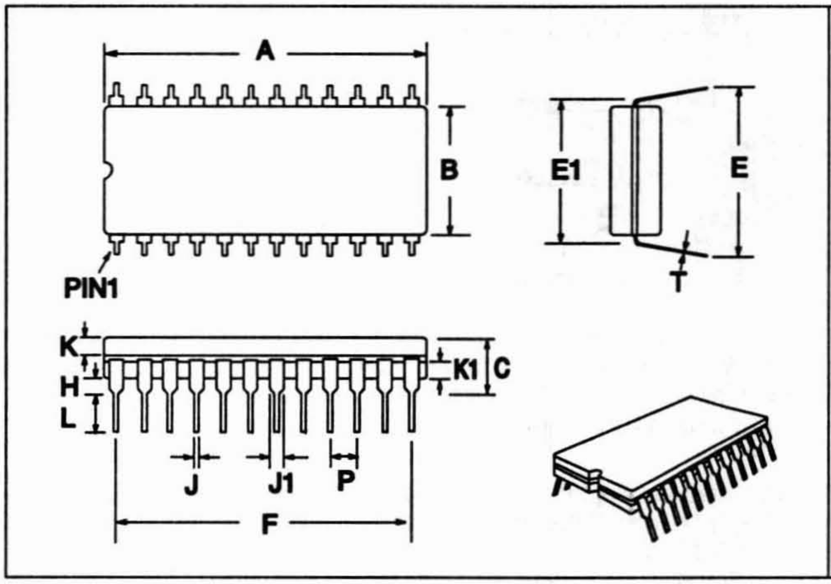


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PLCC Mechanical Outline: order as part no. MX803ALH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin CDIP Mechanical Outline: order as part no. MX803AJ

MX•COM, INC. MiXed Signal ICs

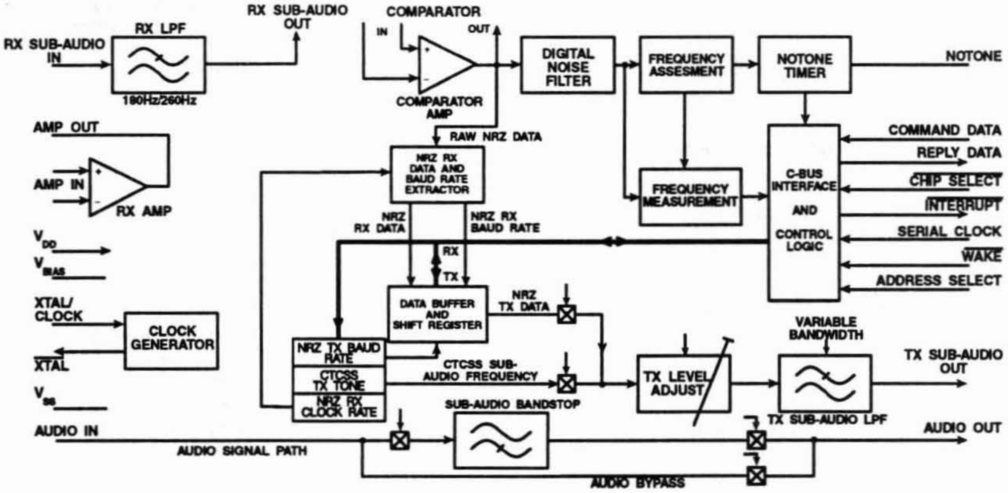
DATA BULLETIN

MX805A

Sub-Audio Signaling Processor

Features

- Non-predictive CTCSS Tone Decoder
- DCS Sub-Audio Signal demodulator
- CTCSS /NRZ Encoder with TX level adjustment and lowpass filter output stage with optional NRZ pre-emphasis
- Selectable Sub-Audio bandstop filter
- NoTone (CTCSS RX) period timer
- Low Power Operation
- Member of DBS800 Family (C-BUS Compatible)


RX SUB-AUDIO IN
RX LPF
180Hz/260Hz
RX SUB-AUDIO OUT
COMPARATOR
IN
OUT
COMPARATOR AMP
DIGITAL NOISE FILTER
FREQUENCY ASSESMENT
NOTONE TIMER
NOTONE
AMP OUT
AMP IN
RX AMP
RAW NRZ DATA
NRZ RX DATA AND BAUD RATE EXTRACTOR
NRZ RX DATA
NRZ RX BAUD RATE
FREQUENCY MEASUREMENT
C-BUS INTERFACE AND CONTROL LOGIC
COMMAND DATA
REPLY DATA
CHIP SELECT
INTERRUPT
SERIAL CLOCK
WAKE
ADDRESS SELECT
V_DD
V_BIAS
XTAL/ CLOCK
CLOCK GENERATOR
XTAL
V_SS
RX
TX
DATA BUFFER AND SHIFT REGISTER
NRZ TX DATA
NRZ TX BAUD RATE
CTCSS TX TONE
NRZ RX CLOCK RATE
CTCSS SUB-AUDIO FREQUENCY
TX LEVEL ADJUST
VARIABLE BANDWIDTH
TX SUB-AUDIO OUT
TX SUB-AUDIO LPF
SUB-AUDIO BANDSTOP
AUDIO IN
AUDIO SIGNAL PATH
AUDIO OUT
AUDIO BYPASS

The MX805A is a sub-audio frequency signaling processor that provides outband audio and digital signaling capability for LMR systems. Designed for the transmission and non-predictive reception of Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard frequencies, the MX805A also handles Non-Return-to Zero (NRZ) data reception and transmission to provide Digitally Coded Squelch (DCS/DPL™) and LTR™ signaling.

Setting the MX805A functions and modes is accomplished by data loaded from the microcontroller to the controlling registers within the device. Reply Data and Interrupt protocol keep the microcontroller up to date on the operational status of the circuitry. CTCSS tone data for transmission is generated in the microcontroller, loaded to the CTCSS TX Frequency Register, encoded and output as a tone via the TX Sub-audio LPF. Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data word, is presented to the microcontroller for matching against a lookup table. Noise filtering is provided to improve the signal quality prior to measurement. NRZ coded data streams for transmission, when generated within a microcontroller, are loaded to the NRZ TX Data Buffer and output, in 8-bit bytes, through the lowpass filter circuitry as subaudible signals. DCS turnoff tones can be added to the data signals by switching the MX805A to the CTCSS transmit mode at the appropriate time. NRZ coding is produced by the microcontroller and translated to subaudio signals by the MX805A. Received NRZ data is filtered, detected, and placed into the NRZ Data Register, which is then available for transfer (one byte at a time) to the microcontroller for decoding by software. Clock extraction circuitry is provided on-chip. TX ad RX baud rates are selectable.

Hardware and software are designed to allow consecutive addressing of two MX805A Sub-Audio Signaling Processors to achieve multi-mode duplex operation. Powersaving may be controlled by software or by an input dedicated to the purpose.

The MX805A may be used with a 5.0V power supply and is available in the following packages:
24-pin SOIC (MX805ADW), 24-pin PLCC (MX805ALH), and 24-pin PDIP (MX805AP).

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5.2.5 Write to CTCSS TX Frequency/NRZ Baud Data Rate Register –A/C 73_H ($7B_H$) followed by 2 bytes of Command Data. .... 3 - 506

5.2.6 Read NRZ RX Data Register – A/C 74_H ($7C_H$) followed by 1 byte Reply Data .... 3 - 508

5.2.7 Write to NRZ TX Data Register – A/C 75_H ($7D_H$) followed by 1 byte of Command Data. .... 3 - 508

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MXCOM, Inc. reserves the right to change specifications at any time without notice.

1 Block Diagram

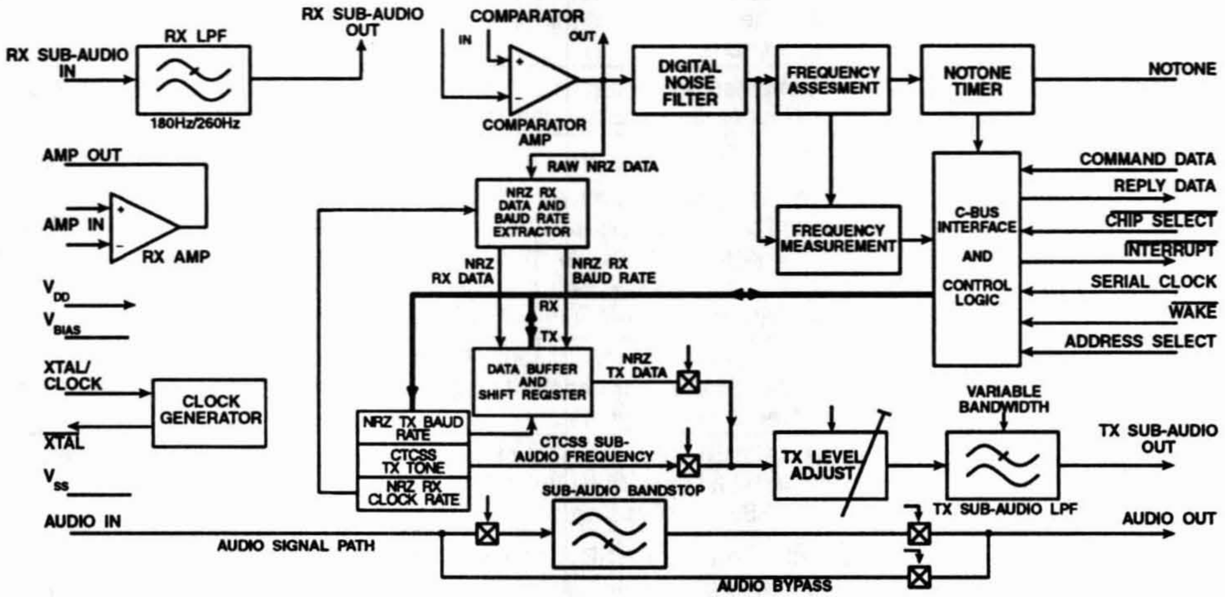

RX SUB-AUDIO IN
RX LPF
180Hz/260Hz
RX SUB-AUDIO OUT
COMPARATOR
IN
OUT
COMPARATOR AMP
DIGITAL NOISE FILTER
FREQUENCY ASSESMENT
NOTONE TIMER
NOTONE
RAW NRZ DATA
AMP OUT
AMP IN
RX AMP
NRZ RX DATA AND BAUD RATE EXTRACTOR
FREQUENCY MEASUREMENT
C-BUS INTERFACE AND CONTROL LOGIC
COMMAND DATA
REPLY DATA
CHIP SELECT
INTERRUPT
SERIAL CLOCK
WAKE
ADDRESS SELECT
NRZ RX DATA
NRZ RX BAUD RATE
RX
TX
V_DD
V_BIAS
XTAL/ CLOCK
CLOCK GENERATOR
XTAL
V_SS
DATA BUFFER AND SHIFT REGISTER
NRZ TX DATA
NRZ TX BAUD RATE
CTCSS TX TONE
NRZ RX CLOCK RATE
CTCSS SUB-AUDIO FREQUENCY
TX LEVEL ADJUST
VARIABLE BANDWIDTH
TX SUB-AUDIO OUT
TX SUB-AUDIO LPF
SUB-AUDIO BANDSTOP
AUDIO IN
AUDIO SIGNAL PATH
AUDIO OUT
AUDIO BYPASS

Figure 1: Block Diagram

2 Signal List

Pin	Signal	Description
1	$\overline{\text{Xtal}}$	The output from the on-chip clock oscillator inverter. External components are required at this input when a Xtal input is used. See Figure 2.
2	Xtal/Clock	The input to the clock oscillator inverter. A Xtal or externally derived clock should be connected here.
3	Address Select	This input enables two MX805A's to be used on the same C-BUS to provide dull-duplex operation. See Table 4 and Table 5.
4	$\overline{\text{IRQ}}$	$\overline{\text{Interrupt Request}}$. The output of this pin indicates an interrupt condition to the microcontroller by going to a logic '0". This 'wire-or-able' output allows the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin has a low impedance pulldown to logic '0' when active, and a high impedance when inactive. The system $\overline{\text{IRQ}}$ line requires 1 pull-up resistor to V_{DD}. The conditions that cause interrupts are indicated in the Table 5 and Table 7.
5	Serial Clock	This is the 'C-BUS' serial Clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MX805A. See timing diagrams.
6	Command Data	This is the 'C-BUS' serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first and LSB (bit 0) last, synchronized to the Serial Clock. See Timing diagrams.
7	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$. This is the 'C-BUS' data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing diagrams.
8	Reply Data	This is the 'C-BUS' serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{\text{CS}}$ input. This 3-state output is held at high impedance when not sending data to the microcontroller. See Timing Diagrams
9	TX Sub-Audio Out	This is the subaudio output (pure or NRZ derived). Signals are band limited. The TX Output Filter had a variable bandwidth (See Table 9). This output is at V_{BIAS} (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the MX805A is placed in the Powersave All condition.
10	Audio In	This is the input to the switched sub-audio bandstop (highpass) filter. It is internally biased, and should be AC coupled by capacitor C7.
11	Audio Out	This is the output of the audio signal path (filter or bandpass). It is controlled by the Control Register. When disabled, the pin is held at V_{BIAS}.
12	V_{SS}	Negative Supply (GND)
13	RX Amp In (-)	This is the inverting input to the on-chip RX Input Amp. (See Figure 2, Figure 3, and Figure 4).
14	RX Amp In (+)	This is the non-inverting input to the on-chip RX Input Amp.
15	RX Amp Out	This is the output of the on-chip RX Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and anti-aliasing filter prior to the RX Lowpass Filter, or for other purposes. See Figure 2 for Component details.
16	RX Sub-Audio In	This is the received Sub-Audio (CTCSS/NRZ) input. It is internally referenced to V_{BIAS}. This signal to this pin should be AC coupled or biased. See Figure 2.
17	RX Sub-Audio Out	This is the output of the RX lowpass filter. It may be coupled into the on-chip amplifier or comparator as required.
18	V_{BIAS}	The internal circuitry bias line, held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C8. See Figure 2.
19	Comparator In (-)	This is the inverting input to the on-chip 'comparator' amplifier. See Figure 2, Figure 3, and Figure 4.
20	Comparator In (+)	This is the non-inverting input to the on-chip 'comparator' amplifier. See Figure 2, Figure 3, and Figure 4.

<table>
<tr><th>Pin</th><th>Signal</th><th>Description</th></tr>
<tr><td>21</td><td>Comparator Out</td><td>This is the output of the 'comparator' amplifier. This node is also connected internally to the input of the /digital Noise Filter (See Figure 1). When both decoders (CTCSS or NRZ) are powersaved, this output is at a logic '0'.</td></tr>
<tr><td>22</td><td>Notone Timing</td><td>External RC components connected to this pin form the timing mechanism of a Notone period timer. The external network determines the "charge rate" of the timer to V_{BIAS}. The expiration of the timer will cause an interrupt. This function is only used in the CTCSS RX mode. See page 9.</td></tr>
<tr><td>23</td><td>$\overline{\text{Wake}}$</td><td>This 'real time' input can be used to reactivate the MX805A from the 'Powersave All' condition using an externally derived signal. The MX805A will be in 'Powersave All' condition when both this pin and bit 0 of the Control Register are set to a logic '1'. Recovery from 'Powersave All' is achieved by putting either the $\overline{\text{Wake}}$ pin or the 'Powersave All" bit at logic '0'. This allows MX805A activation by the microcontroller or an external signal, such as RSSI or Carrier Detect.</td></tr>
<tr><td>24</td><td>V_{DD}</td><td>Positive Supply. A single 5.0V regulated supply is required.</td></tr>
<tr><td colspan="3">Note: More information on external components and the DBS800 system integration of the MX805A are contained in the DBS800 System Support Documentation. Guidance on the generation and manipulation of NRZ and RX and TX data is given in the DBS800 Application support documentation.</td></tr>
<tr><td colspan="3">C-BUS: This is MX-COM's proprietary standard for the transmission of commands and data between a microcontroller and DBS8000 microcircuits. It may be used with any microcontroller, and can, if desired, take advantage of the hardware and serial I/O functions embodied into many types of microcontroller. The C-BUS data rate is determined by the microcontroller.</td></tr>
</table>

Table 1: Signal List

RX CTCSS Tone Measurement Completed
CTCSS NOTONE Timer Expired
1 NRZ RX Data Byte Received
New NRZ Data Received Before Last Byte Read
NRZ TX Buffer Ready
NRZ Data Transmission Complete

Table 2: Interrupt Conditions

3 External Components

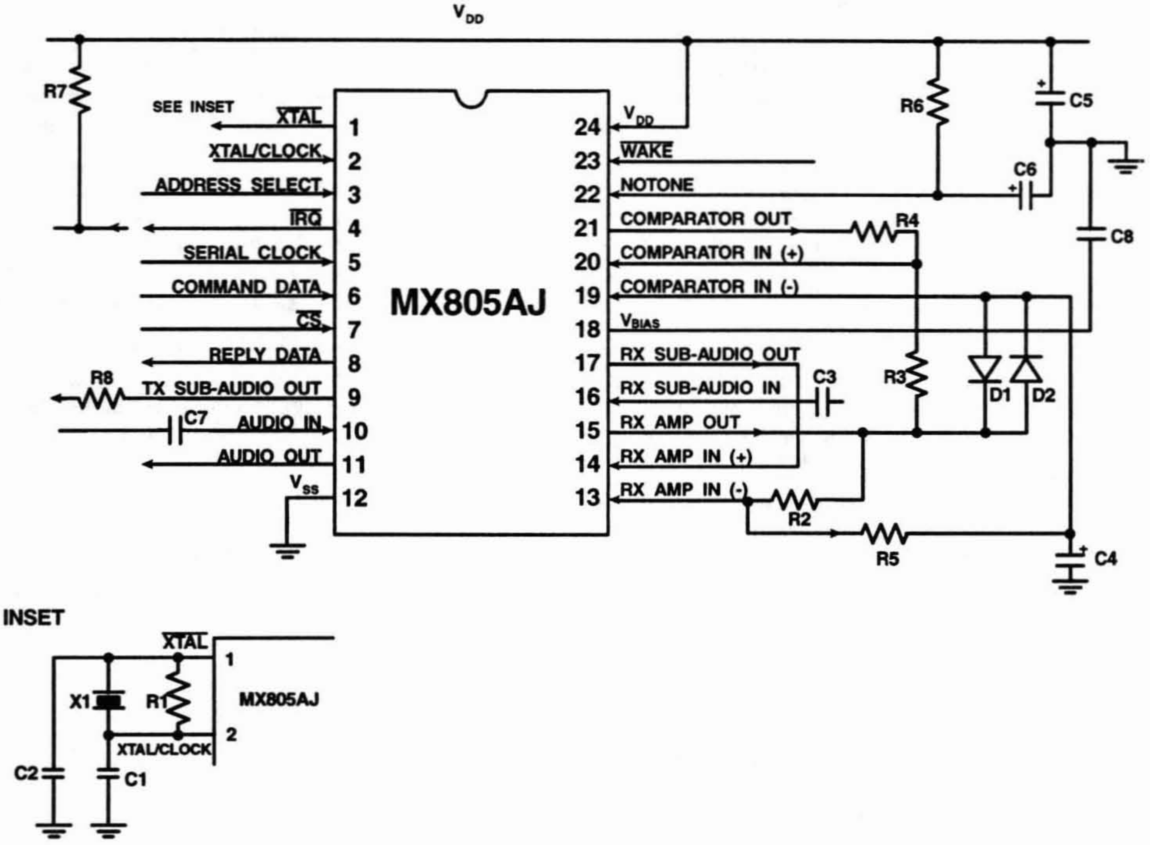

VDD
R7
SEE INSET
XTAL
XTAL/CLOCK
ADDRESS SELECT
IRQ
SERIAL CLOCK
COMMAND DATA
CS
REPLY DATA
R8
TX SUB-AUDIO OUT
C7
AUDIO IN
AUDIO OUT
VSS
1
2
3
4
5
6
7
8
9
10
11
12
MX805AJ
24
23
22
21
20
19
18
17
16
15
14
13
VDD
WAKE
NOTONE
COMPARATOR OUT
COMPARATOR IN (+)
COMPARATOR IN (-)
VBIAS
RX SUB-AUDIO OUT
RX SUB-AUDIO IN
RX AMP OUT
RX AMP IN (+)
RX AMP IN (-)
R6
C5
C6
R4
C8
C3
R3
D1
D2
R2
R5
C4
INSET
XTAL
X1
R1
1
2
MX805AJ
XTAL/CLOCK
C2
C1

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	5	1.0MΩ	±5%
R2	4	360kΩ	±5%
R3	1	10.0kΩ	±5%
R4	4	150kΩ	±5%
R5	4	100kΩ	±5%
R6		150kΩ	±5%
R7	6	22.0kΩ	±5%
R8	2	360kΩ	±5%
C1	5		
C2	5		

Component	Notes	Value	Tolerance
C3		1.5µF	±20%
C4		15.0µF, 6V Tant.	±20%
C5		1.0µF, 10V Tant.	±20%
C6		1.0µF, 10V Tant.	±20%
C7		0.1µF, 25V x 7R	±20%
C8		1.0µF	
D1	8		
D2	8		
X1		4.00MHz	

Table 3: Recommended External Components

Recommended External Component Notes:

1. Xtal/Clock circuitry shown in inset are recommended in accordance with the MX-COM's "Standard and DBS 800 Crystal Oscillators" application note.
2. Resistor R8 is a System Component. Its value is chosen together with the MX806A Modulation Summing Amplifier to provide a subaudio signal level of −11.0dB to the system modulator.
3. Figure 3 and Figure 4 illustrate alternative input component configurations.
4. The values for R2 and R5 are dependent on the input signal level. Values given are for the specified composite signal (reference page 14). R4 add hysteresis to the comparator and is not always required.
5. The values used for C1 and C2 are determined by the frequency of X1.

   As a guide: $C1 = C2 = 33pF$ for $X1 < 5.0MHz$
   $C1 = C2 = 18pF$ for $X1 > 5.0MHz$

   If the on-chip Xtal oscillator is to be used, then the external components X1, C1, C2, and R1 are required as shown in Figure 2 (inset). If an external clock source is used these components are not required; the input should be connected to the Xtal/Clock pin and the $\overline{\text{Xtal}}$ pin unconnected.
6. Resistor R7 is used as the DBS800 system common pull-up for the C-BUS Interrupt Request ($\overline{\text{IRQ}}$) line. The optimum value of this component will depend upon the circuitry connected to the $\overline{\text{IRQ}}$ line.
7. The level at this point should be approximately $900mV_{P-P}$.
8. Silicon small signal

3.1 Input Configurations

Figure 3 shows an input configuration that is generally for use for CTCSS signal and NRZ data reception.

Input coupling capacitor C3 is required because the RX Sub-Audio Input is held at V_{BIAS} during all powered conditions of the MX805A. Diodes D1 and D2 can be any silicon small signal diode.

The output resistance (open loop) of the on-chip Rx Amp is = 6kΩ. In the configuration shown in Figure 3, the (Rx Amp) RC time constant is therefore 90ms. If this period is too long for some systems, i.e. those using half duplex, short data burst, and external amplifier should be considered in place of the on-chip Rx Amp.

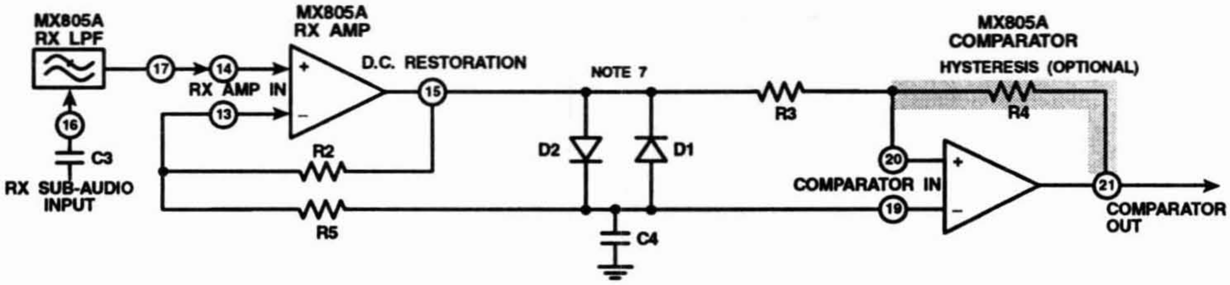


Figure 3: MX805A Input Components

3.1.1 Using and External Op-Amp

For DC coupling the MX805A to the receiver's discriminator output when using burst mode NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will quickly compensate for sudden shift of DC input bas.

Components R9, R10, and R11, should be calculated to provide an accurate potential of 2.5VDC (equal to V_{BIAS}) at pin junction 15/16when using a discriminator input and 900mVP-P at the output of the external op-amp. Note that the MX805A LPF has a 6dB gain. If additional filtering is required, C9 should be used, it should be calculated with R9 to provide a lowpass cutoff frequency (f_{CO}) of 500Hz.

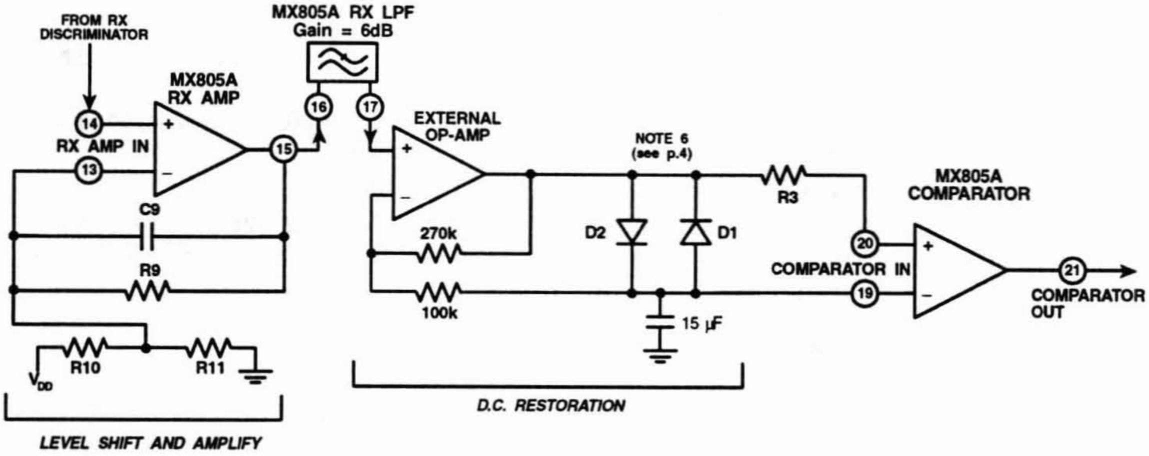

FROM RX DISCRIMINATOR
MX805A RX AMP
14
RX AMP IN
13
15
C9
R9
R10
R11
VDD
LEVEL SHIFT AND AMPLIFY
MX805A RX LPF
Gain = 6dB
16
17
EXTERNAL OP-AMP
270k
100k
NOTE 6 (see p.4)
D2
D1
15 µF
D.C. RESTORATION
R3
MX805A COMPARATOR
20
COMPARATOR IN
19
21
COMPARATOR OUT

Figure 4: MX805A Input Components using and External Op-Amp

4 General Description

4.1 Glossary

DCS	Continuous Digitally Coded Squelch
CTCSS	Continuous Tone Controlled Sub-Audio Squelch
DPL™	Digital Private Line
LTR™	Logic Trunked Radio
NRZ	Non-Return-to-Zero
f_{CO}	Filter Cutoff frequency
$f_{CTCSS\ IN}$	Sub-Audio Rx frequency
$f_{CTCSS\ OUT}$	Sub-Audio Tx frequency
f_{TONE}	Tone frequency
f_{XTAL}	Xtal/Clock frequency
R_{NRZRX}	NRZ RX baud rate
R_{NRZTX}	NRZ TX baud rate
s_{INPUT}	Audio input signal.

4.2 Operating Modes

4.2.1 NRZ Encoding

The NRZ Encoder is formed by a shift register and the TX Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ Tx Data Register. The output data level may be adjusted and filtered. Data may be pre-emphasized via a C-BUS command. The expected Rx baud rate is programmed as the NRZ Tx Baud Rate (R_{NRZTX}). See Table 8

4.2.2 CTCSS Encoding

The CTCSS Tone Encoder is comprised of a clock divider programmed by an 11-bit binary number (Q) loaded to the CTCSS Tx Frequency Register (See Table 8) via the C-BUS Command Data line.

The square-wave output of the encoder is fed through the Tx Level Adjust variable gain block to the Tx Sub-Audio lowpass filter, a variable gain bandwidth circuit controlled by 4-bits (P) if the CTCSS Tx Frequency Register. The Tx Sub-Audio output is a sine-wave. Standard and nonstandard sub-audio tones are available. A CDCS turnoff tone may also be generated.

4.2.3 NRZ Decoding

Input (NRZ type) sub-audio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output on 8-bit byte at a time as Reply Data from the NRZ Rx Data Register to the microcontroller. The expected Rx baud rate is programmed as the NRZ Rx Baud Rate (R_{NRZRX}). See Table 8. Any codeword recognition can be carried out by software.

4.2.4 CTCSS Decoding

Received CTCSS signals are filtered, and coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle–to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64ms (4.0MHz crystal).

If the average signal quality is consistently too low, NoTone is indicated; if not the input frequency is precisely indicated in the CTCSS Rx Frequency Register in a binary form.

Any single sub-audio tone within the specified range may be selected, enabling a DCS turnoff tone of 134Hz) to be decoded while in the NRZ Rx mode.

5 Controlling Protocol

Control of the MX805A Sub-Audio Signaling Processor's operation is by communications between the microcontroller and the MX805A internal registers on the C-BUS, using Address/Commands (A/Cs) and appended instructions or data (See Figure 10). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select Input enables the addressing of 2 separate MX805As on the C-BUS to provide full-duplex signaling.

5.1 MX805A Internal Registers

5.1.1 Control Register (70_H/78_H)

Write only, control and configuration of the MX805A.

5.1.2 Status Register (71_H/79_H)

Read only, reporting of device functions.

5.1.3 CTCSS Rx Frequency Register (72_H/$7A_H$)

Read only, a 2-byte binary word indicating the frequency of the received sub-audio input.

5.1.4 CTCSS Tx Frequency/NRZ Tx or Rx Baud Rate Register (73_H/$7B_H$)

Write only, a 2-byte command to set the relevant parameters.

5.1.5 NRZ Rx Data Register (74_H/$7C_H$)

Read only, a single byte f received NRZ data.

5.1.6 NRZ Tx Data Register (75_H/$7D_H$)

Write only, to load a single byte of NRZ data for transmission.

5.1.7 Gain Set Register (76_H/$7E_H$)

Write only, a single byte to set the gain of the Tx Lowpass Filter.

5.2 Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data

(ii) a Status or data Reply

Instructions and data are loaded and transferred, via C-BUS, in accordance with the timing information in Figure 9 and Figure 11.

Placing the Address Select input at a logic "0" will address MX805A #1, a logic "1" will address MX805A #2.

Table 4 and Table 5 show the list of A/C bytes relevant to the MX805A

Command Assignment	Address/Command (A/C) byte		Data Bytes
	Hex	Binary	
		MSB LSB	
General Reset	01	00000001	
Write to Control Register	70	01110000	+1 byte instruction to Control Register
Read Status Register	71	01110001	+1 byte reply from Status Register
Read CTCSS Rx Freq. Reg.	72	01110010	+2 byte reply of CTCSS Rx Data
Write to CTCSS Tx Freq./NRZ Baud Rate Reg.	73	01110011	+2 byte instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	74	01110100	+1 byte binary data Reply
Write to NRZ Tx Data Reg.	75	01110101	+1 byte binary data Command
Write to Gain Set Reg.	76	01110110	+1 byte instruction for Tx Output

Table 4: MX805A #1 C-BUS Address/Commands – (Address Select input at a logic "0")

Command Assignment	Address/Command (A/C) byte		Data Bytes
	Hex	Binary	
		MSB LSB	
General Reset	01	00000001	
Write to Control Register	78	01111000	+1 byte instruction to Control Register
Read Status Register	79	01111001	+1 byte reply from Status Register
Read CTCSS Rx Freq. Reg.	7A	01111010	+2 byte reply of CTCSS Rx Data
Write to CTCSS Tx Freq./NRZ Baud Rate Reg.	7B	01111011	+2 byte instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	7C	01111100	+1 byte binary data Reply
Write to NRZ Tx Data Reg.	7D	01111101	+1 byte binary data Command
Write to Gain Set Reg.	7E	01111110	+1 byte instruction for Tx Output

Table 5: MX805A #2 C-BUS Address/Commands – (Address Select input at a logic "1")

5.2.1 Write to Control Register - A/C 70H (78H) followed by 1 byte of Command Data

Table 6 shows the configurations available to the MX805A. Bits 5, 6, and 7 are used together to Enable and Powersave circuits sections as required.

Setting			**Control Bits**	
MSB			**Transmitted First**	
7	**6**	**5**	**Enabled**	**Powersaved**
0	0	0	CTCSS Decoder	NRZ Decoder and Both Encoders
0	0	1	NRZ Decoder	CTCSS Decoder and Both Encoders
0	1	0	CTCSS Encoder	All Decoders
0	1	1	NRZ Encoder	All Decoders
1	0	0	CTCSS Encoder and Decoder	NRZ Encoder and Decoder
1	0	1	NRZ Encoder and CTCSS Decoder	No circuits
1	1	0	NRZ Decoder and CTCSS Decoder	All Encoders
1	1	1	NRZ Decoder	All Encodes except Tx Sub-Audio LPF and CTCSS Decoder
4				
1			Enable Audio Output – Used with Bit 3	
0			Disable Audio Output – output to V_{BIAS}	
3				
1			Enable Sub-Audio Bandstop Filter (Audio Signal Path)	
0			Bypass Sub-Audio Bandstop Filter	
2				
1			Enable All MX805A Interrupts	
0			Disable All MX805A Interrupts	
1				
1			Set Rx Lowpass Filter Bandwidth to 180Hz – for low CTCSS tones or NRZ Data	
0			Set Rx Lowpass Filter Bandwidth to 260Hz	
0				
1			All encoders and Decoders Powersaved	
0			All Encoders and Decoders Enabled unless individually Powersaved	

Table 6: Control Register

5.2.2 General Reset

Upon power-up the bits in the MX805A registers will be random (either 0 or 1). A General Reset Command (01_H) will be required to reset all devices on the C-BUS. It has the following effect on the MX805A:

Control Register	Set to 00_H
Status Register	Set to 00_H
NoTone Timer	Discharged

Warning: The following MX805A register configurations are not affected by a General Rest Command:

CTCSS Rx Frequency
CTCSS Tx Frequency/NRZ Baud Rate Register
NRZ Rx Data Register
NRZ Tx Data Register
Gain Set Register

Note: Setting the Control Register in this way will set the MX805A to the CTCSS decode mode and overwrite a "Powersave All" instruction. It should also be considered that a General Reset command will reset All DBS800 ICs operating on the C-BUS.

5.2.3 Read Status Register –A/C 71_H (79_H) followed by 1 byte of Rely Data.

The Status Register indicates the operational condition of the MX805A. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status bit is set to a logic "1", and Interrupt Request (IRQ) output is generated. A read of the Status Register will reset the Interrupt and ascertain the state of this register. Table 7 shows the conditions indicated by the Status bits.

Setting	Set By	Logic	Cleared By	Logic
MSB	Received First			
7, 6	Not Used	0	Not Used	0
5	NRZ data transmission complete. No new data is loaded.	1	1. Write to NRZ Data Reg., or 2. General Reset, or 3. NRZ Encoder Powersave	0
4	NRZ TX Data Buffer ready for next data byte.	1	1. Write to NRZ TX Data Reg., or 2. General Rest, or 3. NRZ TX Powersave	0
3	New NRZ RX data received before last byte was read.	1	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder powersave	0
2	1 byte of NRZ data received	1	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder powersave	0
1	NoTone timer period expired	1	1. Read Status Register, or 2. General Rest, or 3. CTCSS Decoder Powersave	0
0	RX Tone Measurement Complete	1	1. Read Status Register, or 2. General Reset, or 3. CTCSS Decoder Powersave	0

Table 7: Status Register

5.2.4 Read CTCSS RX Frequency Register –A/C 72_H ($7A_H$) followed by 2 bytes of Reply Data

5.2.4.1 Measurement of CTCSS RX Frequency ($f_{CTCSS\ IN}$)

The input sub-audio signal ($f_{CTCSS\ IN}$) is filtered, doubled and measured in the Frequency Counter over the "measurement period" (122.64ms) (4.0MHz Xtal).

The measuring function counts the number of complete input cycles occurring within the measurement period and the number of measuring-clock cycles necessary to make up one period.

When the measurement period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The CTCSS RX Frequency Register will now indicated the sub-audio signal frequency ($f_{CTCSS\ IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.

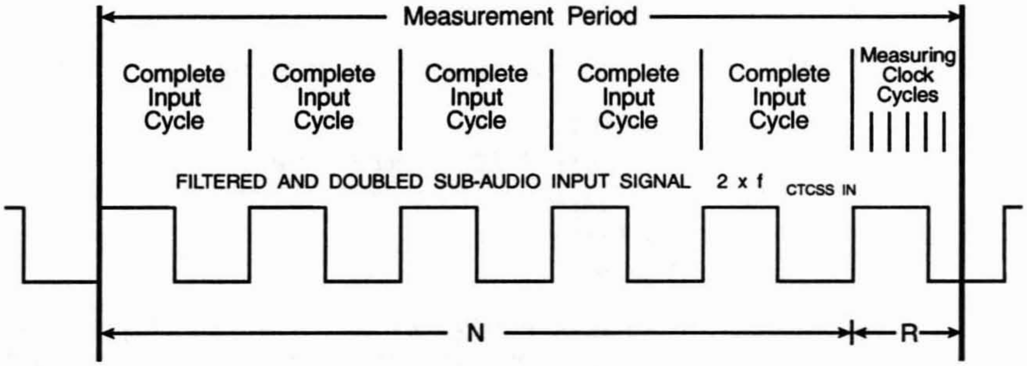


Figure 5: Measurement of a CTCSS RX Frequency

5.2.4.1.1 The Integer (N) –Byte 1

The binary number representing twice the number of cmplete input sub-audio cycle periods counted during the measurement period of 122.64ms (4.0MHz crystal)

5.2.4.1.2 The Remainder (R) –Byte 0

A binary number representing the remainder part, R, of 2x the Sub-Audio Input Frequency. R = number of specified measuring-clock cycles required to complete the specified measurement period (See N). The clock cycle frequency is 4166.6Hz (4.0MHz crystal)

(Reply Data)
(MSB) - Transmitted First

(Reply Data)
(LSB) - Transmitted Last

Byte 1								Byte 0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	"0"	← Integer (N) →						"0"	"0"	← Remainder (R) →					

CTCSS RX Frequency Register

Figure 6: Format of the CTCSS RX Frequency Register

5.2.4.2 CTCSS RX Frequency Register

The format of the CTCSS RX Frequency Register is shown in Figure 6.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of $N = 16 \le N \le 61$ i.e. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) are used to represent the Remainder (R). From Byte 0, valid values of $R \le 31$. This register is not affected by the General Reset command (01H) and may adopt any random configuration at Power-UP.

5.2.4.3 CTCSS RX Frequency Measurement Formulas

To assist in the production of "lookup" tables and limit-values in the microcontroller, and to provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulas show the derivation of the CTCSS RX Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

5.2.4.3.1 $f_{CTCSS\ IN}$

In the measurement period of 122.64ms there are N cycles at 2 x $f_{CTCSS\ IN}$ and R clcok cycles at 4166.6Hz, for any input frequency.

$$f_{CTCSS\,IN} = \frac{N \times f_{XTAL}}{1920 \times (511 - R)}$$

$$N = INT\left[\frac{1920 \text{ x } 511 \text{ x} f_{CTCSS\,IN}}{f_{XTAL}}\right]$$

$$R = INT\left[511 - \left(\frac{N \text{ x } f_{XTAL}}{1920 \text{ x } f_{CTCSS\,IN}}\right) + .5\right]$$

Calculate N first
Example: (f_{XTAL} = 4.00Mhz): $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

5.2.4.4 NoTone Timing

The input sub-audio signal is monitored by the Frequency Assessment Circuitry. Before any NoTone action is enabled, the MX805A must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the NoTone timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (NoTone Timer Expired) are generated. This is a one-shot function which is rest by a "Tone Measurement Complete" interrupt.

5.2.5 Write to CTCSS TX Frequency/NRZ Baud Data Rate Register –A/C 73$_H$ (7B$_H$) followed by 2 bytes of Command Data.

The information loaded to this register will set either the:

(a) CTCSS TX Tone Frequency	$f_{CTCSS\ OUT}$
(b) NRZ TX Baud Rate	$R_{NRZ\ TX}$
(c) NRZ RX Baud Rate	$R_{NRZ\ RX}$

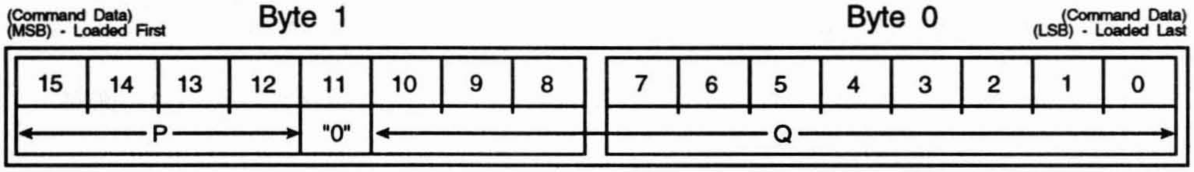
The chosen mode for this register (a, b, or c) is determined by the MX805A modes enabled by the Control Register, as shown in Table 8.

Control Register Bits			MX805A Mode Enabled	CTCSS TX/NRZ Baud Rate Register Function
7	6	5		
0	0	0	CTCSS Decode	
0	0	1	NRZ Decode	NRZ RX Baud Rate
0	1	0	CTCSS Decode	CTCSS TX Frequency
0	1	1	NRZ Encode	NRZ TX Baud Rate
1	0	0	CTCSS Encode and Decode	CTCSS TX Frequency
1	0	1	NRZ Encode & CTCSS Decode	NRZ TX Baud Rate
1	1	0	NRZ & CTCSS Decode	NRZ RX Baud Rate
1	1	1	NRZ Decode	NRZ RX Baud Rate

Table 8 CTCSS Frequency/NRZ Baud Rate Register Configurations

5.2.5.1 Data Format

Data is transmitted to this register as 2 bytes of Command Data in the form illustrated in the diagram below. This register is not affected by the General Rest Command (01H) and may adopt any random configuration at power-up.



CTCSS TX Frequency/NRZ Baud Rate Register

Figure 7: Format of the CTCSS TX Frequency/NRZ Baud Rate Register

5.2.5.2 Command Words P and Q

The two words, P and Q, loaded to this register are interpreted as:

P = *a binary number to set the TX Sub-Audio Lowpass filter bandwidth (applicable to NRX and CTCSS modes).*

Q = *A binary number to set the frequency r baud rate of the selected functon.*

5.2.5.2.1 Command Word P

Bits		LSB			
15	**14**	**13**	**12**	**P**	**LPF Bandwidth**
0	0	1	0	2	300Hz
0	0	1	1	3	200Hz
0	1	0	0	4	150Hz
0	1	0	1	5	120Hz
0	1	1	0	6	100Hz
0	1	1	1	7	85.7Hz
1	0	0	0	8	75Hz

Table 9: Valid Values of P

Bits 12 to 15 are used to produce the data word "P" as shown in Table 9. The cutoff frequency $f_{C/O}$ (0.5dB point) of the TX Sub-Audio Lowpass filter is calculated as:

$$f_{C/O} = \frac{f_{XTAL}}{32 \times 208.33 \times P}$$

$$P = \frac{f_{XTAL}}{32 \times 208.33 \times f_{C/O}}$$

Table 9 is provided as and example and calculated using a Xtal/Clock (f_{XTAL}) frequency of 4.00MHz. As illustrated, only values of "P" of 2 to 8 are usable

5.2.5.2.2 Command Word Q

Bits 0 to 10 (See Figure 7) are used to produce the data word "Q" which sets one of the parameters described below. As you can see, Command Word "Q" could be used to produce a parameter outside that specified in the "Characteristics" section of this data bulletin. Care should be taken not to do this. Examples for limits of "Q" in each operational configuration are included. "Q" = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0".

(a) CTCSS TX Tone Frequency ($f_{CTCSS\ OUT}$)

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times \text{"Q"}}\text{Hz}$$

$f_{CTCSS\ OUT}$ = 67Hz

So "Q" = 1866 "11101001010"

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}}\text{Hz}$$

$f_{CTCSS\ OUT}$ = 250Hz

So "Q" = 500 "00111110100"

(b) NRZ TX Baud Rate ($R_{NRZ\ TX}$)

$$R_{NRZ\ TZ} = \frac{f_{XTAL}}{32 \times \text{"Q"}}\text{bits/sec}$$

$R_{NRZ\ TX}$ = 67bits/sec

So "Q" = 1866 "11101001010"

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times R_{NRZ\ TZ}}$$

$R_{NRZ\ TX}$ = 300bits/sec

So "Q" = 417 "00110100001"

(c) NRZ RX Baud Rate ($R_{NRZ\ RX}$)

$$R_{NRZ\ RX} = \frac{f_{XTAL}}{32 \times 11 \times \text{"Q"}}\text{bits/sec}$$

$R_{NRZ\ RX}$ = 67bits/sec

So "Q" = 114 "00001110010"

$$\text{so "Q"} = \frac{f_{XTAL}}{352 \times R_{NRZ\ RX}}$$

$R_{NRZ\ RX}$ = 300bits/sec

So "Q" = 38 "00000100110"

5.2.6 Read NRZ RX Data Register – A/C 74_H ($7C_H$) followed by 1 byte Reply Data

Received NRZ data bits are organized into bytes and made available to the microcontroller via the Reply Data line. As 8 bits are received into this register and interrupt is generated to indicate that a complete byte has been received. This byte must be read before the arrival of the last (8th) bit of the next incoming byte. If this in not done, an interrupt to indicate this condition will be generated and the previous RX data is discarded. See Table 7.

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host microcontroller. The RX baud rate is set by writing to the CTCSS TX Frequency/NRZ Baud Rate Register (73_H/$7B_H$). The first bit received is the first bit sent to the microcontroller.

This register is not affected by the General Reset Command (01H), and may adopt random configuration at Power-Up.

5.2.7 Write to NRZ TX Data Register – A/C 75_H ($7D_H$) followed by 1 byte of Command Data.

A byte for transmission is loaded from the C-BUS Command Data line with the A/C. The first data bit received via the C-BUS is transmitted first. The transmitter operation is non-inverting.

The first data byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ TX Data Buffer is ready for the next data byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the TX Sub-Audio Output is placed at V_{BIAS}, and a interrupt is generated if the next byte is not loaded within 7 bit periods. See Table 7.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

5.2.8 Write to Gain Set Register – A/C 76_H ($7E_H$) followed by 1 byte of Command Data

5.2.8.1 Gain Set Register Settings:

The settings of this register control the CTCSS and NRZ signal level that is presented at the TX Sub-Audio Output.

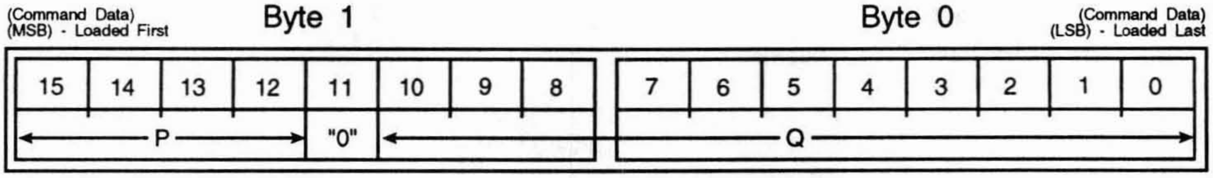
Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ TX Data by increasing the gain of the data bit before a level change (See Figure 8), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater that that set by Bits 0 to 2. If the TX Sub-Audio Output level is set to +2.58dB, the pre-emphasis level will be +4.3dB.

The pre-emphasis function will remain enabled until disabled by setting Bit 3 to a logic "0". If this function remains enabled when using the CTCSS Encoder, the output signal may be adversely affected. Therefore this function should be enabled when in the NRZ Encode mode.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

<table>
<tr><th colspan="12">Setting</th><th>Gain Setting</th></tr>
<tr><td colspan="12"></td><td></td></tr>
<tr><td colspan="3">7</td><td colspan="3">6</td><td colspan="3">5</td><td colspan="3">4</td><td>Transmitted Bit 7 First</td></tr>
<tr><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td><td></td></tr>
<tr><td colspan="12">3</td><td>Pre-Emphasis Setting</td></tr>
<tr><td colspan="12">1</td><td>1.72dB Gain Enabled</td></tr>
<tr><td colspan="12">0</td><td>1.72dB Gain Disabled</td></tr>
<tr><td colspan="4">2</td><td colspan="4">1</td><td colspan="4">0</td><td>Tx Level Adjust Gain Setting</td></tr>
<tr><td colspan="4">0</td><td colspan="4">0</td><td colspan="4">0</td><td>-2.58dB</td></tr>
<tr><td colspan="4">0</td><td colspan="4">0</td><td colspan="4">1</td><td>–1.72dB</td></tr>
<tr><td colspan="4">0</td><td colspan="4">1</td><td colspan="4">0</td><td>–0.86dB</td></tr>
<tr><td colspan="4">0</td><td colspan="4">1</td><td colspan="4">1</td><td>0dB</td></tr>
<tr><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">0</td><td>+0.86dB</td></tr>
<tr><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">1</td><td>+1.72dB</td></tr>
<tr><td colspan="4">1</td><td colspan="4">1</td><td colspan="4">0</td><td>+2.58dB</td></tr>
<tr><td colspan="4">1</td><td colspan="4">1</td><td colspan="4">1</td><td>Not Used</td></tr>
</table>

Table 10: Gain Set Register Settings


(Command Data)
(MSB) - Loaded First
Byte 1
Byte 0
(Command Data)
(LSB) - Loaded Last
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
P
"0"
Q

CTCSS TX Frequency/NRZ Baud Rate Register

Figure 8: Gain Set with Pre-Emphasisi

6 Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
P / DW / LH Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 11: Absolute Maximum Ratings

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.0		MHz

Table 12: Operating Limits

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.0MHz, Audio Level 0dB ref. = 308mV_{RMS} @ 1kHz
Composite Signal = 308mV_{RMS} @ 1kHz + 75mV_{RMS} Noise + 31mV_{RMS} Sub-Audio signal
Noise Bandwidth = 5kHz Band Limited Gaussian

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
All Functions Enabled			5.0	7.0	mA
All Functions Disabled			2.0	3.0	mA
Powersave All			0.9	1.5	mA
Analog Impedances					
RX Sub-Audio Input		350.0	1500.0		kΩ
Audio Input		350.0			kΩ
Audio Bypass Switch On	5		2.0		kΩ
Audio Bypass Switch OFF	5	1.0	6.5		MΩ
RX Amp Input (+ and -)		1.0	6.5		MΩ
Comparator Input (+ and -)		1.0	6.5		MΩ
RX Sub-Audio Output			2.0		kΩ
TX Sub-Audio Output					
Encoder Enabled	5		2.0		kΩ
Encoder Disabled	5		500.0		kΩ
Audio Output					
Encoder Enabled	5		2.0		kΩ
Encoder Disabled	5		500.0		kΩ
RX Amp and Comparator Outputs					
Large Signal			6.0		kΩ
Small Signal			600.0		kΩ
Dynamic Values					
Digital Interface					
Input Logic 1	1	3.5			V
Input Logic 0	1			1.5	V
Output Logic 1 (I_{OH} = -120mA)	2	4.6			V
Output Logic 1 (I_{OL} = -360mA)	3			0.4	V
I_{OUT} Tristate (Logic 1 or 0)	3			4.0	µA
Input Capacitance	1			7.5	pF
Logic Input Current (V_{IN} = 0 to 5.0V)	1			1.0	µA
IOX (V_{OUT} = 5.0V)	4			4.0	µA

	Notes	Min.	Typ.	Max.	Units
Overall Performance					dB
CTCSS - Decode					kHz
Sensitivity (Composite Signal)	6	-20.0	-26.0		dB
Response Time (Composite Signal)					
100Hz to 257Hz Tone			210.0	250.0	ms
65Hz Tone	9		210.0	384.0	ms
Tone Measurement Resolution			0.2		%
Tone Measurement Accuracy		-0.5		0.5	%
NoTone Response Time (Composite Signal)	7		175.0	250.0	ms
False tone Interrupts (Noise Input Only)	10		20.0		/Hr
CTCSS Encode					
Frequency Range		65.0		257.0	Hz
Tone Frequency Resolution				0.2	%
Tone Amplitude Tolerance	12	-1.0		1.0	dB
Rise Time (to 90%)				30.0	ms
Fall Time (to 10%)				50.0	ms
Total Harmonic Distortion				5.0	%
NRX – Decode					
RX Bit Rate Sync Time			2		edge
RX Bit Error Rate	11		1×10^{-3}		$P_{(ERROR)}$
NRZ – TX					
TX Bit Rate		67.0		300.0	bits/sec
TX LPF (3dB) Bandwidth		75.0		300.0	Hz
Sub-Audio TX Output Level					
CTCSS			0		dB
NRZ			0.871		V_{P-P}
Amplitude Adjustment Range		-2.58		2.58	dB
Adjustment Step Size (7 Steps)	8		0.86		dB
Sub-Audio Bandstop Filter					
Passband		297.0		3000.0	Hz
Passband Gain (@ 1.0kHz)			0		dB
Passband Ripple (with respect to gain @ 1.0Hz)		-1.5		0.5	dB
Stopband Gain < 250Hz			36.0		dB
Residual Hum and Noise			-50.0	-45.7	dB
Alias Frequency				62.5	kHz
Receive Lowpass Filter (See Figure 9)					
Cutoff Frequency (-3dB)			280.0		Hz
Passband Gain			6.0		dB
Xtal/Clock Frequency (f_{XTAL})			4.0	6.1	MHz

Table 13: Operating Characteristics

Operating Characteristics Notes:

1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$, and $\overline{\text{CS}}$.
2. Reply Data Output
3. Reply Data and $\overline{\text{IRQ}}$ outputs
4. Leakage current into the "OFF" $\overline{\text{IRQ}}$ output.
5. See Control Register
6. With input gain components set as recommended in Figure 2.
7. Probability 97%
8. See Gain Set Register.
9. For f_{CTCSS} IN of 65Hz to 100Hz, Response Time $t_R = (100/f_{Tone}) \times 250$ms.
10. Distributed across the RX Frequency band
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.
12. At any gain setting of Gain Register.

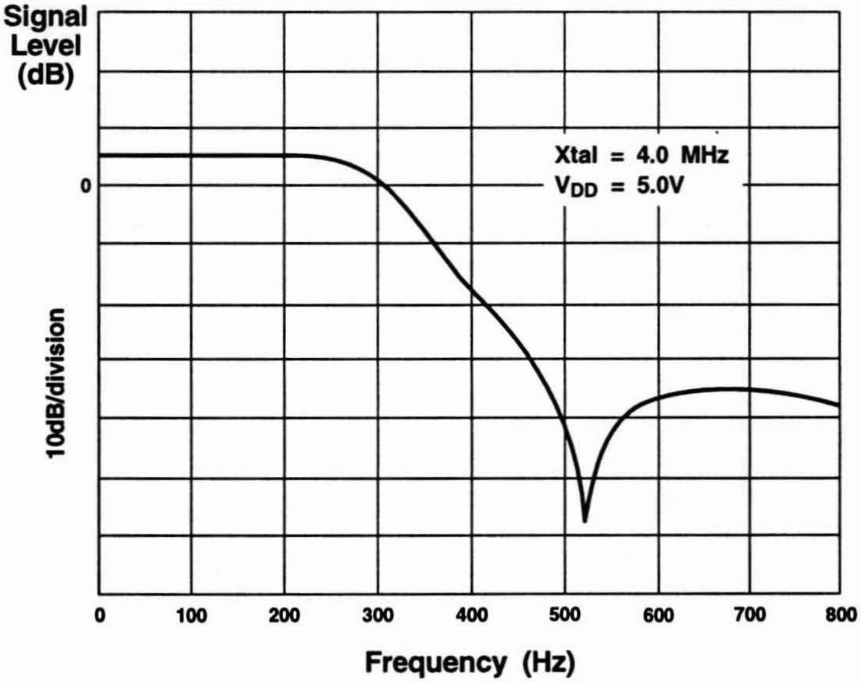


Figure 9: Typical Frequency Response of RX Lowpass Filter

6.1.4 Timing

Timing Parameters for two-way communications between the µC and the MX805A on the C-BUS are shown in Table 14.

C-BUS Timing		Min.	Typ.	Max.	Units
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CHS}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{CSOFF}	Chip Select High	2.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs
t_{CH}	Decoder or Encoder Clock High	500			ns
t_{CL}	Decoder or Encoder Clock Low	500			ns
t_{CDS}	Command Data Set-Up Time	250			ns
t_{CDH}	Command Data Hold Time	0			ns
t_{RDS}	Reply Data Set-Up Time	250			ns
t_{RDH}	Reply Data Hold Time	50.0			ns
t_{HIZ}	Chip Select High to Reply Data High – Z			2.0	µs

Table 14: Timing Information

Notes:

1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX805A MXB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX805A and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX805A will work with either polarity Serial clock pulses.

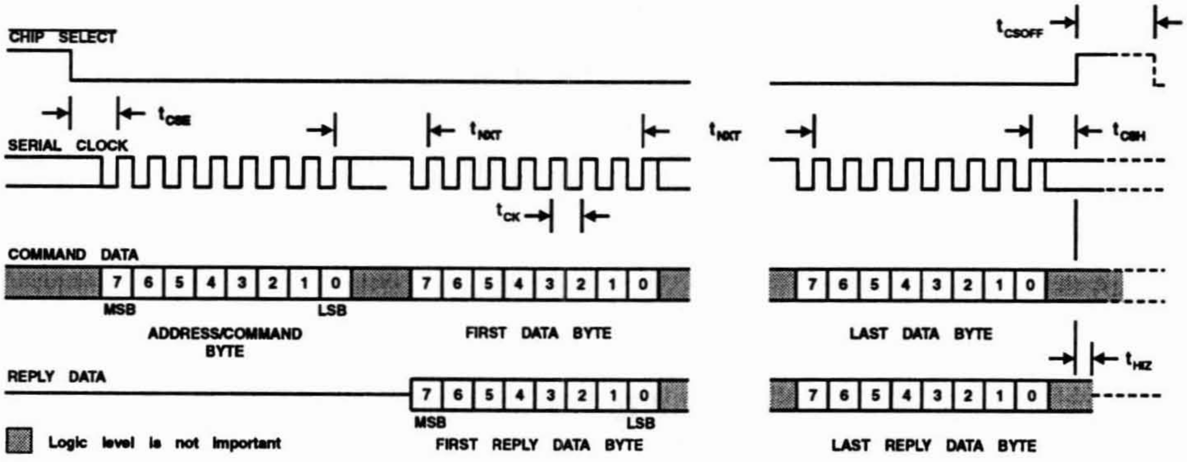

CHIP SELECT
t_{CSOFF}
t_{CSE}
SERIAL CLOCK
t_{NXT}
t_{NXT}
t_{CSH}
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
Logic level is not important

Figure 10: C-BUS Timing Information

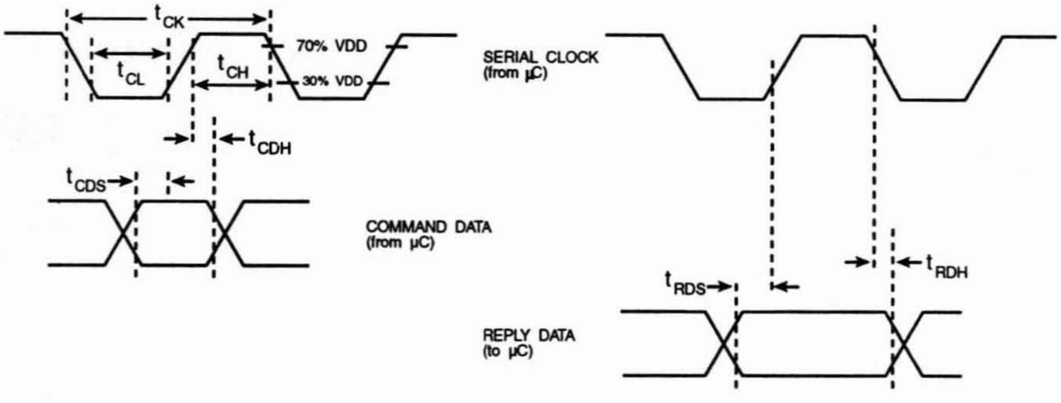
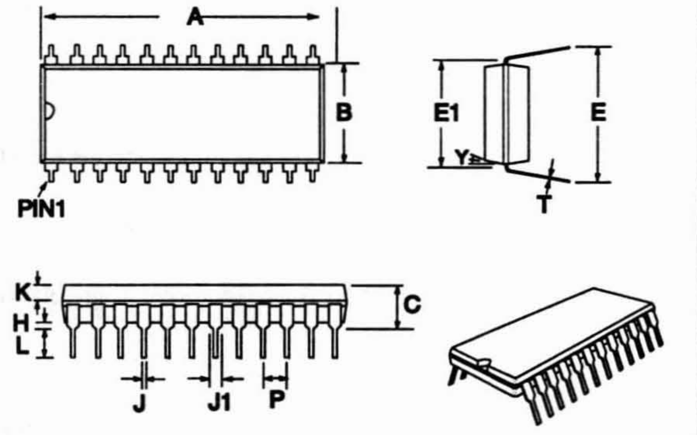

t_{CK}
t_{CL}
t_{CH}
70% VDD
30% VDD
t_{CDH}
t_{CDS}
COMMAND DATA
(from µC)
SERIAL CLOCK
(from µC)
t_{RDS}
t_{RDH}
REPLY DATA
(to µC)

Figure 11: Timing Relationships for C-BUS Information Transfer

6.2 Packages

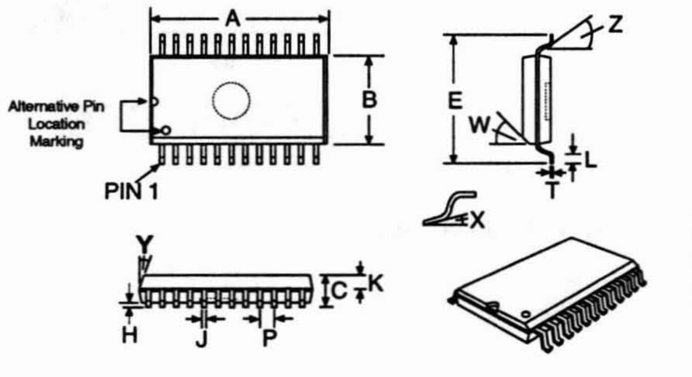

A
B
PIN1
E1
E
Y
T
K
H
L
C
J
J1
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin PDIP Mechanical Outline: *Order as part no. MX805AP*

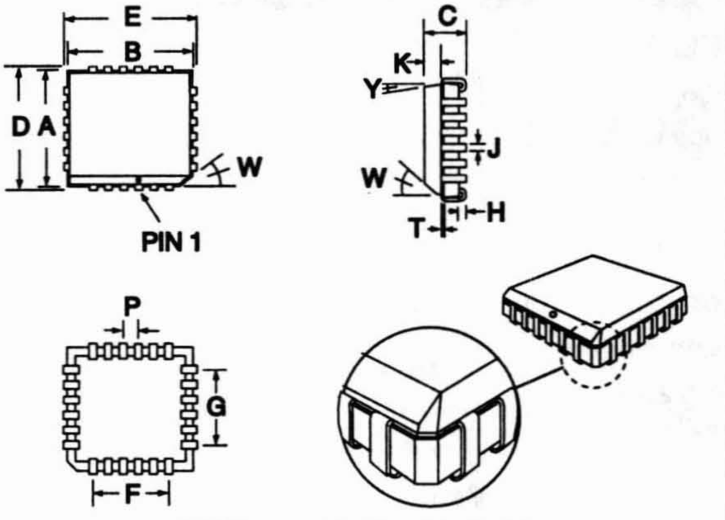

A
B
Alternative Pin Location Marking
PIN 1
Z
E
W
L
T
X
Y
C
K
H
J
P

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin SOIC Mechanical Outline: *Order as part no. MX805ADW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 24-pin PLCC Mechanical Outline: ***Order as part no. MX805ALH***

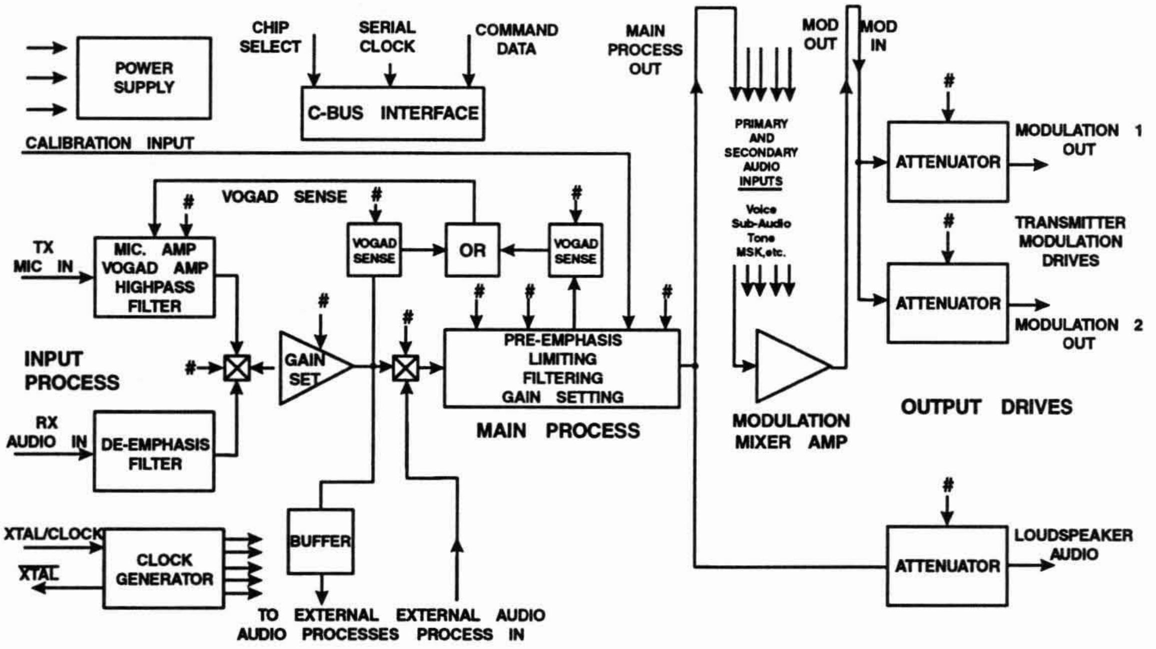
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX806A Audio Processor

Features

- **Half-Duplex Audio Processor**
- **Dynamic Control of Signal Levels**
- **Performs Signal Conditioning and Filtering requirements for both Transmit and Receive**
- **Three separate signal sections:**
  - **Input process**
  - **Main Process**
  - **Mixing and Output Drives**
- **Low Power Operation**
- **Member of DBS800 Family (C-BUS Compatible)**


POWER SUPPLY
CALIBRATION INPUT
CHIP SELECT
SERIAL CLOCK
COMMAND DATA
C-BUS INTERFACE
MAIN PROCESS OUT
MOD OUT
MOD IN
VOGAD SENSE
#
TX MIC IN
MIC. AMP VOGAD AMP HIGHPASS FILTER
VOGAD SENSE
OR
VOGAD SENSE
INPUT PROCESS
GAIN SET
PRE-EMPHASIS LIMITING FILTERING GAIN SETTING
MAIN PROCESS
RX AUDIO IN
DE-EMPHASIS FILTER
PRIMARY AND SECONDARY AUDIO INPUTS
Voice Sub-Audio Tone MSK,etc.
MODULATION MIXER AMP
ATTENUATOR
MODULATION 1 OUT
TRANSMITTER MODULATION DRIVES
ATTENUATOR
MODULATION 2 OUT
OUTPUT DRIVES
XTAL/CLOCK
XTAL
CLOCK GENERATOR
BUFFER
TO EXTERNAL AUDIO PROCESSES
EXTERNAL AUDIO PROCESS IN
ATTENUATOR
LOUDSPEAKER AUDIO

The MX806A LMR audio processor is intended too primarily to operate as the "Audio Terminal" or radio systems using the DBS800 Digitally Integrated Baseband Subsystem.

The MX806A half-duplex device has signal paths and level setting elements that are configured and adjusted by digital information sent from the radio microcontroller using C-BUS protocol. (C-BUS is the serial interface for all DBS 800 ICs.)

The Signal Path is divided into three sections: Input Process, Main process, and Mixing and Output Drives.

If selected, signal level stability and output accuracy of the MX806A is maintained by a voltage-controlled gain system using selectable signal-level detectors. Signal levels can be dynamically controlled to provide "dynamic compensation" for factors such as temperature drift, VCO non-linearity, etc.

The MX806A audio stages can be completely disabled – or the whole IC can be placed into powersave mode, leaving only clock and C-BUS circuitry active.

The MX806A may be used with a 5.0V power supply and is available in the following packages:
24-pin SOIC (MX806ADW), 24-pin PLCC (MX806ALH), and 24-pin PDIP (MX806AP).

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MXCOM, Inc. reserves the right to change specifications at any time without notice.

1 Block Diagram

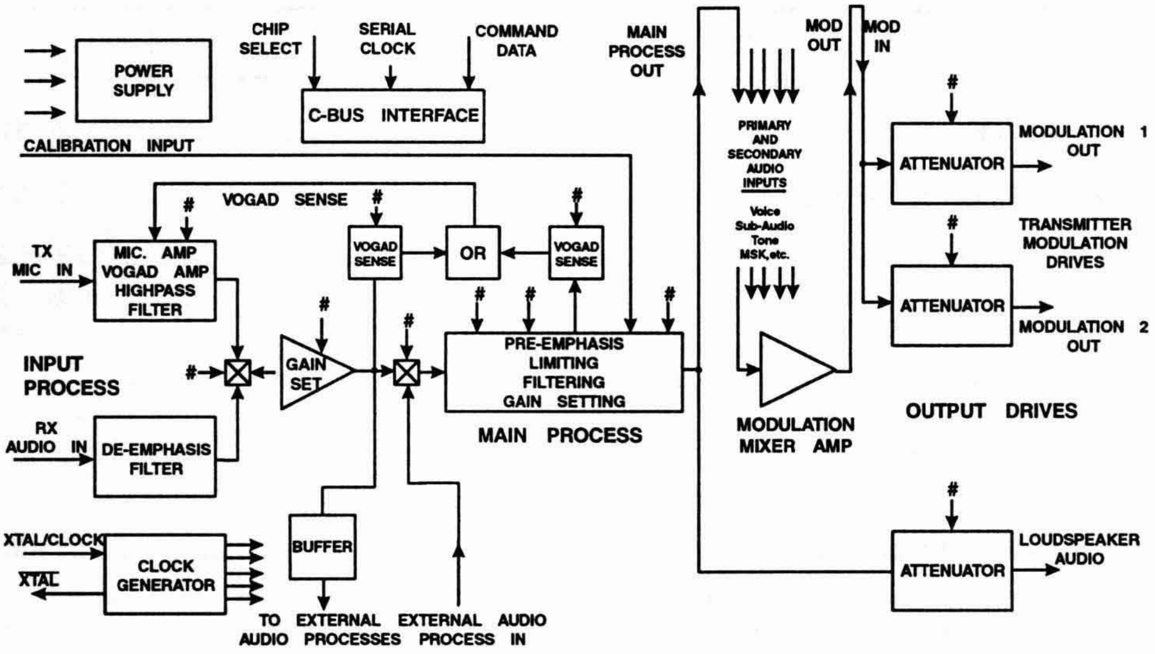

POWER SUPPLY
CHIP SELECT
SERIAL CLOCK
COMMAND DATA
C-BUS INTERFACE
MAIN PROCESS OUT
MOD OUT
MOD IN
CALIBRATION INPUT
PRIMARY AND SECONDARY AUDIO INPUTS
Voice Sub-Audio Tone MSK, etc.
#
ATTENUATOR
MODULATION 1 OUT
TRANSMITTER MODULATION DRIVES
ATTENUATOR
MODULATION 2 OUT
VOGAD SENSE
TX MIC IN
MIC. AMP VOGAD AMP HIGHPASS FILTER
VOGAD SENSE
OR
VOGAD SENSE
INPUT PROCESS
GAIN SET
PRE-EMPHASIS LIMITING FILTERING GAIN SETTING
MAIN PROCESS
MODULATION MIXER AMP
OUTPUT DRIVES
RX AUDIO IN
DE-EMPHASIS FILTER
XTAL/CLOCK
XTAL
CLOCK GENERATOR
BUFFER
TO EXTERNAL AUDIO PROCESSES
EXTERNAL AUDIO PROCESS IN
ATTENUATOR
LOUDSPEAKER AUDIO

Figure 1: Block Diagram

2 Signal List

Pin	Signal	Description
1	$\overline{\text{Xtal}}$	The output of the 4.032MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	Xtal/Clock	The input to the on-chip 4.032MHz clock oscillator inverter. A 4.032MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc.
3	Serial Clock	This is the 'C-BUS' serial Clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MX805A. See Section 6 and Section 7.1.4.
4	Command Data	This is the 'C-BUS' serial data input from the microcontroller. Command Data is loaded to this device in 8-bit bytes, MSB (bit 7) first and LSB (bit 0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Table 3 through Table 7. See Section 6 and Section 7.1.4.
5	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$. This is the 'C-BUS' data loading control function. This input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Section 6 and Section 7.1.4.
6	VOGAD OUT	The error-voltage output of the selected VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figure 2 and Figure 3, to the VOGAD In pin.
7	RX Audio In	The audio input to the MX806A from the radio receiver's demodulator circuits. This input, which requires AC coupling with capacitor C12, is selected via a Control Command bit.
8	VOGAD In	The gain control signal from the selected VOGAD sensor (VOGAD Out) to the Input Process voltage-controlled amplifier. The required sensor is selected via a Mode Command. The choice of two sensors enables gain control from either the Input Process or an External Process. External attack and decay setting components should be applied as recommended. See Figure 2 and Figure 3.
9	V_{BIAS}	The output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C10. See Figure 2.
10	Mic In (+)	The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
11	Mic In (-)	The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
12	V_{SS}	Negative Supply (GND)
13	Mic Out	The output of the Microphone Op-Amp, used with the Mic In (-) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with wither inverting or non-inverting inputs. During Powersave (Volume Command this output is placed at V_{SS}.)
14	Processed Audio In	The input to the device from such external audio processed as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires AC Coupling with capacitor C13, is selected by a Mode Command bit.
15	External Audio Process	The buffered output of the Input Processing Stage. Its purpose is to further external audio processing stages prior to re-introduction at the Processed Audio In Pin.
16	Calibration Input	A unique audio input to be used for dynamic balancing of the modulator drives for measuring Deviation Limiter levels. A CUE (beep) input from the MX803 Audio Tone Processor can be entered on this line. This audio input must be externally biased. It is selected via a Mode Command bit.
17	Main Process Out	The output of the Main Process stage. This output should be mixed with any additional system audio inputs (Audio, Sub-Audio Signaling, MSK) in the on-chip Modulation Summing Amplifier. External components shown in Figure 2 should be used as required.

Pin	Signal	Description
18	Sum In	The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals and gain/attenuation setting as shown in Figure 2. For single-signal, no gain requirements, Main Process Out may be linked directly to Modulation In.
19	Sum Out	
20	Modulation In	The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives
21	Audio Output	The processed audio signal output intended as a received audio (volume) output. Though normally used in the RX mode, operation in TX is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	Modulation 1 Drive	The drive to the radio modulator Voltage Controlled Oscillator (VCO) from the composite audio summing stage.
23	Modulation 2 Drive	The drive to the radio modulator Reference Oscillator from the composite audio summing stage. Note: These VCO output attenuators are individually adjustable using the Modulator Level command. During Powersave these outputs are placed at V_{SS}.
24	V_{DD}	Positive Supply. A single 5.0V regulated supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

Table 1: Signal List

3 External Components

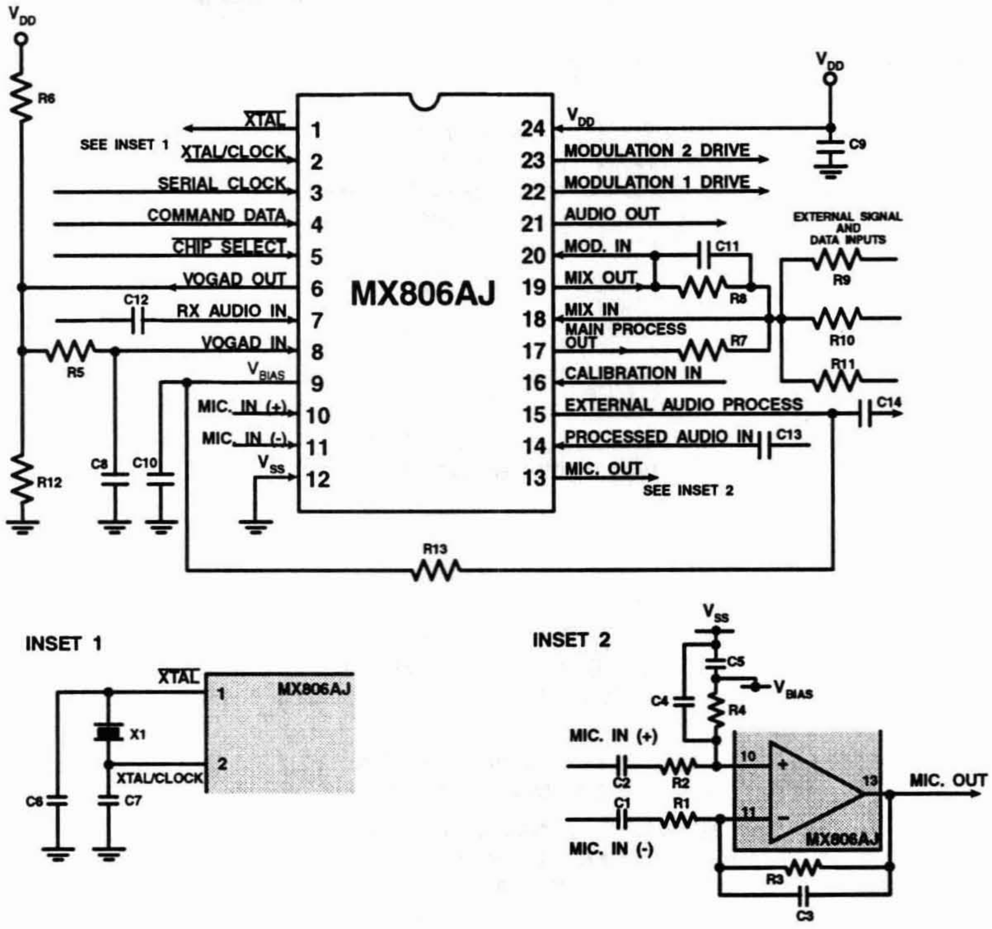

V_DD
R6
SEE INSET 1
XTAL
XTAL/CLOCK
SERIAL CLOCK
COMMAND DATA
CHIP SELECT
VOGAD OUT
C12
RX AUDIO IN
R5
VOGAD IN
V_BIAS
MIC. IN (+)
MIC. IN (-)
V_SS
C8
C10
R12
1
2
3
4
5
6
7
8
9
10
11
12
MX806AJ
24
23
22
21
20
19
18
17
16
15
14
13
V_DD
MODULATION 2 DRIVE
MODULATION 1 DRIVE
AUDIO OUT
MOD. IN
C11
MIX OUT
R8
MIX IN
MAIN PROCESS OUT
R7
CALIBRATION IN
EXTERNAL AUDIO PROCESS
C14
PROCESSED AUDIO IN
C13
MIC. OUT
SEE INSET 2
V_DD
C9
EXTERNAL SIGNAL AND DATA INPUTS
R9
R10
R11
R13
INSET 1
XTAL
1
MX806AJ
X1
XTAL/CLOCK
2
C6
C7
INSET 2
V_SS
C5
V_BIAS
C4
R4
MIC. IN (+)
10
+
C2
R2
C1
R1
11
−
13
MIC. OUT
MX806AJ
MIC. IN (-)
R3
C3

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		10kΩ	±10%
R2		10kΩ	±10%
R3		20kΩ	±10%
R4		20kΩ	±10%
R5		10kΩ	±10%
R6		2.2MΩ	±10%
R7		100kΩ	±10%
R8		100kΩ	±10%
R9		100kΩ	±10%
R10		100kΩ	±10%
R11		100kΩ	±10%
R12		2.2MΩ	±10%
R13		470kΩ	±10%
C1		.47μF	±20%

Component	Notes	Value	Tolerance
C2		.47μF	±20%
C3		270pF	±20%
C4		270pF	±20%
C5		0.1μF	±20%
C6		33pF	±20%
C7		5-65pF	±20%
C8		1.0μF	±20%
C9		1.0μF	±20%
C10		1.0μF	±20%
C11		22pF	±20%
C12		0.1μF	±20%
C13		0.01μF	±20%
C14		0.01μF	±20%
X1		4.00MHz	

Table 2: Recommended External Components

Recommended External Component Notes:

1. Input Op-Amp gain/attenuation components (voltage gain = 6.0dB) are shown in Inset 1 is a differential configuration to demonstrate the versatility of this input. Components for a single (+ or -) input may be used.
2. Resistor values R7 to R11 (summation components) are dependent upon application and configuration requirements.
3. Xtal circuit capacitors C6 (CD) and C7 (CG) shown in Inset 2 are recommended in accordance with MX-COM's Crystal Oscillator Application Note. Circuit drive and drain resistors are incorporated on-chip. Operation of any MX-COM IC without a Xtal clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power-input (V_{DD}).

4 General Description

The MX806A LMR audio processor is intended too primarily to operate as the "Audio Terminal" or radio systems using the DBS800 Digitally Integrated Baseband Subsystem.

The MX806A half-duplex device has signal paths and level setting elements that are configured and adjusted by digital information sent from the radio microcontroller using C-BUS protocol. (C-BUS is the serial interface for all DBS 800 ICs.)

4.1 Signal Path

The Signal path is divided into three sections:

Input Process: This stage has selectable TX/RX paths. Transmits voice signals pass through microphone pre-amplifier, voltage controlled gain (VOGAD) and highpass filter stages. Received audio is de-emphasized. This initial audio, after line-in gain adjustment, may be switched to external audio processes (such as scrambling) or to the internal Main Process stages.

Main Process: Conditioning for the input or external process signals is completed in this stage. It is comprised of pre-emphasis, high and lowpass switched capacitor filters and a deviation limiter.

Mixing and Output Drives: Main audio for transmission is mix with signaling and data from external sources (other DBS 800 ICs) to provide the composite signal for the digitally adjustable transmitter modulation drives. Received audio level is adjusted for output to loudspeaker circuitry.

If selected, signal level stability and output accuracy of the MX806A is maintained by a voltage-controlled gain system using selectable signal-level detectors. Signal levels can be dynamically controlled to provide "dynamic compensation" for factors such as temperature drift, VCO non-linearity, etc.

The MX806A audio stages can be completely disabled – or the whole IC can be placed into powersave mode, leaving only clock and C-BUS circuitry active.

4.2 VOGAD

The overall Gain Control system of the MX806A consists of 2 selectable signal peak detectors whose output is fed via external integrating components to adjust the gain of the Voltage Controlled Amplifier positioned in the TX Input Process Path. The transmit input signals is presented to Peak Detector 1 or 2. The Peak Detectors are enabled individually by a Mode Command. When the input signal exceeds the peak - to - peak threshold of the detector, a 5-volt level is produced at the VOGAD Out pin. This level remains for as long as the signal exceeds the threshold. The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. As can be seen from Figure 3 and Figure 5, Peak Detector 1 allows control of the audio level to the external audio process and Peak Detector 2 allows control of transmit deviation levels.

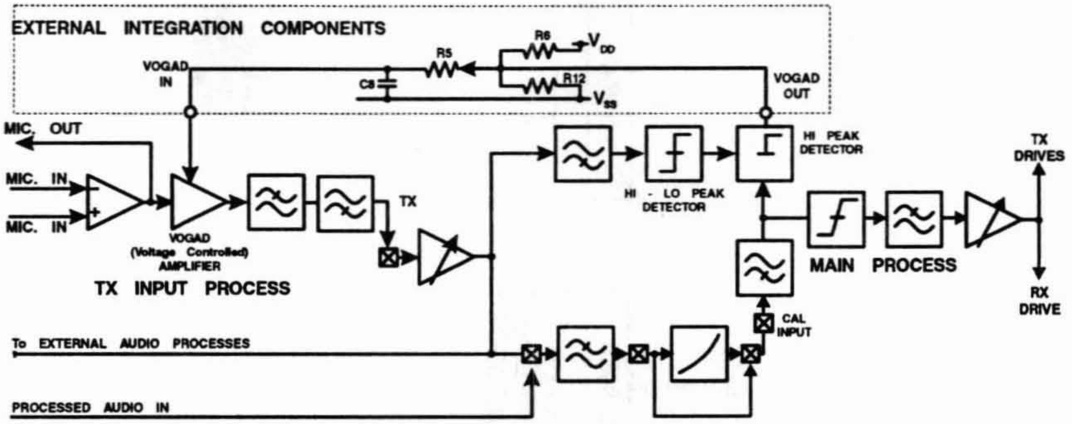

EXTERNAL INTEGRATION COMPONENTS
R6
V_{DD}
R5
VOGAD IN
C8
R12
V_{SS}
VOGAD OUT
MIC. OUT
MIC. IN
MIC. IN
VOGAD (Voltage Controlled) AMPLIFIER
TX INPUT PROCESS
TX
HI PEAK DETECTOR
HI - LO PEAK DETECTOR
TX DRIVES
MAIN PROCESS
RX DRIVE
CAL INPUT
To EXTERNAL AUDIO PROCESSES
PROCESSED AUDIO IN

Figure 3: VOGAD Sensors and Timing Components (from Figure 5)

VOGAD attack and decay times are set using the external components shown in Figure 2 and Figure 3. They are calculated as described below.

4.2.1 VOGAD Components Calculations – Figure 2 and Figure 5

Provided $R5 \gg 1.0k$ and $R6 = R12 \gg R5$

Then

$$\text{Attack Time } (T_A) = R5 \times C8$$

$$\text{Decay Time } (T_D) = \frac{R6 \times C8}{2}$$

4.3 Calibration Methods

To effectively null all internal IC tolerance, the following initial calibration routine is suggested.

4.3.1 TX Calibration: From Mic. In to Modulator Drives Out

Disable Peak Detectors (Mode Command)
Set Transmitter Drives to 0dB (Mod. Levels Set)
Pre-emphasis may be employed as required (Control Command)
Set Input Level Amp to 0dB Control Command)

1. Mic. In = 250mVRMS at 1kHz. Set Process Gain Amp for output of 1440mV$_{P\text{-}P}$ (100% deviation).
2. With Process Gain Amp set as 1 and with Mic. In = 25mV$_{RMS}$ at 1kHz, set the Input Level Amp for an output level of 308mV$_{RMS}$ (60% deviation)

4.3.2 RX Calibration: From RX Audio In to Audio Out

Set Audio Output Drive In to Audio Out
Leave Process Gain Amp set as 1 (See Section 4.3.1)

3. With and RX Audio In level of between 154mV$_{RMS}$ and 308mV$_{RMS}$ (See Section 7) at 1kHz, set the Input Level Amp for and output level of 308mV$_{RMS}$.

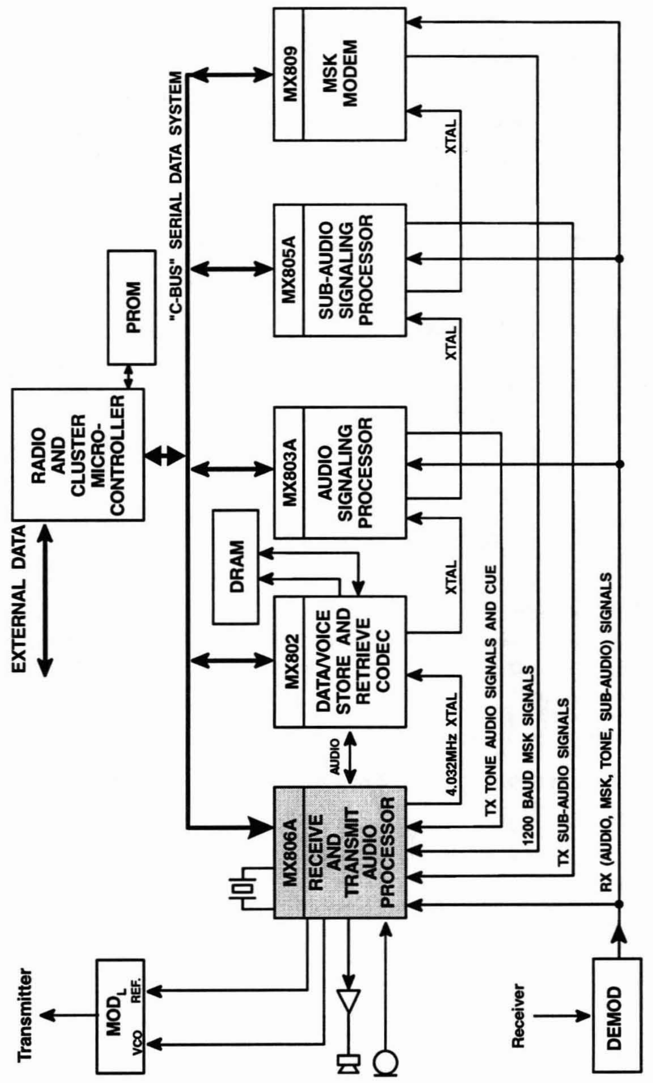
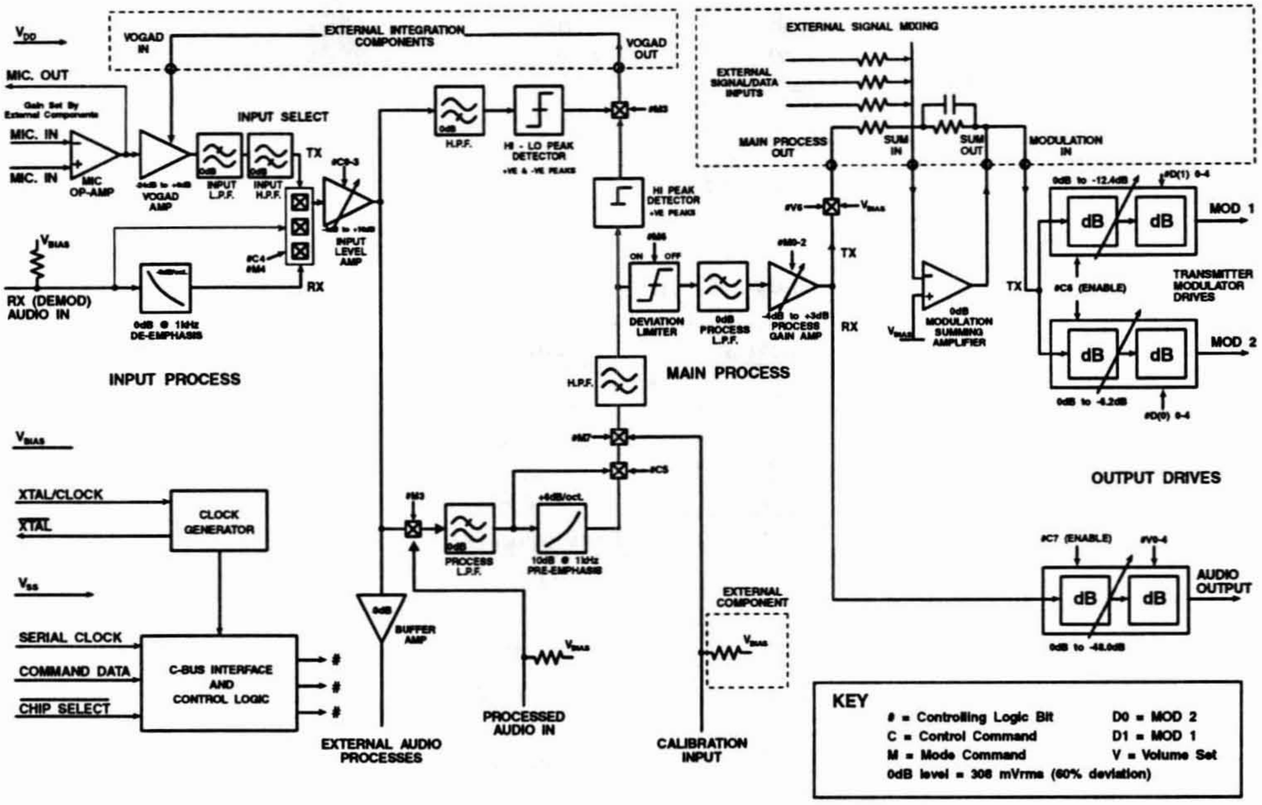

EXTERNAL DATA
RADIO AND CLUSTER MICRO-CONTROLLER
PROM
"C-BUS" SERIAL DATA SYSTEM
Transmitter
MOD$_L$
VCO
REF.
DRAM
MX806A
RECEIVE AND TRANSMIT AUDIO PROCESSOR
AUDIO
MX802
DATA/VOICE STORE AND RETRIEVE CODEC
MX803A
AUDIO SIGNALING PROCESSOR
MX805A
SUB-AUDIO SIGNALING PROCESSOR
MX809
MSK MODEM
4.032MHz XTAL
XTAL
XTAL
XTAL
TX TONE AUDIO SIGNALS AND CUE
1200 BAUD MSK SIGNALS
TX SUB-AUDIO SIGNALS
Receiver
DEMOD
RX (AUDIO, MSK, TONE, SUB-AUDIO) SIGNALS

Figure 4: MX806A Interfaced with Other DBS 800 Elements



V_{DD}
VOGAD IN
EXTERNAL INTEGRATION COMPONENTS
VOGAD OUT
MIC. OUT
Gain Set By External Components
MIC. IN
MIC. IN
MIC OP-AMP
VOGAD AMP
INPUT SELECT
0dB
INPUT L.P.F.
INPUT H.P.F.
TX
RX
#C4
#M4
INPUT LEVEL AMP
V_{BIAS}
RX (DEMOD) AUDIO IN
0dB @ 1kHz DE-EMPHASIS
INPUT PROCESS
H.P.F.
HI - LO PEAK DETECTOR
+VE & -VE PEAKS
#M3
HI PEAK DETECTOR
+VE PEAKS
ON
OFF
DEVIATION LIMITER
0dB PROCESS L.P.F.
#M0-2
-4dB to +3dB PROCESS GAIN AMP
MAIN PROCESS
#M7
#C5
EXTERNAL SIGNAL MIXING
EXTERNAL SIGNAL/DATA INPUTS
MAIN PROCESS OUT
SUM IN
SUM OUT
MODULATION IN
#V6
V_{BIAS}
TX
RX
0dB MODULATION SUMMING AMPLIFIER
V_{BIAS}
0dB to -12.4dB
#D(1) 0-4
dB
dB
MOD 1
#C6 (ENABLE)
TRANSMITTER MODULATOR DRIVES
dB
dB
MOD 2
0dB to -4.2dB
#D(0) 0-4
OUTPUT DRIVES
V_{BIAS}
XTAL/CLOCK
$\overline{XTAL}$
CLOCK GENERATOR
V_{SS}
SERIAL CLOCK
COMMAND DATA
$\overline{CHIP\ SELECT}$
C-BUS INTERFACE AND CONTROL LOGIC
#
#
#
0dB
BUFFER AMP
EXTERNAL AUDIO PROCESSES
#M3
PROCESS L.P.F.
+6dB/oct.
10dB @ 1kHz PRE-EMPHASIS
PROCESSED AUDIO IN
EXTERNAL COMPONENT
CALIBRATION INPUT
#C7 (ENABLE)
#V0-4
AUDIO OUTPUT
0dB to -48.0dB
KEY
# = Controlling Logic Bit
C = Control Command
M = Mode Command
0dB level = 308 mVrms (60% deviation)
D0 = MOD 2
D1 = MOD 1
V = Volume Set

Figure 5: LMR Audio Processor Explanatory Block Diagram

5 Controlling Protocol

Control of the functions and levels within the MX806A LMR Audio processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment		Address/Command Binary		Command Data	Table
	HEX	MSB LSB			
General Reset	01	00000001			
Control Command	10	00010000	+	1 byte	2
Mode Command	11	00010001	+	1 byte	3
Mod. Levels Set	12	00010010	+	2 bytes	4
Volume Set	13	00010011	+	1 byte	5

Table 3: C-BUS Address/Commands

In “C-BUS” protocol the MX806A is allocated Address/Command values 10H and 13H. C-BUS Command Mode, Modulation and Volume assignments, and data requirements are given in Table 3 and illustrated in Figure 5.

Commands and Data are only to be loaded in the group configurations detailed since the “C-BUS” interface recognizes the first byte after Chip Select (logic “0”) as an Address/Command.

Function or Level control data, which is detailed in Table 4, Table 5, Table 6, and Table 7, is acted upon at the end of the loaded instruction

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01H) is required. This command is provided to "reset" all devices on the Command "Data line and has the following effect on the MX806A:

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

5.1.1 Control Command – (Preceded by A/C 10_H)

Settings				**Control Bits**
MSB				
7				**Audio Output (RX)**
0 1				Disabled Enabled
6				**Modulation Drives**
0 1				Disabled Enabled
5				**Pre-Emphasis**
0 1				Bypass Enabled
4				**Input Select**
0 1				RX In Mic. In
3	**2**	**1**	**0**	**Input Level Set**
0	0	0	0	Input Amp Disabled
0	0	0	1	–4.0dB
0	0	1	0	–3.0dB
0	0	1	1	–2.0dB
0	1	0	0	–1.0dB
0	1	0	1	0dB
0	1	1	0	1.0dB
0	1	1	1	2.0dB
1	0	0	0	3.0dB
1	0	0	1	4.0dB
1	0	1	0	5.0dB
1	0	1	1	6.0dB
1	1	0	0	7.0dB
1	1	0	1	8.0dB
1	1	1	0	9.0dB
1	1	1	1	10.0dB

Table 4: Control Commands

5.1.2 Mode Command – (Preceded by A/C 11_H)

Setting			Mode Bits
MSB			
7			**Drive Source**
0			Signals
1			Calibration
6			**Deviation Limiter**
0			Disabled
1			Enabled
5			**VOGAD**
0			Disabled
1			Enabled
4			**De-Emphasis**
0			Enabled
1			Bypassed
3			**Signal Select**
0			Internal
1			External
2	**1**	**0**	**Process Gain Set**
0	0	0	–4.0dB
0	0	1	–3.0dB
0	1	0	–2.0dB
0	1	1	–1.0dB
1	0	0	0dB
1	0	1	1.0dB
1	1	0	2.0dB
1	1	1	3.0dB

Table 5: Mode Commands

5.1.3 Modulator Levels – (Preceded by A/C 12_H)

Setting					Modulator Drives
Byte 1					First byte for transmission
MSB					
7	6	5			
0	0	0			Must be "0"
4	**3**	**2**	**1**	**0**	**VCO Drive Attenuation**
0	0	0	0	0	12.4dB
0	0	0	0	1	12.0dB
0	0	0	1	0	11.6dB
0	0	0	1	1	11.2dB
0	0	1	0	0	10.8dB
0	0	1	0	1	10.4dB
0	0	1	1	0	10.0dB
0	0	1	1	1	9.6dB
0	1	0	0	0	9.2dB
0	1	0	0	1	8.8dB
0	1	0	1	0	8.4dB
0	1	0	1	1	8.0dB
0	1	1	0	0	7.6dB
0	1	1	0	1	7.2dB
0	1	1	1	0	6.8dB
0	1	1	1	1	6.4dB
1	0	0	0	0	6.0dB
1	0	0	0	1	5.6dB
1	0	0	1	0	5.2dB
1	0	0	1	1	4.8dB
1	0	1	0	0	4.4dB
1	0	1	0	1	4.0dB
1	0	1	1	0	3.6dB
1	0	1	1	1	3.2dB
1	1	0	0	0	2.8dB
1	1	0	0	1	2.4dB
1	1	0	1	0	2.0dB
1	1	0	1	1	1.6dB
1	1	1	0	0	1.2dB
1	1	1	0	1	0.8dB
1	1	1	1	0	0.4dB
1	1	1	1	1	0dB

Setting					Modulator Drives
Byte 0					Last byte for transmission
MSB					
7		6	5		
0		0	0		Must be "0"
4	**3**	**2**	**1**	**0**	**VCO Drive Attenuation**
0	0	0	0	0	6.2dB
0	0	0	0	1	6.0dB
0	0	0	1	0	5.8dB
0	0	0	1	1	5.6dB
0	0	1	0	0	5.4dB
0	0	1	0	1	5.2dB
0	0	1	1	0	5.0dB
0	0	1	1	1	4.8dB
0	1	0	0	0	4.6dB
0	1	0	0	1	4.4dB
0	1	0	1	0	4.2dB
0	1	0	1	1	4.0dB
0	1	1	0	0	3.8dB
0	1	1	0	1	3.6dB
0	1	1	1	0	3.4dB
0	1	1	1	1	3.2dB
1	0	0	0	0	3.0dB
1	0	0	0	1	2.8dB
1	0	0	1	0	2.6dB
1	0	0	1	1	2.4dB
1	0	1	0	0	2.2dB
1	0	1	0	1	2.0dB
1	0	1	1	0	1.8dB
1	0	1	1	1	1.6dB
1	1	0	0	0	1.4dB
1	1	0	0	1	1.2dB
1	1	0	1	0	1.0dB
1	1	0	1	1	0.8dB
1	1	1	0	0	0.6dB
1	1	1	0	1	0.4dB
1	1	1	1	0	0.2dB
1	1	1	1	1	0dB

Table 6: Modulator Drive Levels

5.1.4 Volume Set – (Preceded by A/C 13_H)

Setting					Volume Set
MSB					
7		**5**			**Main Process Out**
0		0			Enabled
0		1			Biased
5					**Powersave**
0					Chip Enabled
1					Powersaved
4	**3**	**2**	**1**	**0**	**VCO Drive Attenuation**
0	0	0	0	0	OFF
0	0	0	0	1	48.0dB
0	0	0	1	0	46.4dB
0	0	0	1	1	44.8dB
0	0	1	0	0	43.2dB
0	0	1	0	1	41.6dB
0	0	1	1	0	40.0dB
0	0	1	1	1	38.4dB
0	1	0	0	0	36.8dB
0	1	0	0	1	35.2dB
0	1	0	1	0	33.6dB
0	1	0	1	1	32.0dB
0	1	1	0	0	30.4dB
0	1	1	0	1	28.8dB
0	1	1	1	0	27.2dB
0	1	1	1	1	25.6dB
1	0	0	0	0	24.0dB
1	0	0	0	1	22.4dB
1	0	0	1	0	20.8dB
1	0	0	1	1	19.2dB
1	0	1	0	0	17.6dB
1	0	1	0	1	16.0dB
1	0	1	1	0	14.4dB
1	0	1	1	1	12.8dB
1	1	0	0	0	11.2dB
1	1	0	0	1	9.6dB
1	1	0	1	0	8.0dB
1	1	0	1	1	6.4dB
1	1	1	0	0	4.8dB
1	1	1	0	1	3.2dB
1	1	1	1	0	1.6dB
1	1	1	1	1	0dB

Table 7: Volume Set

Notes:

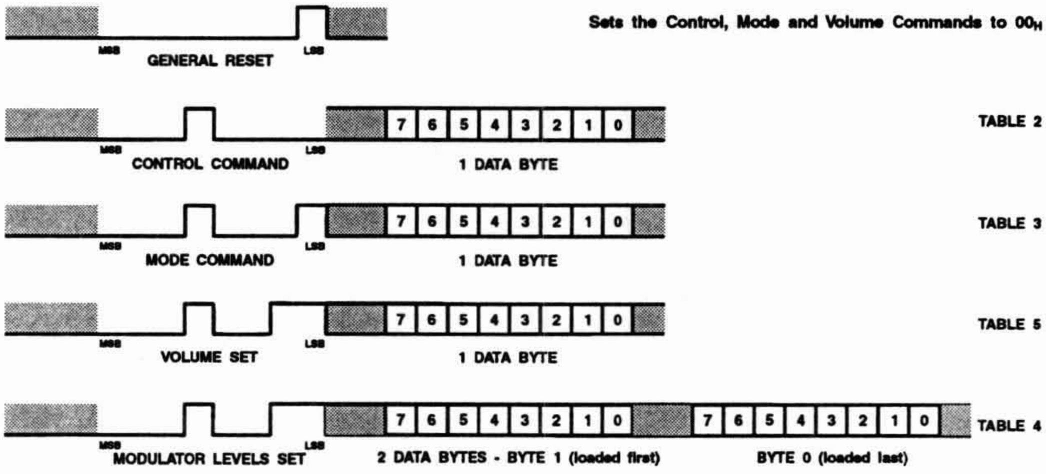
1. Command Loading: Address/Commands and data bytes must be loaded in accordance with the information given in Figure 7.
2. The powersave function is enabled by bit 5 of the Volume Set Command (Table 7).
   During Powersave all internal elements except the clock Generator and "C-BUS" interface are off. The Mic Op-Amp and output Drive stage outputs are connected to V_{SS}.
3. Modulator Drives are controlled separately, but the whole two-byte modulator Drive command must be loaded for each requirement adjustment.
4. $\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

6 Application Notes

To assist in rapid setting, this quick-reference list should be used with Figure 5.

Control	**A/C = 10_H**
7	Audio Out (RX) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Select
4	Input Select (RX/TX)
3-0	Input Level Set (-4dB to 10dB)
Mode	**A/C = 11_H**
7	Drive Source
6	Derivation Limiter Enable
5	VOGAD Enable
4	De-emphasis Enable
3	Signal Select
2-0	Process Gain Set
Modulator Levels	**A/C = 12_H**
Byte 1	
7-5	"0"
4-0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7-5	"0"
4-0	Mod 2 Attenuation (0 to 6.2dB)
Volume Set	**A/C = 13_H**
7-6	"0"
5	Powersave
4-0	Volume Set Attenuation (0 to 48dB)

Table 8: Quick Reference List


MSB
GENERAL RESET
LSB
MSB
CONTROL COMMAND
LSB
1 DATA BYTE
MSB
MODE COMMAND
LSB
1 DATA BYTE
MSB
VOLUME SET
LSB
1 DATA BYTE
MSB
MODULATOR LEVELS SET
LSB
2 DATA BYTES - BYTE 1 (loaded first)
BYTE 0 (loaded last)
7 6 5 4 3 2 1 0

Sets the Control, Mode and Volume Commands to 00_H

TABLE 2

TABLE 3

TABLE 5

TABLE 4

Figure 6: Examples of Command Data Configurations

7 Performance Specifications

7.1 Electrical Specifications

7.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
P / DW / LH Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 9: Absolute Maximum Ratings

7.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.0		MHz

Table 10: Operating Limits

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
$V_{DD} = 5.0V$ @ $T_{AMB} = 25°C$
Xtal/Clock Frequency = 4.0MHz, Audio Level 0dB ref. = 308mV$_{RMS}$ @ 1kHz (60% deviation, FM)

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
All Elements Enabled			8.0	15.0	mA
Maximum Powersave			0.7	1.5	mA
"C-BUS" Interface					
Input Logic "1"		3.5			V
Input Logic "0"				1.5	V
Input Current		-1.0		1.0	µA
Input Capacitance				7.5	pF
Overall Performance					
Microphone Input Level	1, 2		25		mV$_{RMS}$
Discriminator Input Level	2, 3	154		308	mV$_{RMS}$
Output Drive Level					
60% Deviation	2, 4	291	308	326	mV$_{RMS}$
100% Deviation	2, 4, 5		1440		MV$_{P-P}$
Passband	6	297		3000	Hz
Passband Ripple	7	-2		0.5	dB
Stopband Attenuation	6, 8				
@ 150Hz		10	12		dB
@ 3400Hz			2		dB
@ 6000Hz		30	36		dB
@ 8000Hz to 20,000Hz			60		dB
Signal Path Noise					
TX			-50		dBp
TX	9		-45		dB
RX			-60		dB
RX	9		-55		dB
Total Harmonic Distortion					
RX or TX, 60% Deviation			1.0		%
Circuit Elements – Figure 5					
Mic. Amp or Mod. Summation Amp					
Open Loop Gain			50.0		dB
Bandwidth		20.0			kHz
Input Impedance		10.0			MΩ
Output Impedance					
Open Loop			6.0		kΩ
Closed Loop			600		Ω
De-emphasis					
Slope			-6.0		dB/octave
Gain			0		dB
Input Impedance			1		MΩ

	Notes	Min.	Typ.	Max.	Units
Voltage Controlled Gain Amp (VOGAD)					
Gain					
Non-Compression	2		6.0		dB
Full-Compression			-24		dB
Input Impedance		10.0			MΩ
VOGAD Peak Detectors					
Output Impedance					
Logic "1" (Compress)			1		kΩ
Logic "0"			10		MΩ
Hi/Lo Peak Detector Threshold	10		1300		mV_{P-P}
Hi Peak Detector Threshold	10		650		mV + ve pk
Input (Low + Highpass) Filter					
Gain @ 1.0kHz		-1.0		1.0	dB
Input Level Amp					
Gain Range			0		dB
Overall Tolerance		-1.0		1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope			6.0		dB/octave
Gain @ 1.0kHz			10.0		dB
Process Highpass Filter					
Gain @ 1.0kHz		-0.1	0	0.1	dB
Deviation Limiter					
Threshold		708	1300	1413	mV_{RMS}
Gain		-0.5		0.5	dB
Process Lowpass Filter					
Gain @ 1.0kHz		-0.1	0	0.1	dB
Process Gain Amp					
Gain Range		-4.0		3.0	dB
Overall Tolerance		-0.5		0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance			600		Ω
Transmitter Modulator Drives					
Input Impedance			15.0		kΩ
Mod. 1 Attenuator					
Attenuation Range		0		12.4	dB
Overall Tolerance		-1		1	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance			600		Ω
Mod. 2 Attenuator					
Attenuation Range		0		6.2	dB
Overall Tolerance		-0.5		0.5	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance			600		Ω

	Notes	Min.	Typ.	Max.	Units
Audio Output Attenuator					
Attenuation Range		0		48.0	dB
Overall Tolerance		-1.0		1.0	dB
Step Size		1.1	1.6	2.1	dB
Output Impedance			600		Ω
Miscellaneous Impedances					
Processed Audio Input			500		kΩ
Calibration Input			500		kΩ
External Process Out			100		Ω
RX with De-emphasis Bypass			25.0		kΩ

Table 11: Operating Characteristics

Operating Characteristics Notes:

1. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
2. With Output Drives set to 0dB and the system calibrated as described in the Application Notes.
3. Input level range for 0dB output, by adjustment of the Input Level Amp.
4. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
5. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
6. Between Microphone or RX inputs to Modulator or Audio Outputs.
7. Deviation from the ideal overall response including the pre- or de-emphasis slope.
8. Excluding the effect of pre- or de-emphasis slope.
9. In a 30kHz bandwidth.
10. Using pre-emphasis in the TX path.

7.1.4 Timing

Timing Parameters for two-way communications between the µC and the MX805A on the C-BUS are shown in Table 12.

C-BUS Timing		**Min.**	**Typ.**	**Max.**	**Units**
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CHS}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{CSOFF}	Chip Select High time between transactions	2.0			µs
t_{NXT}	Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs

Table 12: Timing Information

Notes:

1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX805A MXB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX805A and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX806A will work with either polarity Serial Clock pulses.

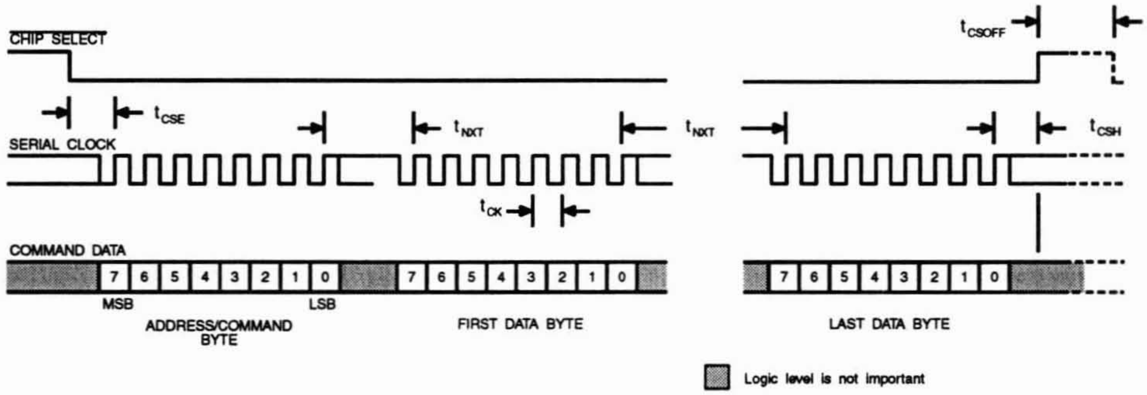
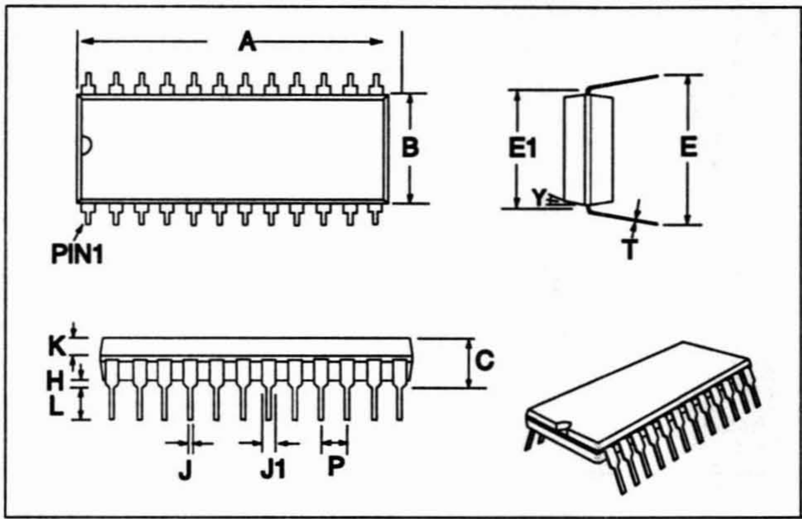

CHIP SELECT
t_{CSOFF}
t_{CSE}
t_{NXT}
t_{NXT}
t_{CSH}
SERIAL CLOCK
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
Logic level is not important

Figure 7: C-BUS Timing Information

7.2 Packages

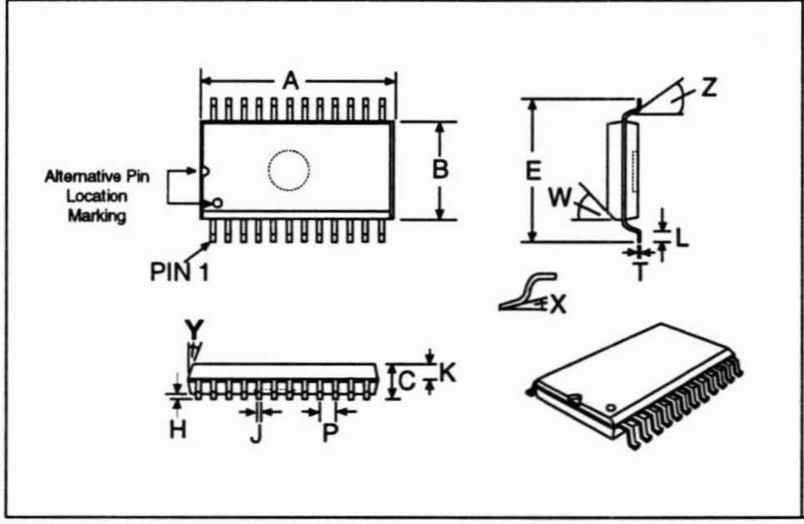


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PDIP Mechanical Outline: ***Order as part no. MX806AP***

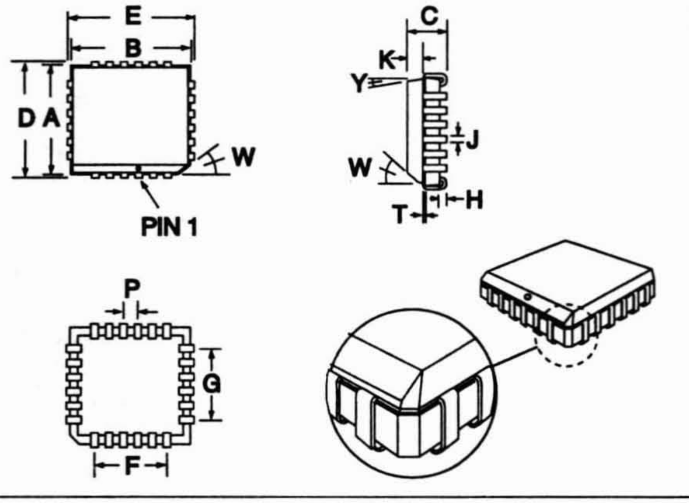


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin SOIC Mechanical Outline: ***Order as part no. MX806ADW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin PLCC Mechanical Outline: ***Order as part no. MX806ALH***

MX·COM, INC. MiXed Signal ICs

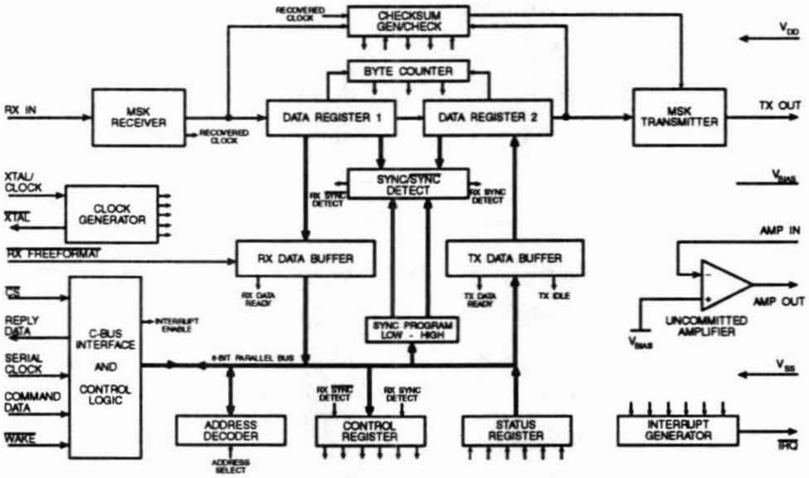
DATA BULLETIN

MX809 1200bps MSK Modem

PRELIMINARY INFORMATION

Features

- **Half-Duplex 1200bps MSK Modem operating under C-BUS control**
- **Software Selectable Checksum Generation and Error Checking in accordance with MPT1327**
- **Low Power Operation**
- **Member of DBS800 Family (C-BUS Compatible)**


RECOVERED CLOCK
CHECKSUM GEN/CHECK
VDD
BYTE COUNTER
RX IN
MSK RECEIVER
RECOVERED CLOCK
DATA REGISTER 1
DATA REGISTER 2
MSK TRANSMITTER
TX OUT
XTAL/CLOCK
XTAL
CLOCK GENERATOR
SYNC/SYNC DETECT
RX SYNC DETECT
RX SYNC DETECT
VBIAS
RX FREEFORMAT
RX DATA BUFFER
TX DATA BUFFER
AMP IN
RX DATA READY
TX DATA READY
TX IDLE
AMP OUT
CS
REPLY DATA
SERIAL CLOCK
COMMAND DATA
WAKE
C-BUS INTERFACE AND CONTROL LOGIC
INTERRUPT ENABLE
SYNC PROGRAM LOW - HIGH
UNCOMMITTED AMPLIFIER
VBIAS
8-BIT PARALLEL BUS
VSS
RX SYNC DETECT
RX SYNC DETECT
ADDRESS DECODER
ADDRESS SELECT
CONTROL REGISTER
STATUS REGISTER
INTERRUPT GENERATOR
IRQ

The MX809 is an intelligent, half-duplex 1200-baud MSK Modem, which operates under C-BUS control. This modem provides software selectable checksum generation and error checking in accordance with MPT1327.

In TX Mode the MX809 will:

1. a) Accept from the host and transmit 8-bit bytes of data as instructed (preamble, sync, address, and data), or
   b) Internally calculate and inset a 2 byte checksum based on the preceding 6 bytes f data, or
   c) Disable the internal checksum generator and continuously transmit the data supplied.
2. Transmit 1 hang-bit and go to TX idle when all loaded data bytes have been transmitted.

In RX Mode the MX809 will:

1. Detect and carry out bit synchronization within 16 bits.
2. a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and carry out frame synchronization. Data will then be output in 8-bit bytes via the RX Data Buffer.
   b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.
3. Make the incoming data directly available via the RX Data Buffer (RX Freeformat), overriding the synchronization requirements.

RX input timing is achieved by recovering an RX clock from the incoming data stream. Output tones are timed to the internally generated TX clock. Filter, register clocks, and transmit MSK tone frequencies are derived internally from the external Xtal or clock pulse input.

A 4.032MHz Xtal or clock input is required for compliance with the MPT1327 Signaling Specification. Note: All information contained in this data bulletin is specified using a 4.032MHz Xtal, 1200bps baud rate, with Mark and Space frequencies of 1200Hz and 1800Hz. The MX809 has a non-committed amplifier on-chip for general applications in the DBS 800 series.

The MX809 may be used with a 5.0V power supply and is available in the following packages:
24-pin PLCC (MX809LH), and 24-pin CERDIP (MX809J).

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MXCOM, Inc. reserves the right to change specifications at any time without notice.

1 Block Diagram

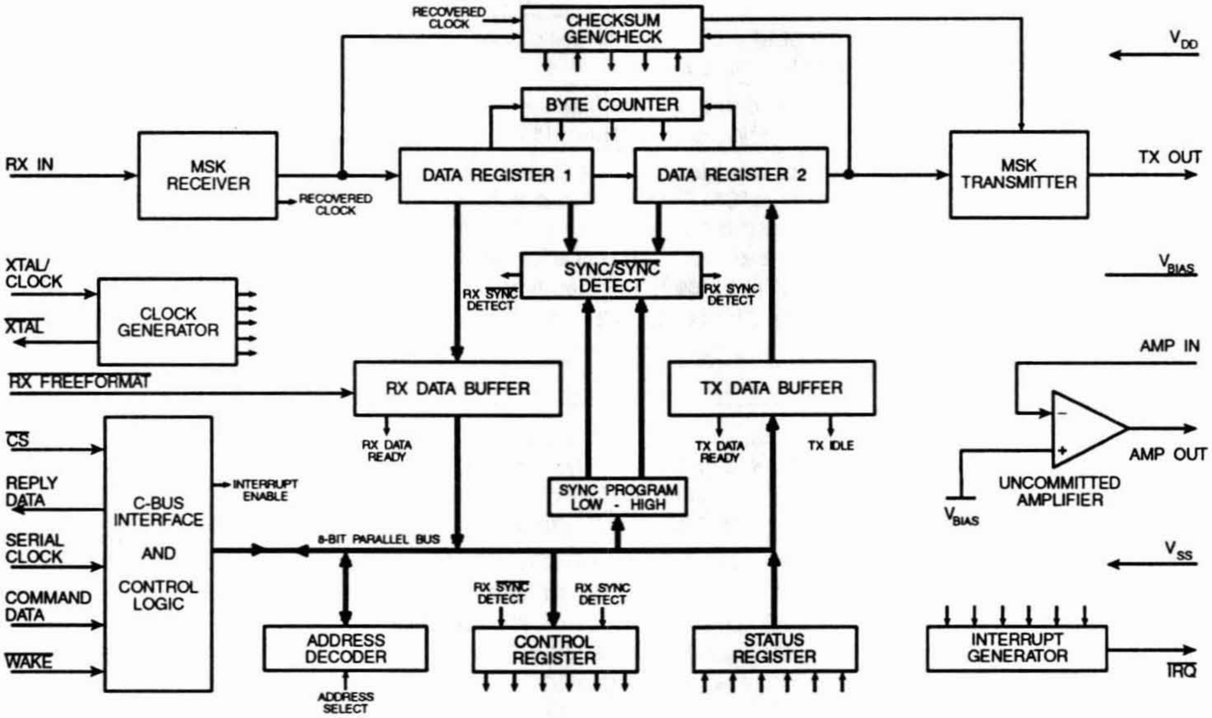

RECOVERED CLOCK
CHECKSUM GEN/CHECK
VDD
BYTE COUNTER
RX IN
MSK RECEIVER
RECOVERED CLOCK
DATA REGISTER 1
DATA REGISTER 2
MSK TRANSMITTER
TX OUT
XTAL/ CLOCK
XTAL
CLOCK GENERATOR
SYNC/SYNC DETECT
RX SYNC DETECT
RX SYNC DETECT
VBIAS
AMP IN
RX FREEFORMAT
RX DATA BUFFER
TX DATA BUFFER
CS
RX DATA READY
TX DATA READY
TX IDLE
AMP OUT
REPLY DATA
C-BUS INTERFACE AND CONTROL LOGIC
INTERRUPT ENABLE
SYNC PROGRAM LOW - HIGH
UNCOMMITTED AMPLIFIER
VBIAS
SERIAL CLOCK
8-BIT PARALLEL BUS
VSS
COMMAND DATA
RX SYNC DETECT
RX SYNC DETECT
WAKE
ADDRESS DECODER
CONTROL REGISTER
STATUS REGISTER
INTERRUPT GENERATOR
IRQ
ADDRESS SELECT

Figure 1: Block Diagram

2 Signal List

Pin	Signal	Description
1	$\overline{\text{Xtal}}$	This is the output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2. Inset
2	Xtal/Clock	This is the input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2. Inset
3	$\overline{\text{IRQ}}$	The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0". This is a "wire-or-able" output that enables the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open-drain output, and therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The conditions that cause interrupts are indicted in the Status Register and are shown in Table 2. The system $\overline{\text{IRQ}}$ line requires a pull-up resistor to V_{DD}.
4	N/C	
5	N/C	
6	$\overline{\text{RX Freeformat}}$	When this input is logic "0" in the RX Mode, it allows received data to be read from the RX Data Buffer via the Reply Data line without having to achieve byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime Bit is set or the modem is set to TX Mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pull-up resistor. **Note**: If this input is held at a logic "0" in the TX Mode, the RX Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the RX Mode, and RX Data Ready interrupt may be generated immediately (in this case the first byte of RX data should be ignored).
7	V_{BIAS}	The internal circuitry bias line, this is held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C3. See Figure 2.
8	Amp In	The inverting input to the on-chip uncommitted amplifier.
9	Amp Out	The output of the on-chip uncommitted amplifier.
10	RX In	This is the 1200 baud, 1200Hz/1800Hz received MSK signal input. The input signal to this pin must be AC coupled via capacitor C4. See Figure 2.
11	N/C	
12	V_{SS}	Negative Supply (GND)
13	TX Out	This is the 1200 baud, 1200Hz/1800Hz MSK TX output. When not transmitting data the output impedance of this pin is high. On power-up this output can be any level. A General Reset command is required to ensure that this output attains V_{BIAS} initially.
14	N/C	
15	N/C	
16	N/C	
17	Reply Data	This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the $\overline{\text{CS}}$ input. This 3-state output is held high impedance when not sending data to the microcontroller. See Section 6 and Section 7.1.4.
18	N/C	
19	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$. This is the 'C-BUS' data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Section 6 and Section 7.1.4.
20	Command Data	This is the 'C-BUS' serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first and LSB (bit 0) last, synchronized to the Serial Clock. See Section 6 and Section 7.1.4.

Pin	Signal	Description
21	Serial Clock	This is the 'C-BUS' serial Clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MSK Modem. See Section 6 and Section 7.1.4.
22	Address Select	This pin enables two MX809s to be used on the same C-BUS, providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Table 5 and Table 6.
23	$\overline{\text{Wake}}$	This input can be used to reactivate the MX809 from Powersave. The device will be in Powersave when both this pin and bit 2 of the Control Register are set to logic "1". Recovery from Powersave is achieved by putting either the $\overline{\text{Wake}}$ pin or the Powersave bit in the Control Register to logic "0". This allows MX809 activation by the microcontroller or an external signal, such as R.S.S.I. or Carrier Detect. See Table 3.
24	V_{DD}	Positive supply. A single +5.0V power supply is required. Levels and voltages within the MSK Modem are dependent upon this supply.

Table 1: Signal List

TX Idle	RX Data Ready	TX Data Ready
RX SYNC Detect		RX Sync Detect
Interrupt outputs can be disabled by bit 3 of the Control Register		

Table 2: $\overline{\text{IRQ}}$ Conditions

Powersave (CR bit 2)	$\overline{\text{Wake}}$	MX809 Condition
1	1	Powersave
0	1	Enabled
1	0	Enabled
0	0	Enabled

Table 3: $\overline{\text{Wake}}$ and Powersave Conditions

3 External Components

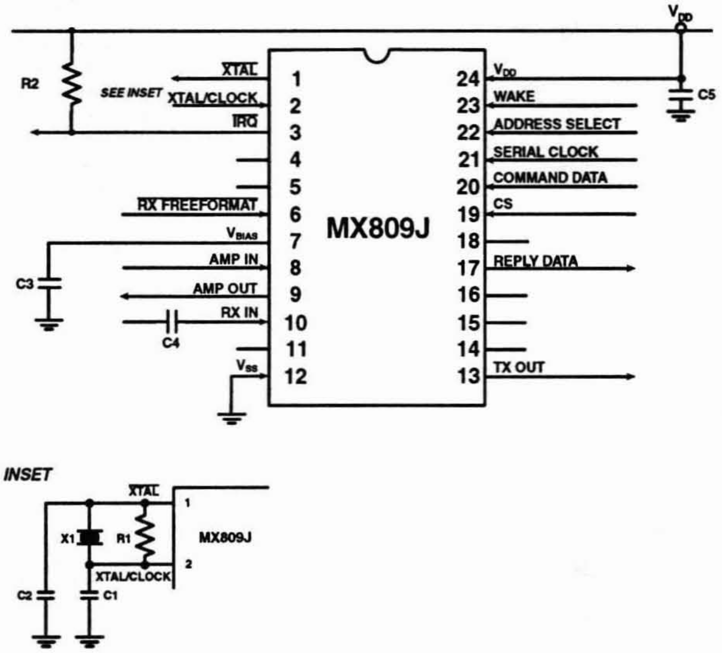

V_DD
R2
SEE INSET
XTAL
XTAL/CLOCK
IRQ
RX FREEFORMAT
V_BIAS
AMP IN
AMP OUT
RX IN
C3
C4
V_SS
1
2
3
4
5
6
7
8
9
10
11
12
MX809J
24
23
22
21
20
19
18
17
16
15
14
13
V_DD
WAKE
ADDRESS SELECT
SERIAL CLOCK
COMMAND DATA
CS
REPLY DATA
TX OUT
C5
INSET
XTAL
X1
R1
MX809J
XTAL/CLOCK
C2
C1

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
R2		22.0KΩ	±10%
C1	1	33pF	±20%
C2	1	33pF	±20%
C3		1.0µF	±20%
C4		0.1µF	±20%
C5		1.0µF	±20%
X1	1	4.032MHz	

Table 4: Recommended External Components

Recommended External Component Notes:

1. Xtal circuit capacitors C1 (CD) and C2 (CG) shown in Inset 2 are recommended in accordance with MX-COM's Crystal Oscillator Application Note.

4 General Description

The MX809 is an intelligent, half-duplex 1200-baud MSK Modem, which operates under C-BUS control. This modem provides software selectable checksum generation and error checking in accordance with MPT1327.

In TX Mode the MX809 will:

1. a) Accept from the host and transmit 8-bit bytes of data as instructed (preamble, sync, address, and data), or
   b) Internally calculate and inset a 2 byte checksum based on the preceding 6 bytes of data, or
   c) Disable the internal checksum generator and continuously transmit the data supplied.
2. Transmit 1 hang-bit and go to TX idle when all loaded data bytes have been transmitted.

In RX Mode the MX809 will:

1. Detect and carry out bit synchronization within 16 bits.
2. a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and carry out frame synchronization. Data will then be output in 8-bit bytes via the RX Data Buffer.
   b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.
3. Make the incoming data directly available via the RX Data Buffer (RX Freeformat), overriding the synchronization requirements.

RX input timing is achieved by recovering an RX clock from the incoming data stream. Output tones are timed to the internally generated TX clock. Filter, register clocks, and transmit MSK tone frequencies are derived internally from the external Xtal or clock pulse input.

A 4.032MHz Xtal or clock input is required for compliance with the MPT1327 Signaling Specification. Note: All information contained in this data bulletin is specified using a 4.032MHz Xtal, 1200bps baud rate, with Mark and Space frequencies of 1200Hz and 1800Hz. The MX809 has a non-committed amplifier on-chip for general applications in the DBS 800 series.

5 Controlling Protocol

Control of the functions within the MX809 MSK Modem is by a group of Address/Commands and appended data instructions from the system microcontroller. Two separate MSK Modems can be addressed. The use of these A/Cs is detailed in the following paragraphs and tables.

Command Assignment		**Address/Command Binary**		**Command Data**
	HEX	**MSB LSB**		
General Reset	01	00000001		Control Register bits set to logic "0"
Write to Control Register	40	01000000	+	1 byte instruction to Control Register
Read Status Register	41	01000001	+	1 byte reply from Status Register
Read RX Data Buffer	42	01000010	+	1 byte of data from RX Data Buffer
Write to TX Data Buffer	43	01000011	+	1 byte of data to TX Data Buffer
Write to SYNC Program	44	01000100	+	2 bytes of SYNC Word to SYNC Program. Register

Table 5: Modem No. 1 C-BUS Address/Commands – (Address Select input at a logic "0")

5.1 Address/Commands

Instructions and data transactions to and from the MX809 consist of an Address/Command (A/C) byte followed by either further instructions or data, or a Status or RX Data Reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register [40_H (48_H)].

Reporting of the MX809 configuration is by reading the Status Register [41_H (49_H)]. Instructions and data are transferred via C-BUS in accordance with the timing information given in Figure 11.

Data to be transmitted as MSK is sent to the TX Data Buffer via the Command Data line. Received data is read from the RX Data buffer via the Reply Data line.

Instructions and data transactions to and from this device are preceded by the relevant A/C.

C-BUS allocations for the MX809 are shown in Table 5 and Table 6.

Command Assignment		**Address/Command Binary**		**Command Data**
	HEX	**MSB LSB**		
General Reset	01	00000001		Control Register bits set to logic "0"
Write to Control Register	48	01001000	+	1 byte instruction to Control Register
Read Status Register	49	01001001	+	1 byte reply from Status Register
Read RX Data Buffer	4A	01001010	+	1 byte of data from RX Data Buffer
Write to TX Data Buffer	4B	01001011	+	1 byte of data to TX Data Buffer
Write to SYNC Program	4C	01001100	+	2 bytes of SYNC Word to SYNC Program Register

Table 6: Modem No. 2 C-BUS Address/Commands – (Address Select input at a logic "1")

5.2 Address Select

This input allows 2 MSK Modems on the same BUS, using the correct addressing.

When operating in a system using 2 MSK Modems, one MSK Modem is designated No. 1 and requires its Address Select input to be held at a logic "0". The second Modem (No. 2) requires its Address select input to be held at logic "1".

All C-BUS transactions with Modem 1 will use Address/Command allocations 40_H to 44_H (Table 5) and transactions with Modem 2 will use 48_H to $4C_H$ (Table 6).

For explanation purposes, further descriptions of MX809 MSK Modem internal register functions will deal primarily with MSK Modem No. 1 (Address Select at logic "0").

5.3 Write to Control Register

This "Write Only" register directs the Modem's operation.

$\overline{\text{SYNC}}$: When set, this bit enables $\overline{\text{SYNC}}$ Word detection. It is cleared on a successful $\overline{\text{SYNC}}$ Word detection.

SYNC Prime: When set, this bit enables SYNC Word detection. It is cleared on a successful SYNC Word detection.

Interrupt Enable: When set, this bit allows interrupts to be output by the MX809 on the $\overline{\text{IRQ}}$ line.

Powersave: Used in conjunction with the $\overline{\text{Wake}}$ input (see Section 2) to control the Powersave state of the MX809.

Checksum Enable: When set:

In TX: A 2-byte checksum is generated and transmitted after every 6 bytes transmitted.

In RX: After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the RX Checksum True bit in the Status Register is set to a logic "1". When this bit is a logic "0" no checksum are generated or checked.

Note: Checksum operation is inhibited during the SYNC / $\overline{\text{SYNC}}$ search period.

Setting	Control bits
MSB	**Transmitter first**
Bit 7	Not Used
	Set to "0"
6	Not Used
	Set to "0"
5	**$\overline{\text{SYNC}}$ Prime**
0 1	 Primed
4	**SYNC Prime**
0 1	 Primed
3	**Interrupt Enable**
0 1	Disable Enable
2	**Powersave**
0 1	Normal Operation Powersave
1	**Checksum Enable**
0 1	Disable Enable
0	**RX/TX Mode**
0 1	RX TX

Table 7: Control Register

5.4 RX Data buffer – "Read RX Data Buffer"

This "Read Only" register contains the last byte of data received from the Data Register. Data is received Bit 7 (MSB) first.

MSB							**LSB**
7	6	5	4	3	2	1	0
RX Data Buffer							

5.5 TX Data Buffer -- "Write to TX Data Buffer"

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) is transmitted first.

MSB							LSB
7	6	5	4	3	2	1	0
TX Data Buffer							

5.6 SYNC Program -- "Write to SYNC Program"

This "Write Only" register is loaded with the required SYNC word. This word (or its opposite logic sense, $\overline{\text{SYNC}}$) is compared with the received synchronization word. If the required SYNC Word is less that 16bits, the remaining bits must be programmed as preamble (10101010...etc). Bit 15 (MSB) is loaded first.

MSB				Byte 1							Byte 2				LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC High								SYNC Low							

5.7 Read Status Register

This "Read Only" register indicated the source of MX809 interrupts ($\overline{\text{IRQs}}$).

RX $\overline{\text{SYNC}}$ Detect: This is set and an Interrupt is generated when the correct $\overline{\text{SYNC}}$ Word is detected (if $\overline{\text{SYNC}}$ Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{\text{RX}}$/TX to logic "1".

RX SYNC Detect: This is set and an Interrupt is generated when the correct SYNC Word is detected (if SYNC Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{\text{RX}}$/TX to logic "1".

TX Idle: This is set and an Interrupt is generated when all loaded TX data and 1 "hang-bit" have been transmitted.

It is cleared by (1) writing to the TX Data Buffer, and (2) setting $\overline{\text{RX}}$/TX to logic "0".

TX Data Ready: This is set and an Interrupt generated indicating that a byte of data should be written to the TX Data Buffer.

It is cleared by (1) reading the Status Register and writing a byte of data to the TX Data Buffer, and (2) setting $\overline{\text{RX}}$/TX to logic "0".

RX Data Ready: When this is set and an Interrupt generated, it indicates that the RX Data Buffer is full, and that a byte of data is to be read from the RX Data buffer. This must be read within 8 bit periods.

It is cleared by (1) reading the Status Register and the RX Data buffer, and (2) setting the $\overline{\text{RX}}$/TX to logic "1"/

RX Checksum True: This is set and an Interrupt is generated by a successful comparison of the received and self-generated checksums.

It is cleared by (1) reading the Status Register and the RX Data Buffer, and (2) $\overline{\text{RX}}$/TX being taken to logic "1"

Reading	**Status Bits**
MSB	**Received First**
Bit 7	**Undefined**
0	"0" or
1	"1"
6	**Undefined**
0	"0" or
1	"1"
5	**RX $\overline{\text{SYNC}}$ Detect**
0	
1	$\overline{\text{SYNC}}$
4	**RX SYNC Detect**
0	
1	SYNC
3	**TX Idle**
0	
1	Idle
2	**TX Data Ready**
0	
1	TX Date Ready
1	**RX Checksum True**
0	
1	True
0	**RX Data Ready**
0	
1	RX Data Ready

Table 8: Status Register

5.8 Interrupt Request

The conditions that cause interrupts to be output (if enabled by the Control Register) from the MX809 are:

TX Idle
TX Data Ready
RX $\overline{\text{SYNC}}$ Detect
RX Data Ready
RX SYNC Detect

The Status Register should be read to find the cause of the interrupt. Interrupts are cleared by (1) reading the Status Register, or (2) changing the state of the $\overline{\text{RX}}$/TX bit.

5.9 General Reset

Upon power-up, the bits in the MX809 Mode register and buffer will be random (either "0" or "1"). The General Reset command (01_H) will "reset" all microcircuits in the C-BUS and had the following effect on the MX809.

All bits in the Control Register will be set to logic "0". The Tx Out output will be set to V_{BIAS}.

Note: The Status register, RX Data Buffer, TX Data Buffer, and SYNC Program register are not affected by the General Reset Command.

6 Application

6.1 Checksum Generation and Checking

6.1.1 Generation

The checksum generator takes the 48 bits from the 6 bytes loaded into the TX Data Buffer and divides them into modulo-2 by the generating polynomial:

$$x^{15} + x^{14} + x^{13} + x^{11} + x^{4} + x^{2} + x^{1}$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16 bit word is used as the "Checksum".

6.1.2 Checking

The checksum checker does two things:

1. It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo-2 by the generating polynomial:

$$x^{15} + x^{14} + x^{13} + x^{11} + x^{4} + x^{2} + x^{1}$$

2. The 15 bits remaining in the polynomial divider are checked to make sure that they are all zero.
3. It generates an even parity bit from the first 63 bits of a received message and compares this bit with the received parity (bit 64).
   If the 15 bits in the polynomial divider are all zero and the two parity bits are equal, then the RX Checksum True (Status Register bit 1) is set.

6.2 Modem Performance

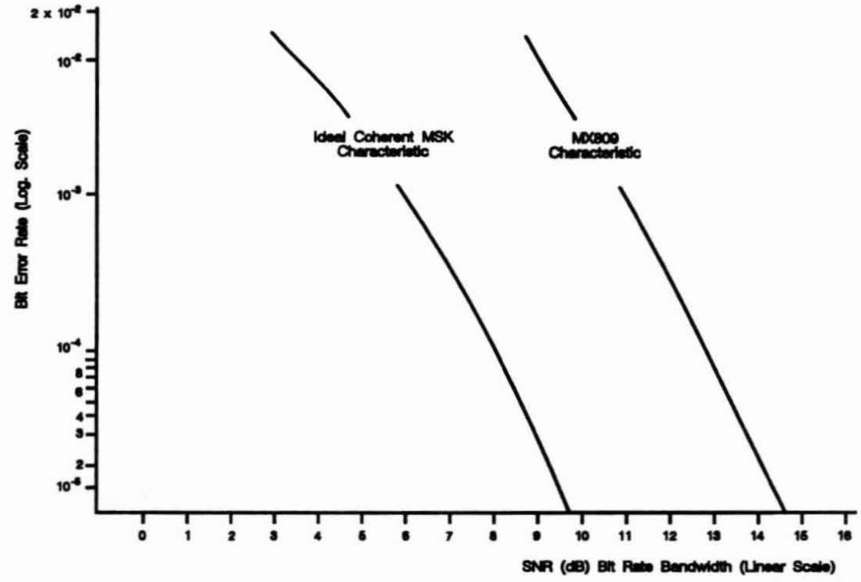


Figure 3: Bit Error Rate vs. Signal-to-Noise Ratio

6.3 Modem Timing Information

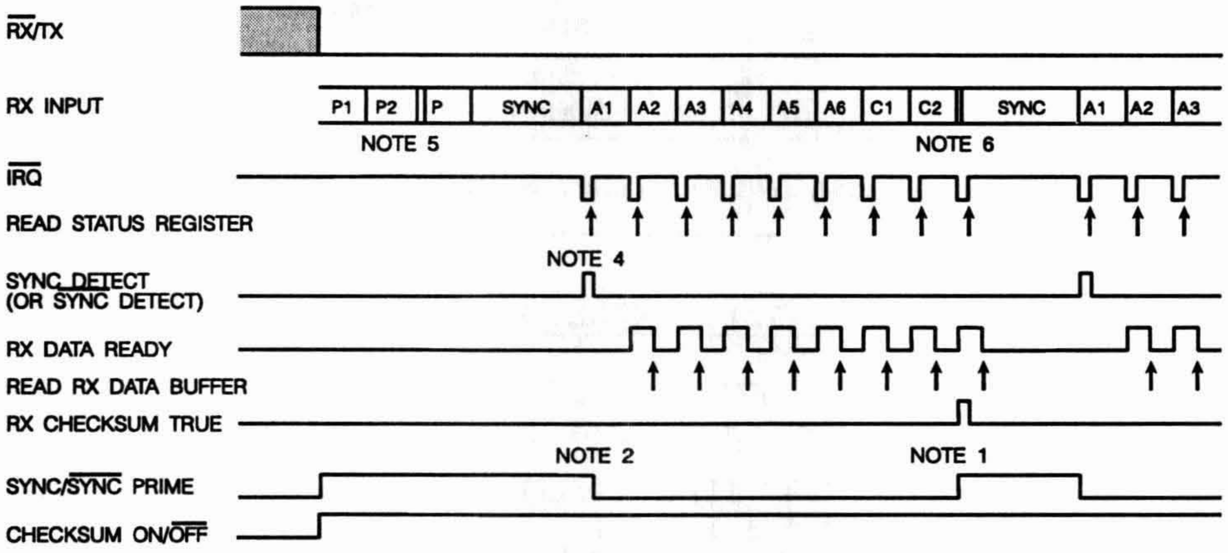

RX/TX
RX INPUT
P1
P2
P
SYNC
A1
A2
A3
A4
A5
A6
C1
C2
SYNC
A1
A2
A3
NOTE 5
NOTE 6
IRQ
READ STATUS REGISTER
NOTE 4
SYNC DETECT
(OR SYNC DETECT)
RX DATA READY
READ RX DATA BUFFER
RX CHECKSUM TRUE
NOTE 2
NOTE 1
SYNC/SYNC PRIME
CHECKSUM ON/OFF

Figure 4: Modem Timing

Notes:

1. The SYNC and $\overline{\text{SYNC}}$ detector searches the incoming bit stream starting at the end of the byte in which SYNC / $\overline{\text{SYNC}}$ Prime was set.
2. After detection of a SYNC / $\overline{\text{SYNC}}$ word, the SYNC / $\overline{\text{SYNC}}$ Prime bits automatically go low (control bits 5 and 6: detector off.
3. The checksum checker is inhibited during the time SYNC / $\overline{\text{SYNC}}$ search is operating.
4. The Status Register will indicate whether SYNC or $\overline{\text{SYNC}}$ was detected here.
5. Any number of preamble bits can occur here.
6. Any number of bits can occur here.
7. $\overline{\text{RX Freeformat}}$ set high.

6.4 TX Timing

A – Address bytes C – Checksum bytes D – Data bytes H – Hang bit P – Preamble bytes	▨ - Don't care state TX only – In TX, Preamble, and SYNC are loaded as data from the microcontroller.

6.4.1 TX More Than One Message, SYNC Before Every Message, TX Checksum Enabled

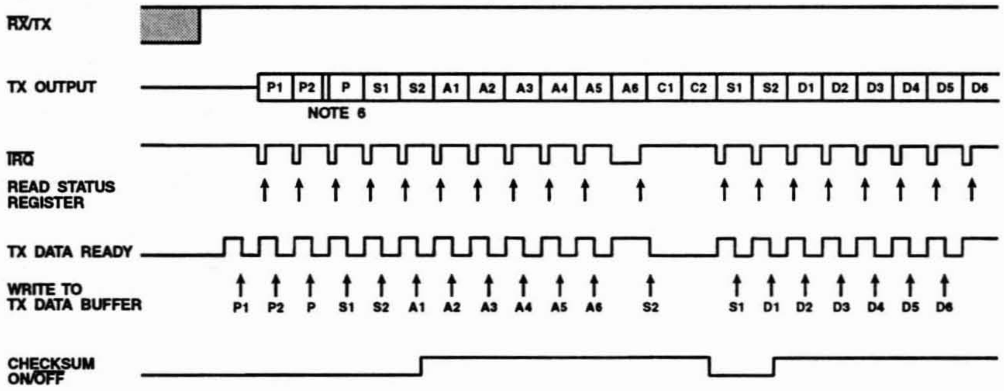

RX/TX
TX OUTPUT
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6 C1 C2 S1 S2 D1 D2 D3 D4 D5 D6
NOTE 6
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6 S2 S1 D1 D2 D3 D4 D5 D6
CHECKSUM ON/OFF

Figure 5: TX More Than One Message, SYNC Before Every Message, TX Checksum Enabled

Notes:

1. Preamble and SYNC bytes are loaded as data from the microcontroller.
2. The TX output will be held at bias level when no data is being transmitted.
3. TX byte synchronization is established by loading of the first preamble byte from the microcontroller.
4. Checksum must be turned off during preamble and SYNC words.
5. When $\overline{RX}$/TX is low, TX output is at bias.
6. Any number of preamble bytes can occur here.

6.4.2 TX More Than One Message, TX Checksum Not Enabled.

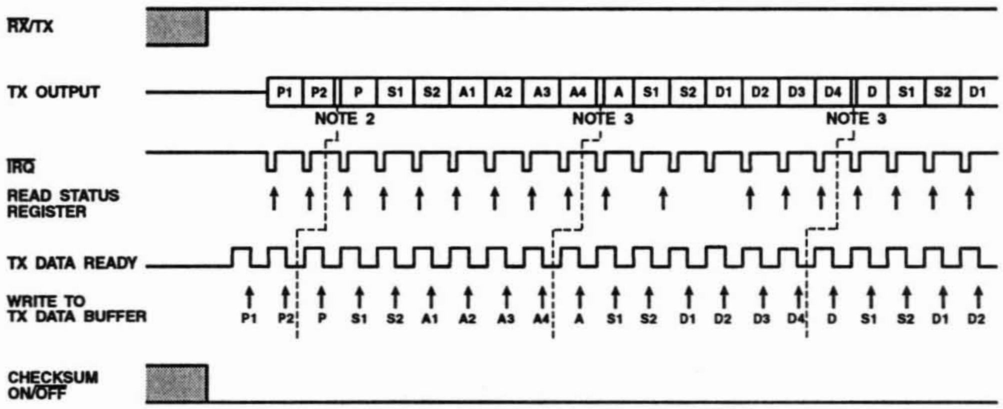
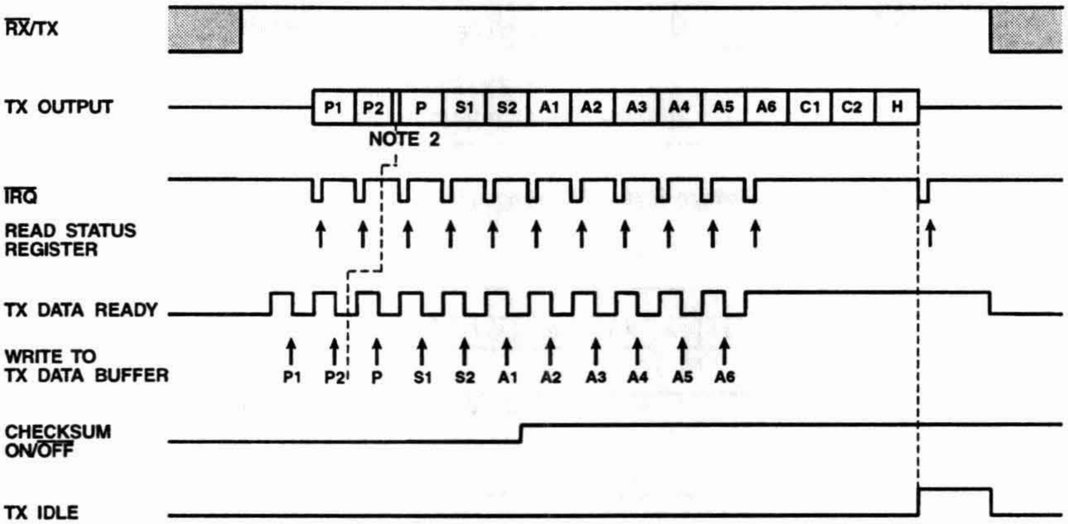

RX/TX
TX OUTPUT
P1 P2 P S1 S2 A1 A2 A3 A4 A S1 S2 D1 D2 D3 D4 D S1 S2 D1
NOTE 2
NOTE 3
NOTE 3
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1 P2 P S1 S2 A1 A2 A3 A4 A S1 S2 D1 D2 D3 D4 D S1 S2 D1 D2
CHECKSUM ON/OFF

Figure 6: TX More Than One Message, TX Checksum Not Enabled.

Notes:

1. Preamble, SYNC words and checksums are supplied by the microcontroller in this format as data bytes.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.

6.4.3 TX One Message, TX Checksum Enabled



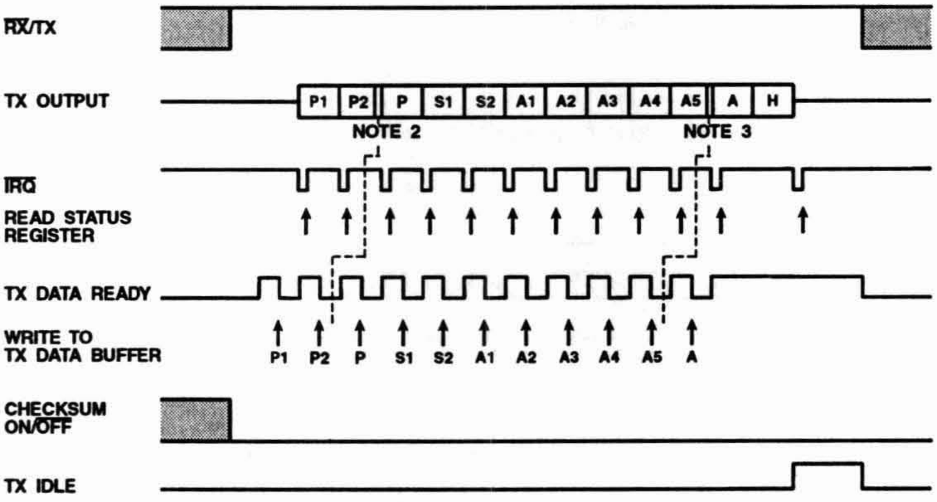
RX/TX
TX OUTPUT
P1
P2
P
S1
S2
A1
A2
A3
A4
A5
A6
C1
C2
H
NOTE 2
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1
P2
P
S1
S2
A1
A2
A3
A4
A5
A6
CHECKSUM ON/OFF
TX IDLE

Figure 7: TX One Message, TX Checksum Enabled

Notes:

1. H is the "Hangover bit" (Logic1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Transmission terminates after C1, C2, and H. Termination occurs when no further data bytes are written to the TX Data Buffer.

6.4.4 TX One Message, TX Checksum Not Enabled.



RX/TX
TX OUTPUT
P1
P2
P
S1
S2
A1
A2
A3
A4
A5
A
H
NOTE 2
NOTE 3
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1
P2
P
S1
S2
A1
A2
A3
A4
A5
A
CHECKSUM ON/OFF
TX IDLE

Figure 8: TX One Message, TX Checksum Not Enabled

Notes:

1. H is the "Hangover bit" (Logic1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.
4. Transmission terminates when no further data bytes are loaded into the TX Data Buffer.

6.5 RX Timing

A – Address bytes C – Checksum bytes D – Data bytes H – Hang bit P – Preamble bytes	▨ - Don't care state TX only – In TX, Preamble, and SYNC are loaded as data from the microcontroller.

6.5.1 RX SYNC / $\overline{\text{SYNC}}$ Required Before Every Message, Rx Checksum Not Enabled

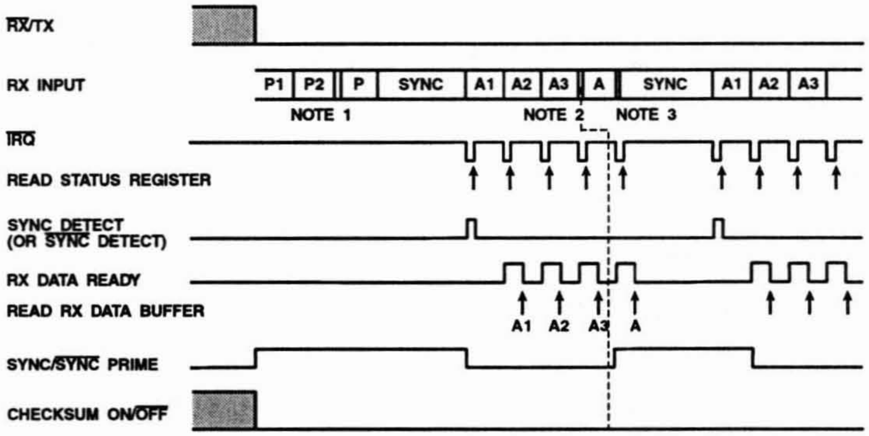

$\overline{\text{RX}}$/TX
RX INPUT
P1
P2
P
SYNC
A1
A2
A3
A
SYNC
A1
A2
A3
NOTE 1
NOTE 2
NOTE 3
$\overline{\text{IRQ}}$
READ STATUS REGISTER
SYNC DETECT (OR $\overline{\text{SYNC}}$ DETECT)
RX DATA READY
READ RX DATA BUFFER
A1
A2
A3
A
SYNC/$\overline{\text{SYNC}}$ PRIME
CHECKSUM ON/$\overline{\text{OFF}}$

Figure 9: RX SYNC / $\overline{\text{SYNC}}$ Required Before Every Message, RX Checksum not Enabled

Notes:

1. Any number of preamble bits can occur here.
2. Any number of address/data bytes can occur here.
3. Any number of bits can occur here
4. $\overline{\text{RX Freeformat}}$ set high.

6.5.2 RX Additional Data Follows Initial Address (6 Data & 2 Checksum Bytes) Data, RX checksum Enabled

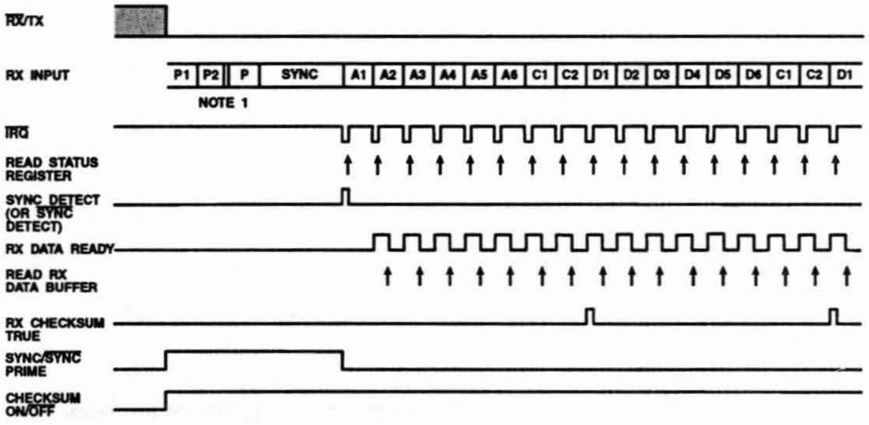

$\overline{\text{RX}}$/TX
RX INPUT
P1
P2
P
SYNC
A1
A2
A3
A4
A5
A6
C1
C2
D1
D2
D3
D4
D5
D6
C1
C2
D1
NOTE 1
$\overline{\text{IRQ}}$
READ STATUS REGISTER
SYNC DETECT (OR $\overline{\text{SYNC}}$ DETECT)
RX DATA READY
READ RX DATA BUFFER
RX CHECKSUM TRUE
SYNC/$\overline{\text{SYNC}}$ PRIME
CHECKSUM ON/$\overline{\text{OFF}}$

Figure 10: RX Additional Data Follows Initial Address (6 Data & 2 Checksum Bytes) Data , RX Checksum Enabled

Notes:

1. Any number of preamble bits can occur here.
2. $\overline{\text{RX Freeformat}}$ set high.

7 Performance Specifications

7.1 Electrical Specifications

7.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
J / LH Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 9: Absolute Maximum Ratings

7.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	**Min.**	**Typ.**	**Max.**	**Units**
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.032		MHz

Table 10: Operating Limits

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.032MHz, Audio Level 0dB ref. = 308mV_{RMS} @ 1kHz
Bit Rate = 1200bps

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
Enabled			5.0		mA
Powersave			2.0		mA
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5			V
Input Logic "0"	1			1.5	V
Output Logic "1" (I_{OH} = -120µA)	2	4.6			V
Output Logic "0" (I_{OH} = 360µA)	2, 3			0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	1			1.0	µA
Digital Input Capacitance	1			7.5	pF
Tri-State "OFF" Leakage Current	8	-4.0		4.0	µA
Analog Impedance					
Input Impedance		100			kΩ
Output Impedance					
Transmitting Data			6.0	10.0	kΩ
Not Transmitting Data			1.0		kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0			MΩ
R_{OUT}		5.0			kΩ
Gain			15.0		dB
Frequency	4		4.032		MHz
Receiver					
Signal Input Levels	5	-9.0	-2.0	10.5	dB
Bit Error Rate					
At 12dB SNR			7.0		10^{-4}
At 20dB SNR			1.0		10^{-8}
Synchronization at 12dB SNR	6				
Probability of Bit 8 being correct			99.0		%
Probability of Bit 16 being correct			99.5		%

	Notes	Min.	Typ.	Max.	Units
Transmitter					
Output Level			0		dB
Output Level Variation		-1.0		1.0	dB
Output Distortion			3.0	5.0	%
Third Harmonic Distortion			2.0	3.0	%
Logic "1" Frequency	7		1200		Hz
Logic "0" Frequency	7		1800		Hz
Isochronous Distortion					
1200Hz – 1800Hz			25.0	40.0	µs
1800Hz – 1200Hz			20.0	40.0	µs
Uncommitted Amplifier					
Bandwidth			200		kHz
Gain			50.0		dB
Input Impedance		1.0			
Output Impedance				10.0	kΩ

Table 11: Operating Characteristics

Operating Characteristics Notes:

1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$, and $\overline{\text{CS}}$.
2. Reply Data output.
3. $\overline{\text{IRQ}}$ output
4. For baud rate specified (1200 baud)
5. Signal-to-Noise Ratio = 50dB
6. The response time is measured using 10101010…101 signal input pattern at 230mV$_{RMS}$ (-2.5dB) with noise.
7. Dependant upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs for $V_{SS} < V_{OUT} < V_{DD}$.

7.1.4 Timing

C-BUS Timing		Min.	Typ.	Max.	Units
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CHS}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{HIZ}	Chip Select High to Reply Data High -Z			2.0	
t_{CSOFF}	Chip Select High time between transactions	2.0			µs
t_{NXT}	Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs

Table 12: Timing Information

Notes:

1. Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the peripheral MXB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.

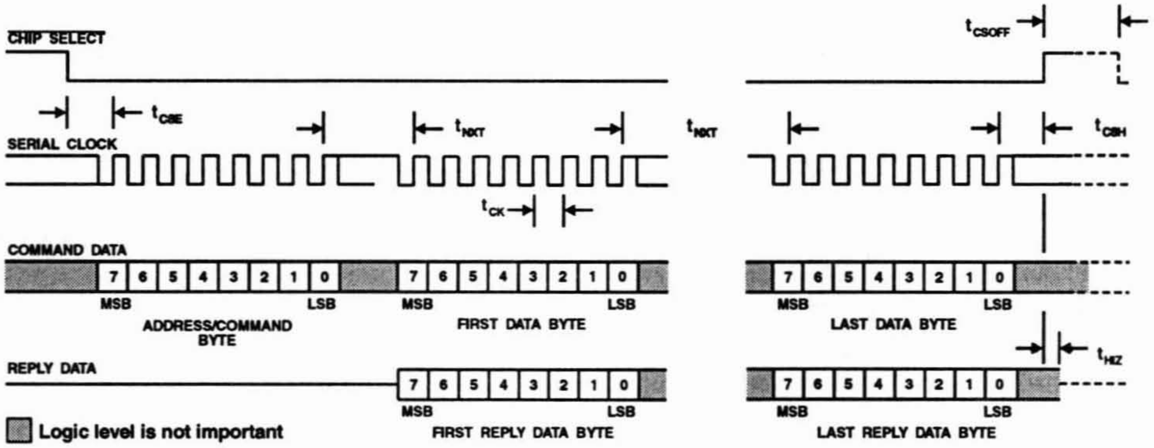
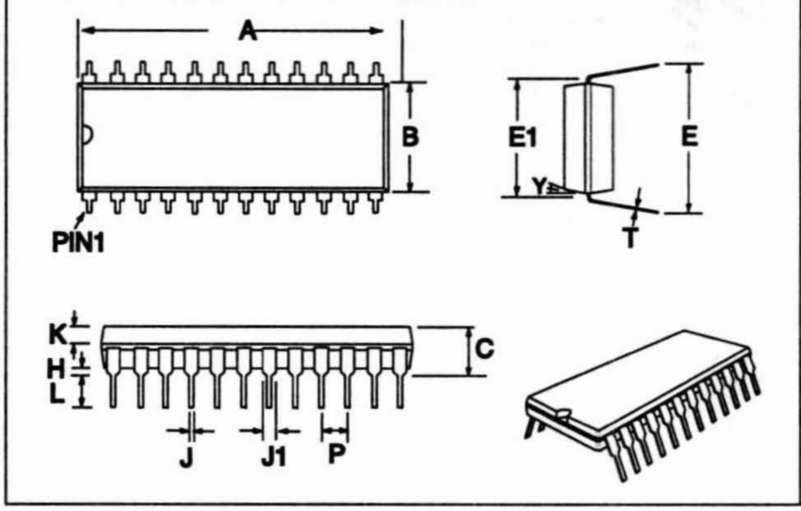

CHIP SELECT
t_{CSOFF}
t_{CSE}
SERIAL CLOCK
t_{NXT}
t_{NXT}
t_{CSH}
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
▨ Logic level is not important

Figure 11: C-BUS Timing Information

7.2 Packages

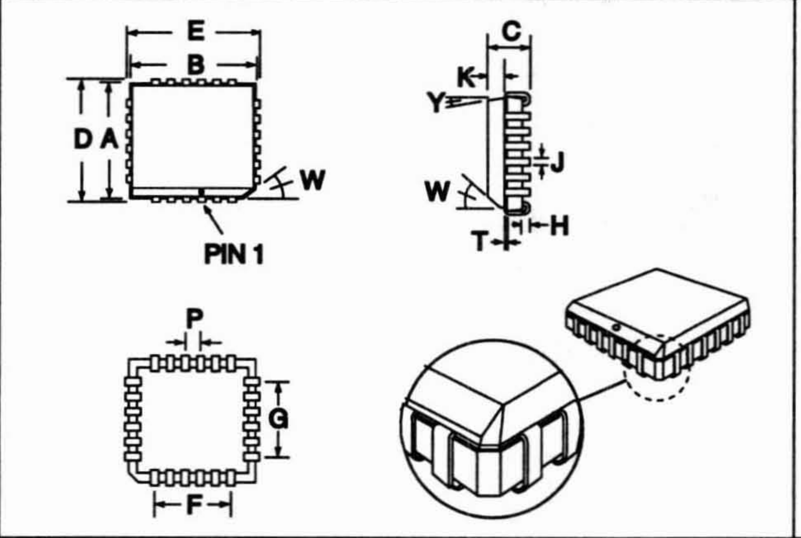


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin CERDIP Mechanical Outline: ***Order as part no. MX809J***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin PLCC Mechanical Outline: ***Order as part no. MX809LH***

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX818 CTCSS Signaling Processor

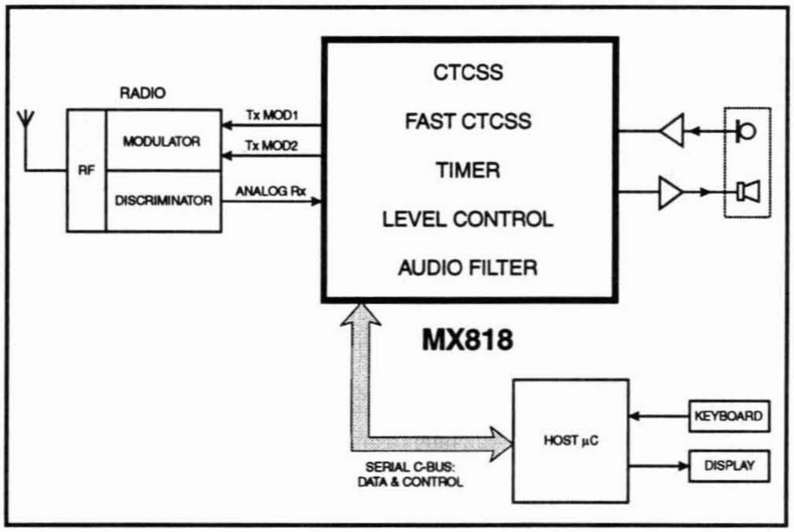
PRELIMINARY INFORMATION

Features

- **Fast CTCSS Detection**
- **Non Predictive Tone Detection**
- **Low Power 3.3V/5.0V Operation**
- **Variable Gain Audio Filter**
- **Programmable:**
  - **Modulator Drivers**
  - **Tone Decoder**
  - **Tone Encoder**
- **Pin compatible with enhanced function MX828**
- **Full control via 4-Wire Serial Interface**

Applications

- **Radio Systems Requiring Sub-Audible Signaling**
  - **Trunking Control**
  - **Selective Calling**
  - **Group Calling**
- **Increased Efficiency**
  - **Scanning Systems**
  - **Trunking Systems**



The MX818 is a low power CTCSS Signal Processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling and Group Calling applications. The MX818 is full duplex and offers many advanced features to assist in the operation of new CTCSS based systems including: programmable tone decoders to facilitate the decoding of between 1 and 15 programmable CTCSS tones, a CTCSS Fast/Predictive detector which may respond to a single programmed tone in less than 60ms, a high resolution tone encoder that will accurately generate CTCSS tones, and High and Low pass filters for CTCSS and Voice Band signals. The MX818 also provides on chip audio summation and digitally adjustable modulation drivers to facilitate design integration and reduce part count.

The MX818 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP(MX818DS), 24-pin SOIC (MX818DW), and 24-pin PDIP (MX818P).

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1. Block Diagram

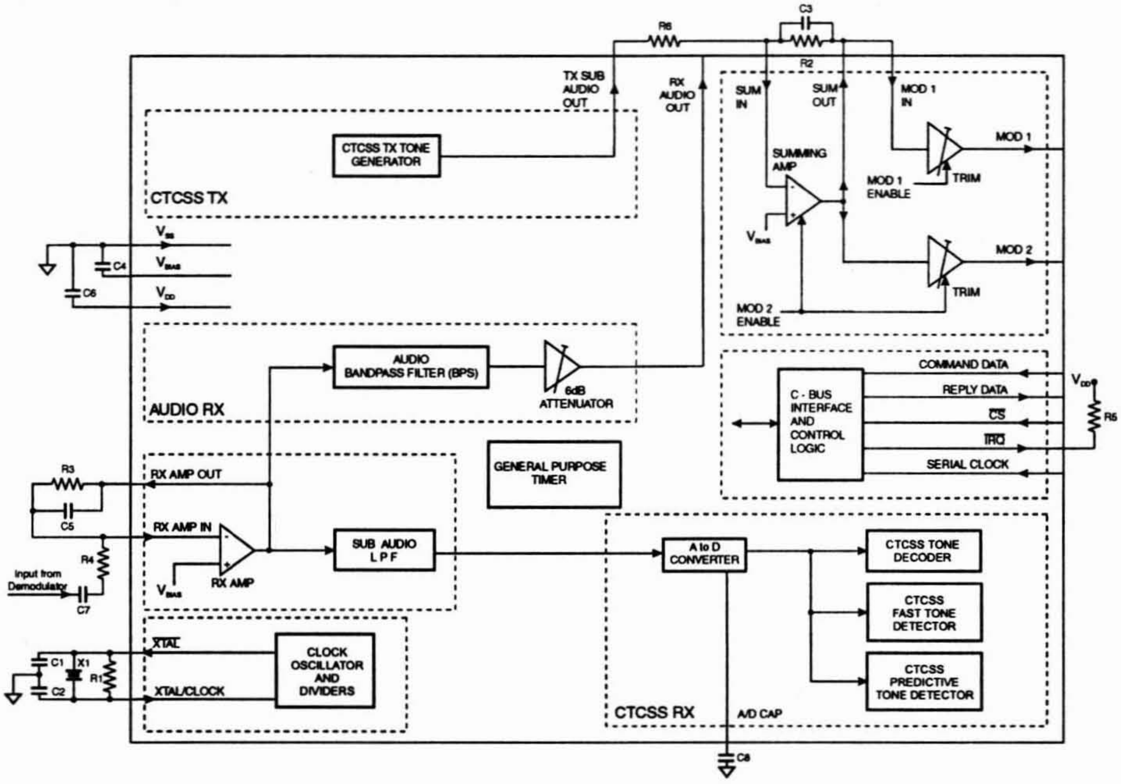

R6
C3
R2
TX SUB AUDIO OUT
RX AUDIO OUT
SUM IN
SUM OUT
MOD 1 IN
CTCSS TX TONE GENERATOR
CTCSS TX
SUMMING AMP
MOD 1
MOD 1 ENABLE
TRIM
V_{BIAS}
MOD 2
TRIM
MOD 2 ENABLE
V_{SS}
C4
V_{BIAS}
C6
V_{DD}
AUDIO BANDPASS FILTER (BPS)
6dB ATTENUATOR
AUDIO RX
C - BUS INTERFACE AND CONTROL LOGIC
COMMAND DATA
REPLY DATA
$\overline{CS}$
$\overline{IRQ}$
SERIAL CLOCK
V_{DD}
R5
GENERAL PURPOSE TIMER
R3
RX AMP OUT
C5
RX AMP IN
R4
Input from Demodulator
C7
V_{BIAS}
RX AMP
SUB AUDIO LPF
A to D CONVERTER
CTCSS TONE DECODER
CTCSS FAST TONE DETECTOR
CTCSS PREDICTIVE TONE DETECTOR
$\overline{XTAL}$
XTAL/CLOCK
CLOCK OSCILLATOR AND DIVIDERS
C1
X1
R1
C2
CTCSS RX
A/D CAP
C8

Figure 1: Device Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 4
4	COMMAND DATA	input	The C-BUS serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 4
5	REPLY DATA	output	The C-BUS serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 4
6	$\overline{\text{CS}}$	input	The C-BUS data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Figure 4.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic 0. This is a wire-ORable output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic 0 when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	N/C		No internal connection. Do not make any connection to these pin
9	N/C		No internal connection. Do not make any connection to these pin
10	A/D CAP	output	An internal reference voltage for the A to D, decoupled to V_{SS} by an external capacitor.
11	N/C		No internal connection. Do not make any connection to this pin.
12	V_{SS}	power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	The output of the Rx input amplifier and the input to the audio filter section.
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	N/C		No internal connection. Do not make any connection to this pin.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier, internally tied to input of MOD2
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

3. External Components

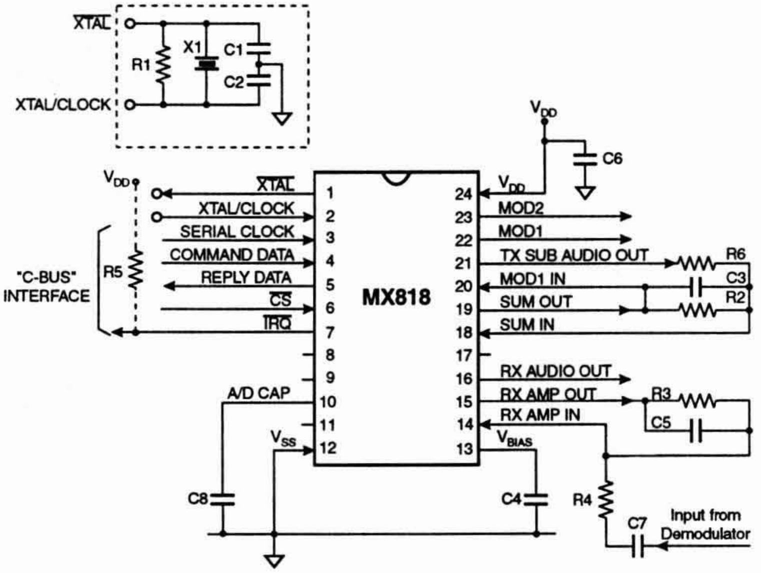

XTAL
XTAL/CLOCK
R1
X1
C1
C2
VDD
C6
"C-BUS" INTERFACE
R5
XTAL
XTAL/CLOCK
SERIAL CLOCK
COMMAND DATA
REPLY DATA
CS
IRQ
A/D CAP
VSS
MX818
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
MOD2
MOD1
TX SUB AUDIO OUT
MOD1 IN
SUM OUT
SUM IN
RX AUDIO OUT
RX AMP OUT
RX AMP IN
VBIAS
R6
C3
R2
R3
C5
C8
C4
R4
C7
Input from Demodulator

Figure 2: Recommended External Components

R1		1MΩ	±5%
R2	Note 2	100kΩ	±10%
R3	Note 3	100kΩ	±10%
R4	Note 3, 4		±10%
R5		22kΩ	±10%
R6	Note 2		±10%
C1		22pF	±20%
C2		22pF	±20%

C3	Note 2	100pF	±20%
C4		0.1µF	±20%
C5	Note 3	100pF	±20%
C6		0.1µF	±20%
C7	Note 3, 4		±20%
C8		0.1µF	±20%
X1	Note 1	4.032MHz	±100ppm

Table 1: Recommended External Components

Recommended External Components Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. R2, R6 and C3 form the gain components for the Summing Amplifier. R6 should be chosen as required from the system specification, using the following formula:

   $$\text{Tx Sub Audio Gain} = -\frac{R2}{R6}$$

3. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

   $$\text{Gain} = -\frac{R3}{R4}$$

4. C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

4. General Description

The MX818 is a programmable CTCSS sub-audio encoder/decoder for use in land mobile radio equipment.

The receiver section of the MX818 has a fast/predictive tone detector which operates in parallel with a tone decoder. The latter decodes a user-programmable set of up to 15 tones and performs a more accurate (but slower) analysis of the tones detected by the fast/predictive tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

The high pass audio filter is designed to filter out the CTCSS sub-audio tones. The summing and modulation amplifiers allow the audio modulation to be controlled digitally via the C-BUS. A general purpose timer is included.

Each function, and the routing of signals, is flexible and may be configured or controlled by the user's software.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

				DATA BYTE(S)	
REGISTER NAME	**SECTION**	**HEX ADDRESS COMMAND**	**READ / WRITE**	**BYTE 1**	**BYTE 2**
General Reset	4.1.3.1	$01	W	none	none
Sub-Audio Control	4.1.3.2	$80	W	Refer to Bit Description	none
Sub-Audio Status	4.1.4, 4.1.5.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.1.3.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.1.3.7	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
CTCSS RX Program	4.1.3.8	$84	W	1 of 15 possible Register Select & Decode Frequencies	
General Control	4.1.3.4	$88	W	Refer to Bit Description	none
Audio Control	4.1.3.9	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.1.3.5	$8B	W	Refer to Bit Description	none
IRQ Mask	4.1.3.6	$8E	W	Refer to Bit Description	none
IRQ Flag	4.1.4, 4.1.5.2	$8F	R	Refer to Bit Description	none

Table 2: Command Summary

4.1.2 Address/Commands

Instructions and data are transferred, via C-BUS, in accordance with the timing information provided in Figure 4.

Instruction and data transactions to and from the MX818 consist of an Address/Command (A/C) byte followed by either:

a. further instruction or data (0,1, or 2 bytes)
b. status or Rx data reply (1 byte)

4.1.2.1 8-bit Write Only Registers

HEX ADDRESS COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SUB-AUDIO CONTROL	CTCSS			0	0	0	0	0
		TX ENABLE	DECODE RX ENABLE	FAST DETECT ENABLE					
$82	SUB-AUDIO SET-UP	CTCSS DECODER BANDWIDTH				FAST CTCSS MODE DETECT/ PREDICTIVE	0	0	0
		MSB BIT 3	BIT 2	BIT 1	LSB BIT 0				
$88	GENERAL CONTROL	AUDIO BAND-PASS FILTER			0	0	0	TIMER ENABLE	TIMER RE-CYCLE
		BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD					
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER (GPT)							
		MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GPT IRQ MASK	0	0	CTCSS IRQ MASK	CTCSS FAST IRQ MASK	0	0

Table 3: 8-bit Write Only Register

4.1.2.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX / FAST RX FREQUENCY				
					MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX / FAST RX FREQUENCY							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	CTCSS RX PROGRAM (1)	CTCSS TONE ADDRESS				CTCSS FREQUENCY			
		MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	MSB BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS RX PROGRAM (2)	CTCSS FREQUENCY							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)				MOD 1				
		0	0	MOD 1 ENABLE	MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)				MOD 2				
		0	0	MOD 2 ENABLE	MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Table 4: 16-bit Write Only Registers

4.1.3 Write Only Register Description

4.1.3.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME		HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
SUB-AUDIO CONTROL		$80	0	0	0	0	0	0	0	0
SUB-AUDIO STATUS		$81	0	0	0	0	X	X	X	X
SUB-AUDIO SET-UP		$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY	(1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY	(2)		0	0	0	0	0	0	0	0
CTCSS RX PROGRAM	(1)	$84	0	0	0	0	0	0	0	0
CTCSS RX PROGRAM	(2)		0	0	0	0	0	0	0	0
GENERAL CONTROL		$88	0	0	0	0	0	0	0	0
AUDIO CONTROL	(1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL	(2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER		$8B	0	0	0	0	0	0	0	0
IRQ MASK		$8E	0	0	0	0	0	0	0	0
IRQ FLAG		$8F	0	0	0	0	0	0	0	0

X = undefined

Table 5: General Reset (Hex Address $01)

4.1.3.2 SUB-AUDIO CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

CTCSS TX ENABLE and DECODER ENABLE (Bits 7 and 6)	Bit 7 and Bit 6 enable and disable the CTCSS decoder (Rx) or transmitter (Tx) according to Table 7. See Note 1
CTCSS FAST DETECT ENABLE (Bit 5)	When bit 5 is set to 1, the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SUB-AUDIO SET-UP Register, $82). When this bit is 0, both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled. See Note 2
(Bits 4, 3, 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 6: Sub-Audio Control Register (Hex Address $80)

Tx Bit 7	Rx Bit 6	Function
0	0	Tx disabled, Rx disabled
0	1	Tx disabled, Rx enabled
1	0	Tx enabled, Rx disabled
1	1	Tx enabled, Rx enabled

Table 7: CTCSS Tx Enable and Decoder Enable

Notes:

1. Bit 7 should be set to 0 if CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is set to 1.
2. Bit 5 should be set to 0 if CTCSS TX ENABLE (Bit 7 SUB-AUDIO CONTROL Register, $80) is set to 1.

4.1.3.3 SUB-AUDIO SET-UP Register (Hex address $82)

This register is used to define the CTCSS parameters, as described below:

CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS tone decoder according to Table 9
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is 1, this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to Table 10.
(Bits 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 8: Sub-Audio Set-up Register (Hex Address $82)

				BANDWIDTH	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Will Decode**	**Will Not Decode**
1	0	0	0	±1.1%	±2.4%
1	0	0	1	±1.3%	±2.7%
1	0	1	0	±1.6%	±2.9%
1	0	1	1	±1.8%	±3.2%
1	1	0	0	±2.0%	±3.5%
1	1	0	1	±2.2%	±3.7%
1	1	1	0	±2.5%	±4.0%
1	1	1	1	±2.7%	±4.2%

Table 9: CTCSS Decoder Bandwidth

DETECT/PREDICTIVE Bit 3	FUNCTION
0	DETECT mode
1	PREDICTIVE mode

If the CTCSS FAST DETECT ENABLE bit is 0 then both modes are deselected.

Table 10: Fast CTCSS Mode

4.1.3.4 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below

BPF ENABLE (Bit 7)	When this bit is 1 the audio band-pass filter is enabled. When this bit is 0 the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is 1 the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is 0 the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is 1 a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is 0 the output of the audio band-pass filter is not attenuated.
(Bits 4, 3 and 2)	Reserved for future use. These bits should be set to 0.
TIMER ENABLE (Bit 1)	When this bit goes to a 1 the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is 0 the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is 1 the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is 0 the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from 1 to 0 while the timer is enabled then the timer will complete the present count before stopping.

Table 11: General Control Register (Hex Address $88)

4.1.3.5 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (0.95ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to 1. An interrupt is generated on the $\overline{\text{IRQ}}$ pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is 1 otherwise the GPT IRQ FLAG remains set to 1 and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is 1 then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is 0 then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with 0 will cause the timer circuitry to be disabled (i.e. powersaved).

4.1.3.6 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These bits should be set to 0.
GPT IRQ MASK **(Bit 6)**	When bit 6 is set to 1 it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS IRQ MASK **(Bit 3)**	When bit is set to 1 it enables an interrupt that occurs when CTCSS IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS FAST IRQ MASK **(Bit 2)**	When this bit is set to 1 it enables an interrupt that occurs when CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.

Table 12: IRQ MASK Register (Hex address $8E)

4.1.3.7 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, bits 0 - 12 defines the receive frequency the fast predictive detector is looking for, according to the formula below:

$$A = \frac{f_{XTAL}\ (\text{Hz})}{16 \times f_{TONE}\ (\text{Hz})}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, bits 0 - 12 control the frequency of the transmitted CTCSS tones, according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above: (i.e. Tx tone = predictive tone).

When Bit 7 (in the first 8 bits) is set to 1, the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 - 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT.

4.1.3.8 CTCSS RX PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. Byte 1 and Byte 2 are used to program the center frequencies of up to 15 tones in the sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<------------------- N ------------------->						<------------------- R ------------------->					
0	0	0	1												
0	0	1	0												
0	0	1	1												
0	1	0	0												
0	1	0	1	N is the binary representation of the following decimal number (n): $n = \text{INT}(948982 \times f_{TONE} / f_{XTAL})$						R is the nearest 6-bit binary representation of (r), where: $r = \{[237245/f_{XTAL}] - [n/(4 \times f_{TONE})]\} \times 8400$					
0	1	1	0												
0	1	1	1												
1	0	0	0												
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0												
1	1	0	1												
1	1	1	0												

Table 13: CTCSS RX PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal.

$$n = \text{INT}(948982 \times 100 / 4.032 \times 10^6)$$
$$= \text{INT}(23.536) = 23$$
$$N = 010111 \text{ (binary)}$$

$$r = \{[237245 / 4.032 \times 10^6] - [23 / (4 \times 100)]\} \times 8400$$
$$= 11.26$$
$$R = 11 \text{ (rounding up if exactly halfway)}$$
$$= 001011 \text{ (binary)}$$

This generates the 12-bit code of 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

4.1.3.9 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the six least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

BYTE 1						
5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

BYTE 2						
5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is 1 the MOD1 attenuator is enabled. When this bit is 0 the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is 1 the MOD2 attenuator and the SUMMER AMP are enabled. When this bit is 0 they are both disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to 0

Table 14: AUDIO CONTROL Register (Hex address $8A)

4.1.4 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$81	SUB-AUDIO STATUS	0	CTCSS FAST TONE	0	TONE DECODE	CTCSS RX TONE			
						MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
$8F	IRQ FLAG	0	GP TIMER IRQ FLAG	0	0	CTCSS IRQ FLAG	CTCSS FAST IRQ FLAG	0	0

4.1.5 Read Only Register Description

4.1.5.1 SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

(Bit 7)	Reserved for future use. This will be set to 0 and should be ignored by user's software.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to 1 if a periodic tone is detected. If no periodic tone is detected this bit will be set to 0. When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to 1 if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX Register is detected. If no match is found this bit will be set to 0. When Bit 5 in the SUB-AUDIO CONTROL Register is set to 0 this bit will be a 0.
(Bit 5)	Reserved for future use. This will be set to 0 and should be ignored by the user's software.
TONE DECODE (Bits 4)	This bit indicates the status of the tone decoder. A 1 indicates a tone has been detected (TONE DECODE). A 0 indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SUB-AUDIO SET-UP Register bits 7, 6, 5 and 4) and the CTCSS RX TONE number (See SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SUB-AUDIO CONTROL Register is set to 0 the TONE DECODE bit 4 will be set to 0. Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of 1111 in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone will cause the NOTONE timer to be started. If loss of tone continues for the duration of the time-out period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
CTCSS RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the CTCSS tone decoded according to the tones programmed in the CTCSS RX PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SUB-AUDIO SET-UP Register, $82) and CTCSS FREQUENCY (Bits 11 - 0, CTCSS RX PROGRAM Register, $84).

Table 15: SUB-AUDIO STATUS Register (Hex address $81)

4.1.5.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as indicated below.

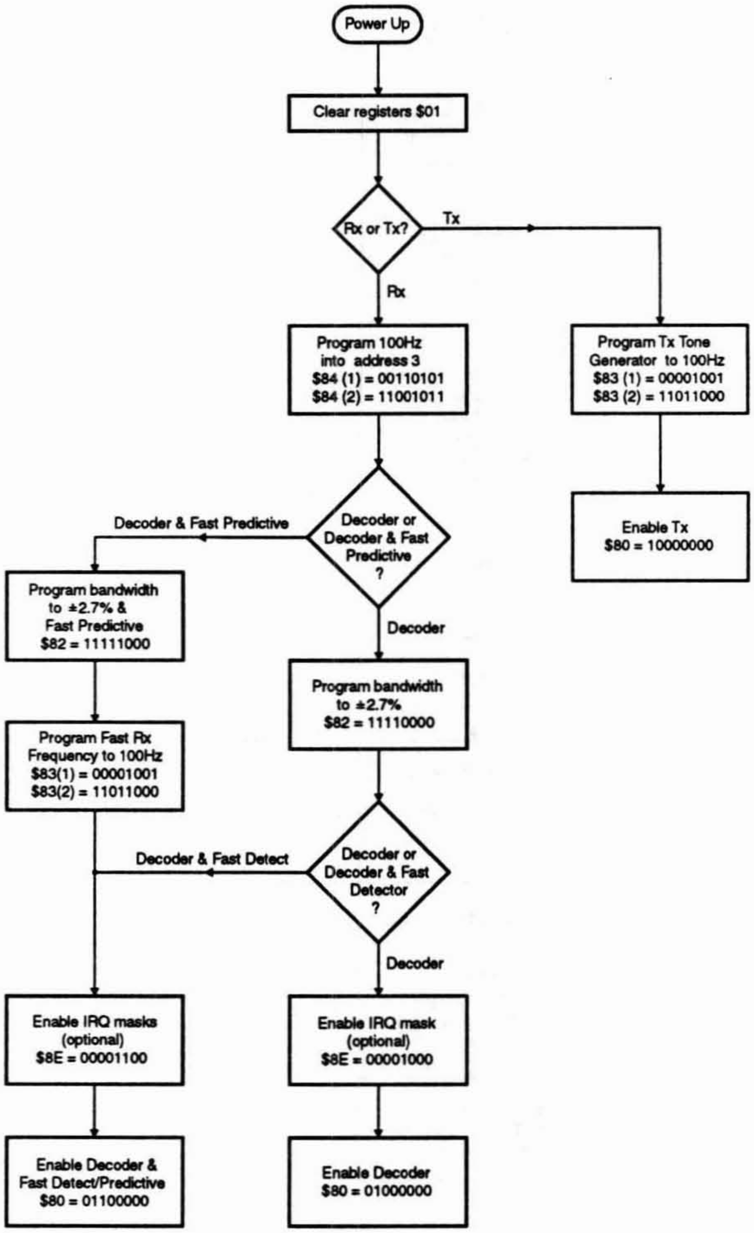
(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These will be set to 0 and should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to 1 to indicate the timeout has expired. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS IRQ FLAG (Bit 3)	When CTCSS RX DECODE (Bit 4, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).

Table 16: IRQ FLAG Register (Hex address $8F)

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

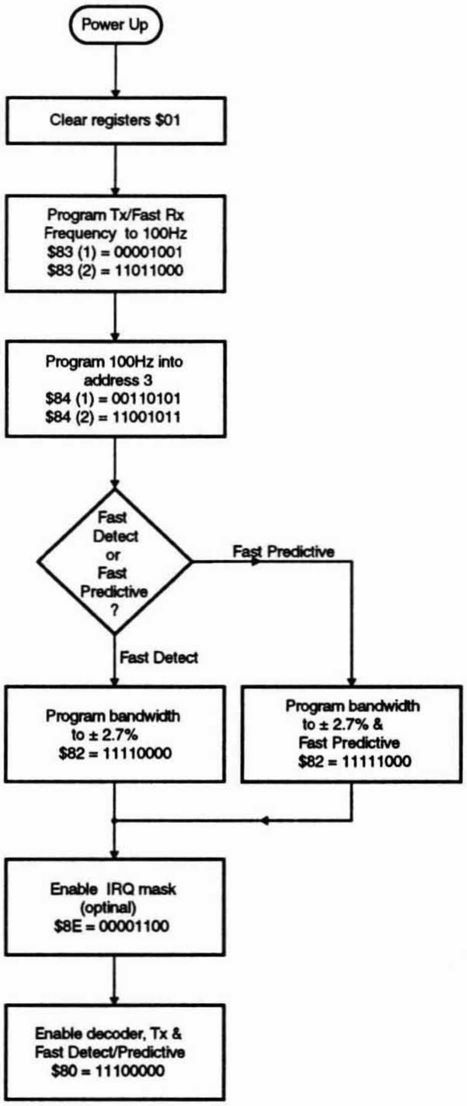
Note: $8X is the Hex address/command.


Power Up
Clear registers $01
Rx or Tx?
Tx
Rx
Program 100Hz into address 3
$84 (1) = 00110101
$84 (2) = 11001011
Program Tx Tone Generator to 100Hz
$83 (1) = 00001001
$83 (2) = 11011000
Enable Tx
$80 = 10000000
Decoder & Fast Predictive
Decoder or Decoder & Fast Predictive ?
Decoder
Program bandwidth to ±2.7% & Fast Predictive
$82 = 11111000
Program bandwidth to ±2.7%
$82 = 11110000
Program Fast Rx Frequency to 100Hz
$83(1) = 00001001
$83(2) = 11011000
Decoder & Fast Detect
Decoder or Decoder & Fast Detector ?
Decoder
Enable IRQ masks (optional)
$8E = 00001100
Enable IRQ mask (optional)
$8E = 00001000
Enable Decoder & Fast Detect/Predictive
$80 = 01100000
Enable Decoder
$80 = 01000000

The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.


Power Up
Clear registers $01
Program Tx/Fast Rx Frequency to 100Hz
$83 (1) = 00001001
$83 (2) = 11011000
Program 100Hz into address 3
$84 (1) = 00110101
$84 (2) = 11001011
Fast Detect or Fast Predictive ?
Fast Predictive
Fast Detect
Program bandwidth to ± 2.7%
$82 = 11110000
Program bandwidth to ± 2.7% & Fast Predictive
$82 = 11111000
Enable IRQ mask (optinal)
$8E = 00001100
Enable decoder, Tx & Fast Detect/Predictive
$80 = 11100000

5. Application

5.1 General

The MX818 is intended for use in radio systems where sub-audio signaling is required for functions such as trunking control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permits certainty and signal to noise performance to be traded when congestion or range, limits the system performance.

5.2 Transmitter

The transmitter is enabled with Bit 7 in the SUB-AUDIO CONTROL register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to 1 the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 to 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT (Bits 7 and 5 in the SUB-AUDIO CONTROL register $80).

5.3 Receiver (Decode)

The CTCSS Receiver (Decoder) should first be set up according to the desired characteristics. This entails setting the CTCSS decoder bandwidth in the SUB-AUDIO SET-UP register ($82), also programming the center frequencies of the desired tones in the CTCSS RX PROGRAM register ($84). (It can hold up to 15 different tones). Any tone can be in any location. During operation when the device is receiving, the tones are scanned in the sequence of their location, i.e. $0 first and $E last and once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The CTCSS IRQ MASK in the IRQ MASK register ($8E) should also be set as required.

The CTCSS DECODER ENABLE in the SUB-AUDIO CONTROL register ($80) should then be set to 1. While in the Decode mode the FAST DETECT may be enabled (see below).

When the receiver detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SUB-AUDIO STATUS register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (Fast Detect)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SUB-AUDIO CONTROL register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SUB-AUDIO SET UP register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG register ($8F), and the CTCSS FAST TONE Bit 6 in the SUB-AUDIO STATUS register ($81).

5.5 General Purpose Timer (GPT)

This may be used in conjunction with the Rx Decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value register GENERAL PURPOSE TIMER register ($8B) set in units of 1.0ms, an IRQ FLAG Bit 6 of the IRQ FLAG register ($8F) and an IRQ MASK Bit 6 IRQ MASK register ($8E).

5.6 Tx / Fast Rx Tone Table

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 17: Tx / Fast Rx Tone Table

5.7 Rx Program Tone Table

The following table lists the commonly used CTCSS tones together with the values for programming the "CTCSS RX PROGRAM" register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 18: Rx Program Tone Table

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

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6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308mVrms at 1kHz
V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C, T_{OP} = -45°C to 85°C.
Composite Signal = 308mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Note	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
All Powersaved						
V_{DD} = 5.0V		1, 2		0.6	1.0	mA
V_{DD} = 3.3V		2		0.35	0.6	mA
Tx/Rx Operating						
V_{DD} = 5.0V		1, 2		3.5	6.0	mA
V_{DD} = 3.3V		2		1.6	2.5	mA
C-BUS Interface						
Input Logic 1			70%			V_{DD}
Input Logic 0					30%	V_{DD}
Input Leakage Current (Logic 1 or 0)			-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic 1 (I_{OH} = 120µA)			90%			V_{DD}
Output Logic 0 (I_{OL} = 360µA)					10%	V_{DD}
Off State Leakage Current (V_{OUT} = V_{DD})		6			10	µA
AC Parameters						
CTCSS Decoder						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			140		ms
De-Response Time	(Composite Signal)			145		ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Detect						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			56.0		ms
Frequncy Range			60		253	Hz
CTCSS Detector - Fast Predictive						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)	7		37.0		ms
Frequemcy Range			60		253	Hz
Decode Bandwidth				40		Hz
CTCSS Encoder						
Frequency Range			60		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	1.0	dB
Total Harmonic Distortion		9		2.0		%

Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain	(at 1.0kHz)	8		0		dB
Passband Ripple	(wrt gain at 1.0kHz)	8	-2		0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz
Output Impedance						
TX SUB-AUDIO OUT	(Enabled)			2.0		kΩ
RX AUDIO OUT	(Disabled)			500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	(input = 1mV at 100Hz)			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	(at 100Hz)		10			MΩ
Output Impedance	(Open Loop)			6.0		kΩ
Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	(at 100Hz)			15.0		kΩ
Mod.2 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-0.6		0.6	dB
Output Impedance		3		600		Ω
General Purpose Timer						
Timing Period Range			1.0		242	ms
Count Interval				0.95		ms
Xtal/Clock Input						
Pulse Width ('High' or 'Low')		4	40.0			ns
Input Impedance (at 100Hz)			10.0			MΩ
Gain (input = 1mV$_{RMS}$ at 100Hz)			20.0			dB

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{\text{IRQ}}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD1 or MOD2 output.

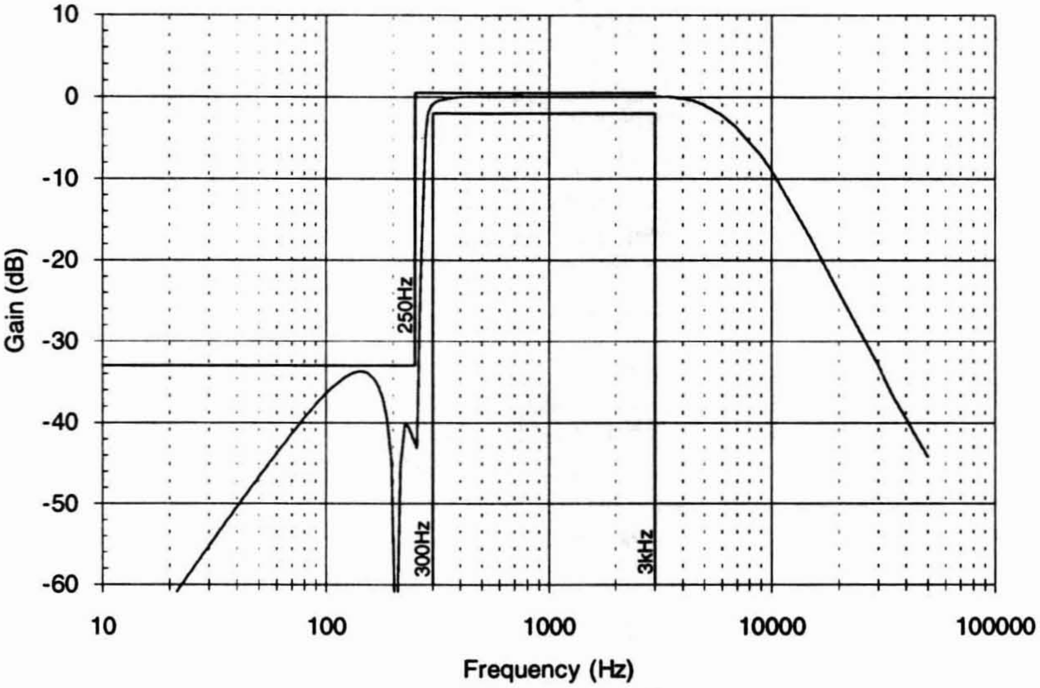


Figure 3: Audio Band-Pass Filter Frequency Response

6.1.4 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

Parameter		Min.	Typ.	Max.	Units
t_{CSE}	CS-Enable to Clock-High	2.0			μs
t_{CSH}	Last Clock-High to CS-High	4.0			μs
t_{HIZ}	CS-High to Reply Output 3-state			2.0	μs
t_{CSOFF}	CS-High Time between transactions	2.0			μs
t_{NXT}	Inter-Byte Time	4.0			μs
t_{CK}	Clock-Cycle time	2.0			μs

Timing Diagrams Notes

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing μC serial interface formats C-BUS compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

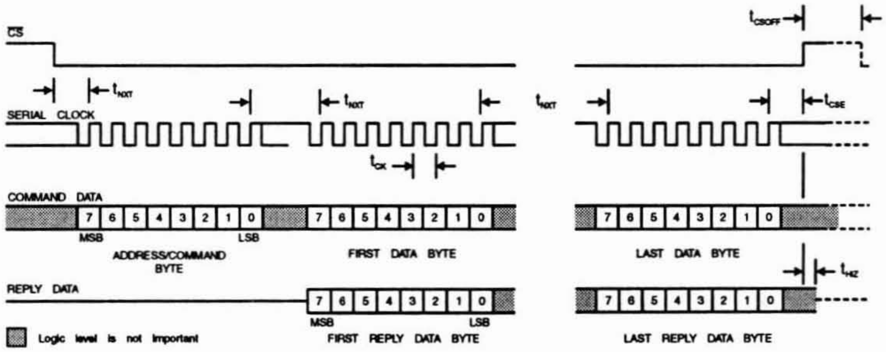
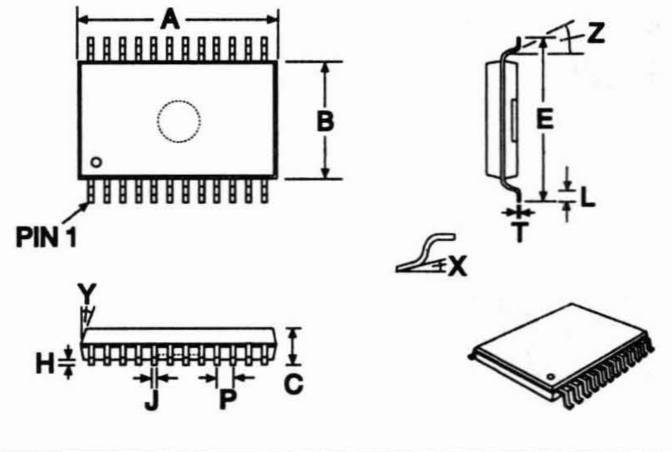

$\overline{CS}$
t_{CSOFF}
SERIAL CLOCK
t_{NXT}
t_{NXT}
t_{NXT}
t_{CSE}
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
Logic level is not important

Figure 4: C-BUS Timing

6.2 Packaging

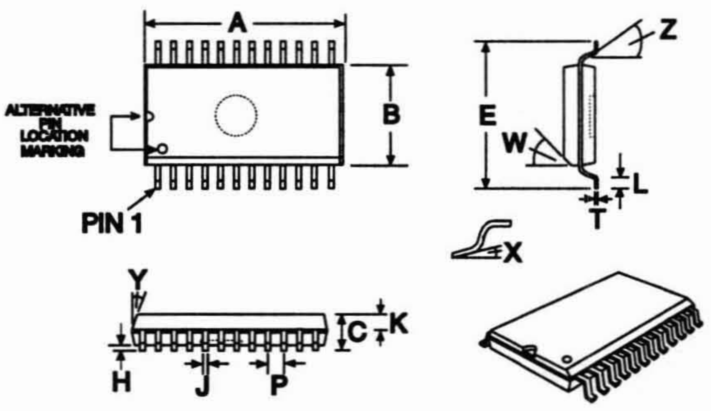


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin SSOP Mechanical Outline: ***Order as part no. MX818DS***

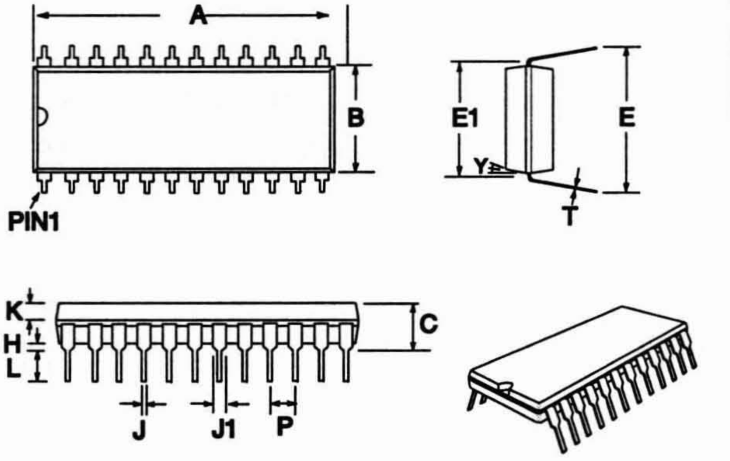


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SOIC Mechanical Outline: ***Order as part no. MX818DW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin PDIP Mechanical Outline: ***Order as part no. MX818P***

MX•COM, INC. MiXed Signal ICs
DATA BULLETIN

MX828 CTCSS/DCS/SelCall Processor

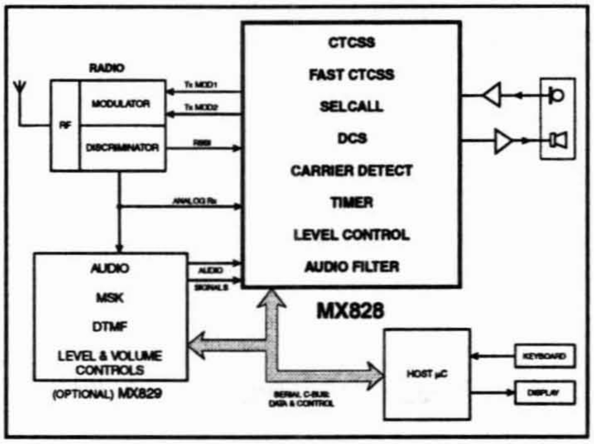
PRELIMINARY INFORMATION

Features

- Fast CTCSS Detection
- Full Duplex CTCSS and SelCall
- Full 23/24 Bit DCS Codec
- SelCall Codec
- Non Predictive Tone Detection
- Low Power 3.3V/5.0V Operation
- Variable Gain Audio Filter
- Programmable:
  - Tone Decoder
  - Tone Encoder
  - Modulator Drivers
  - Comparator for RSSI
- Pin compatible with reduced function MX818
- Full control via 4-Wire Serial Interface

Applications

- Radio Systems Requiring Sub-Audible Signaling
  - Trunking Control
  - Selective Calling
  - Group Calling
- Increased Efficiency
  - Scanning Systems
  - Trunking Systems


RADIO
RF
MODULATOR
DISCRIMINATOR
Tx MOD1
Tx MOD2
RSSI
ANALOG Rx
CTCSS
FAST CTCSS
SELCALL
DCS
CARRIER DETECT
TIMER
LEVEL CONTROL
AUDIO FILTER
MX828
AUDIO
MSK
DTMF
LEVEL & VOLUME CONTROLS
(OPTIONAL) MX829
AUDIO SIGNALS
SERIAL C-BUS: DATA & CONTROL
HOST µC
KEYBOARD
DISPLAY

The MX828 is a low power SelCall, CTCSS, and DCS signal processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling, and Group Calling applications. The MX828 is full duplex and offers many advanced features to assist in the design of new Sub-Audible and in-band based systems. These include: a programmable tone decoder which may be set to respond to between 1 and 15 CTCSS or SelCall tones with minimum software intervention, a Fast/Predictive CTCSS detector that can respond to a single programmed tone in less than 60ms or provide an output if CTCSS tone is present at the detector input, two high resolution tone encoders that accurately generate CTCSS or SelCall tones, and a full 23/24 bit DCS encoder and decoder. The MX828 also provides a general purpose timer, a comparator with a programmable threshold, and a summing amplifier with two adjustable gain blocks to facilitate design integration and reduce part count.

The MX828 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP (MX828DS), 24-pin SOIC (MX828DW), and 24-pin PDIP (MX828P).

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

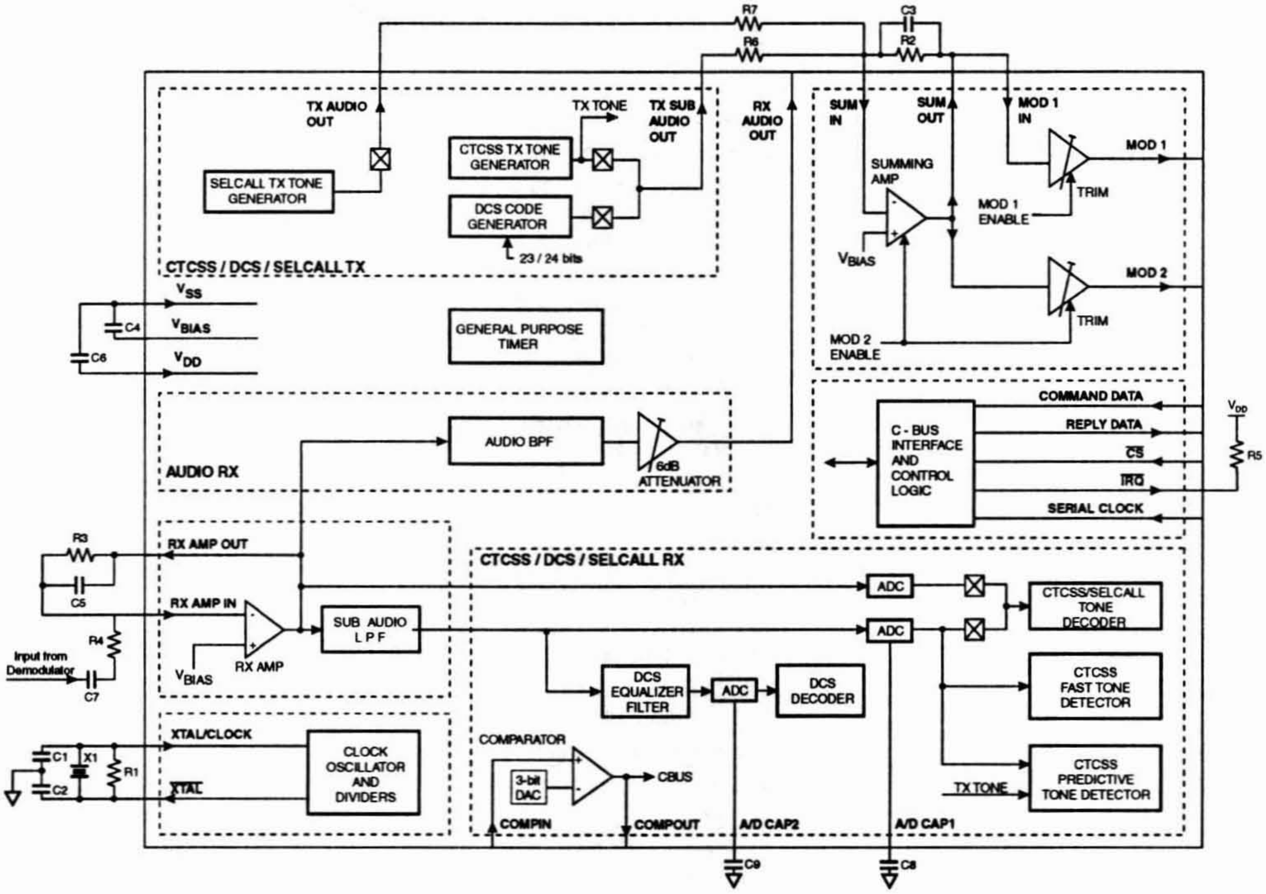

R7
C3
R6
R2
TX AUDIO OUT
TX TONE
TX SUB AUDIO OUT
RX AUDIO OUT
SUM IN
SUM OUT
MOD 1 IN
MOD 1
SELCALL TX TONE GENERATOR
CTCSS TX TONE GENERATOR
DCS CODE GENERATOR
23 / 24 bits
CTCSS / DCS / SELCALL TX
SUMMING AMP
MOD 1 ENABLE
TRIM
V_{BIAS}
MOD 2
TRIM
MOD 2 ENABLE
V_{SS}
C4
V_{BIAS}
C6
V_{DD}
GENERAL PURPOSE TIMER
COMMAND DATA
V_{DD}
REPLY DATA
R5
C - BUS INTERFACE AND CONTROL LOGIC
$\overline{CS}$
$\overline{IRQ}$
SERIAL CLOCK
AUDIO BPF
6dB ATTENUATOR
AUDIO RX
R3
RX AMP OUT
C5
RX AMP IN
R4
Input from Demodulator
C7
V_{BIAS}
RX AMP
SUB AUDIO LPF
CTCSS / DCS / SELCALL RX
ADC
ADC
CTCSS/SELCALL TONE DECODER
DCS EQUALIZER FILTER
ADC
DCS DECODER
CTCSS FAST TONE DETECTOR
XTAL/CLOCK
C1
X1
R1
C2
$\overline{XTAL}$
CLOCK OSCILLATOR AND DIVIDERS
COMPARATOR
3-bit DAC
CBUS
TX TONE
CTCSS PREDICTIVE TONE DETECTOR
COMPIN
COMPOUT
A/D CAP2
A/D CAP1
C9
C8

Figure 1: Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The "C-BUS" serial clock input. This clock, produced by the µC, is used for timing transfer of commands and data to and from the device. (Figure 4).
4	COMMAND DATA	input	The "C-BUS" serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. (Figure 4).
5	REPLY DATA	output	The "C-BUS" serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This 3-state output is held at high impedance when not sending data to the µC. (Figure 4).
6	$\overline{\text{CS}}$	input	The "C-BUS" data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal (Figure 4).
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	COMPOUT	output	The output of the comparator.
9	COMPIN	input	The input to the comparator.
10	A/D CAP 1	output	An internal reference voltage for the CTCSS A/D. Bypassed to V_{SS} with an external capacitor.
11	A/D CAP 2	output	An internal reference voltage for the DCS A/D. Bypassed to V_{SS} with an external capacitor.
12	V_{SS}	Power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	Output of the Rx input amplifier
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	TX AUDIO OUT	output	Output of the SelCall tone generator.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier.
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS or DCS Tx tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

Table 1: Signal List

3. External Components

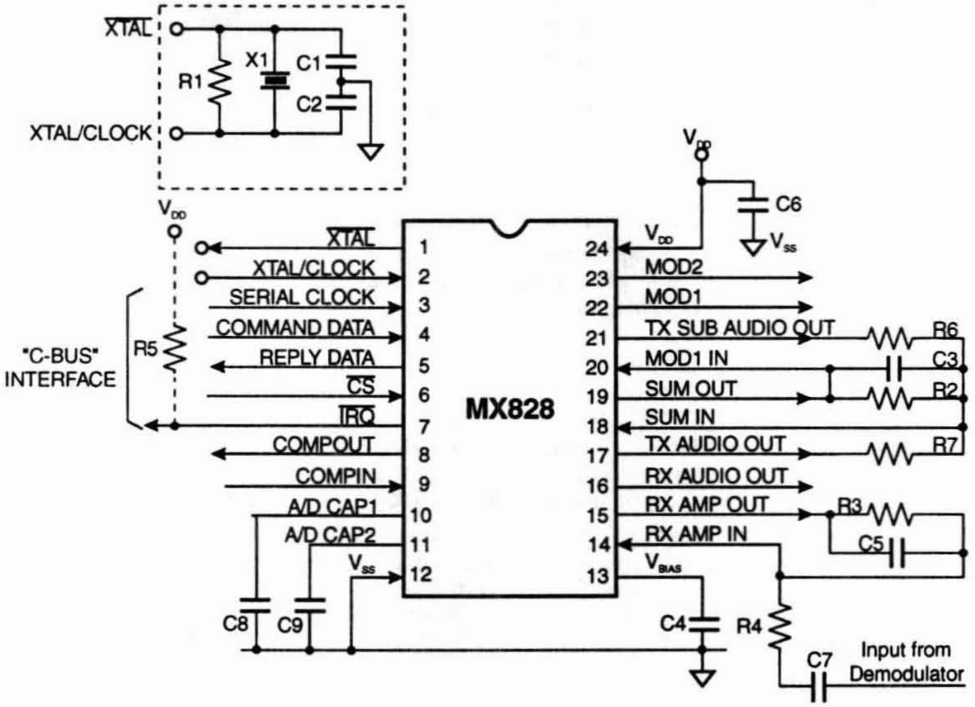

XTAL
R1
X1
C1
C2
XTAL/CLOCK
VDD
C6
VSS
VDD
XTAL
XTAL/CLOCK
SERIAL CLOCK
COMMAND DATA
REPLY DATA
CS
IRQ
COMPOUT
COMPIN
A/D CAP1
A/D CAP2
VSS
"C-BUS"
INTERFACE
R5
MX828
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
MOD2
MOD1
TX SUB AUDIO OUT
MOD1 IN
SUM OUT
SUM IN
TX AUDIO OUT
RX AUDIO OUT
RX AMP OUT
RX AMP IN
VBIAS
R6
C3
R2
R7
R3
C5
C8
C9
C4
R4
C7
Input from
Demodulator

Figure 2: Recommended External Components

R1		1MΩ	±5%
R2		100kΩ	±10%
R3		100kΩ	±10%
R4	Note 2		±10%
R5		22kΩ	±10%
R6	Note 1		±10%
R7	Note 1		±10%
C1		22pF	±20%
C2		22pF	±20%

C3		100pF	±20%
C4		0.1µF	±20%
C5		100pF	±20%
C6		0.1µF	±20%
C7	Note 2		±20%
C8		0.1µF	±20%
C9		1.0µF to 3.3µF	±20%
X1	Note 3	4.032MHz	±100ppm

Table 2: External Components

External Components Notes:

1. R2, R6, R7 and C3 form the gain components for the Summing Amplifier. R6 and R7 should be chosen as required from the system specification, using the following formula:

   Tx Sub Audio Gain $= -\frac{R2}{R6}$ Tx Audio Gain $= -\frac{R2}{R7}$

2. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

   Gain $= -\frac{R3}{R4}$

   C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX828 is a signaling encoder/decoder for use in land mobile radio equipment, see Figure 1. The transmitter section of the MX828 has independently controllable tone generators for sub-audio (CTCSS) and inband (SelCall) signaling. Also featured is a DCS code generator, which may be used in place of the CTCSS tone generator.

The receiver section of the MX828 has a fast/predictive CTCSS tone detector which operates in parallel with a DCS decoder and a CTCSS/SelCall tone decoder. The latter is switchable to perform either CTCSS or SelCall tone decoding of a user-programmable set of up to 15 tones. In the CTCSS mode it performs a more accurate (but slower) analysis of the tones detected by the fast/predictive CTCSS tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

Both the DCS transmit and receive bit rates are fixed at 134.4bps.

Other functions on the MX828 are a comparator with programmable threshold level, a general purpose timer and a summing amplifier with two adjustable gain blocks, which may be used for two point modulation, for example. All MX828 functions are controlled by an external µC over the "C-BUS" interface, a serial interface designed to reduce interference levels in radio equipment.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

REGISTER NAME	SECTION	HEX ADDRESS COMMAND	READ / WRITE	DATA BYTE(S)	
				BYTE 1	BYTE 2
General Reset	4.4.1	$01	W	none	none
Sub-Audio Control	4.4.2	$80	W	Refer to Bit Description	none
SelCall Sub-Audio Status	4.5 4.6.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.4.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.4.10	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
RX Tone Program	4.4.11	$84	W	1 of 15 possible Registers Select & Decode Frequencies	
DCS Code	4.4.4	$85	W	Byte 3 of 3	none
DCS Code	4.4.5	$86	W	Byte 2 of 3	none
DCS Code	4.4.6	$87	W	Byte 1 of 3	none
General Control	4.4.7	$88	W	Refer to Bit Description	none
Audio Control	4.4.12	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.4.8	$8B	W	Refer to Bit Description	none
SelCall TX	4.4.13 4.4.2 4.4.3	$8D	W	Specify TX SelCall Frequencies	
IRQ Mask	4.4.9	$8E	W	Refer to Bit Description	none
IRQ Flag	4.5 4.6.2	$8F	R	Refer to Bit Description	none

Table 3: Command Summary

4.1.2 Address/Commands

Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the MX828 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or

(ii) a status or Rx data reply (1 byte)

4.2 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SIGNALLING CONTROL	SUBAUDIO TX ENABLE	TONE DECODER ENABLE	FAST DETECT ENABLE	0	0	SELCALL TX ENABLE	0	DCS RX ENABLE
$82	SIGNALLING SET-UP	TONE DECODER BANDWIDTH				FAST CTCSS MODE DETECT/ PREDICTIVE	TONE DECODER MODE	SUBAUDIO TX MODE	DCS 23/24
		MSB BIT 3	BIT 2	BIT 1	LSB BIT 0				
$85	DCS BYTE 3	DCS BYTE 3							
		OPTIONAL MSB BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
$86	DCS BYTE 2	DCS BYTE 2							
		BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$87	DCS BYTE 1	DCS BYTE 1							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$88	GENERAL CONTROL	BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD	MSB DAC BIT 2	DAC BIT 1	LSB DAC BIT 0	GP TIMER ENABLE	GP TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER							
		MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GP TIMER IRQ MASK	COMP 0 to 1 IRQ MASK	COMP 1 to 0 IRQ MASK	TONE IRQ MASK	CTCSS FAST IRQ MASK	0	DCS IRQ MASK
$9C	*Reserved for later use*								

Table 4: 8-bit Write Only Registers

4.3 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX/FAST RX FREQUENCY				
					MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX/FAST RX FREQUENCY							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	RX TONE PROGRAM (1)	TONE ADDRESS				TONE FREQUENCY			
		MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	MSB BIT 11	BIT 10	BIT 9	BIT 8
	RX TONE PROGRAM (2)	TONE FREQUENCY							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)	0	0	MOD 1 ENABLE	MOD 1				
					MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)	0	0	MOD 2 ENABLE	MOD 2				
					MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8D	SELCALL TX (1)	SELCALL NOTONE	0	0	SELCALL TX TONE				
					MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	SELCALL TX (2)	SELCALL TX TONE							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Table 5: 16-bit Write Only Registers

4.4 Write Only Register Description

4.4.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
SIGNALING CONTROL	$80	0	0	0	0	0	0	0	0
SELCALL & SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SIGNALING SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (2)		0	0	0	0	0	0	0	0
RX TONE PROGRAM (1)	$84	0	0	0	0	0	0	0	0
RX TONE PROGRAM (2)		0	0	0	0	0	0	0	0
DCS BYTE 3	$85	0	0	0	0	0	0	0	0
DCS BYTE 2	$86	0	0	0	0	0	0	0	0
DCS BYTE 1	$87	0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
SELCALL TX (1)	$8D	0	0	0	0	0	0	0	0
SELCALL TX (2)		0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

Table 6: GENERAL RESET (Hex address $01)

4.4.2 SIGNALING CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

SUBAUDIO TX ENABLE (Bit 7)	Bit 7 should be set to "1" to enable the CTCSS/DCS subaudio transmitter. The subaudio Tx type will depend on the state of the SUBAUDIO TX MODE (Bit 1 SIGNALING SET-UP Register $82).
TONE DECODER ENABLE (Bit 6)	Bit 6 should be set to "1" to enable the CTCSS/SelCall tone decoder or the DCS decoder. Note: See Bit 0 for DCS decoder operation. Bits 7 and 6 should not both be set to "1" when Bit 0 is set to "1" because the DCS function is half-duplex only.
CTCSS FAST DETECT ENABLE (Bit 5)	When this bit is "1", the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SIGNALING SET-UP Register, $82). When this bit is "0", both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled.
SELCALL TX ENABLE (Bit 2)	When this bit is "1" the SelCall transmitter is enabled. When this bit is "0" the SelCall transmitter is disabled and powersaved.

DCS RX ENABLE **(Bit 0)**	When this bit is "1", the DCS decoder is enabled. When this bit is "0" the DCS decoder is disabled. The DCS decoder and the subaudio (CTCSS or DCS) transmitter should not be enabled at the same time.
(Bits 4, 3, and 1)	Reserved for future use. These bits should be set to "0".

Table 7: SIGNALING CONTROL Register (Hex address $80)

4.4.3 SIGNALING SET-UP Register (Hex address $82)

This register is used to define the signaling parameters, as described below:

TONE DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS/SelCall tone decoder according to the table below:
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SIGNALING CONTROL Register, $80) is "1", this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to the table below: If the CTCSS FAST DETECT ENABLE bit is "0" then both modes are deselected.
TONE DECODER MODE (Bit 2)	When this bit is "1" the CTCSS/SelCall tone decoder is set to detect inband (SelCall) tones. When this bit is "0" the tone decoder is set to detect subaudio (CTCSS) tones.
SUBAUDIO TX MODE (Bit 1)	When this bit is "1" the subaudio transmitter will be set to transmit DCS signals, if enabled. When this bit is "0" the subaudio transmitter will be set to transmit CTCSS signals, if enabled.
DCS 23/24 (Bit 0)	When this bit is "1" the DCS transmitter and decoder are configured for a 23-bit code. When this bit is "0" they are configured for a 24-bit code.

Table 8: SIGNALING SET-UP Register (Hex address $82)

					BANDWIDTH	
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Will Decode**	**Will Not Decode**
Recommended for CTCSS	1	0	0	0	±1.1%	±2.4%
Recommended for CCIR	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%
	1	1	0	0	±2.0%	±3.5%
	1	1	0	1	±2.2%	±3.7%
Recommended for ZVEI	1	1	1	0	±2.5%	±4.0%
	1	1	1	1	±2.7%	±4.2%

Table 9: TONE DECODER BANDWIDTH

DETECT/PREDICTIVE Bit 3	**Function**
0	DETECT mode
1	PREDICTIVE mode

Table 10: FAST CTCSS MODE

4.4.4 DCS BYTE 3 Register (Hex address $85)

4.4.5 DCS BYTE 2 Register (Hex address $86)

4.4.6 DCS BYTE 1 Register (Hex address $87)

These three bytes set the code that is transmitted or received in the DCS mode. The LSB bit "0" of the DCS BYTE 1 is transmitted first and the last bit is the MSB bit 23 of DCS BYTE 3 in the 24-bit mode or bit 22 in the 23-bit mode. See Table 22 or refer to the latest version of ANSI/TIA/EIA - 603 specification and programming documentation for DCS standard 23-bit codes.

4.4.7 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below:

BPF ENABLE (Bit 7)	When this bit is "1" the audio band-pass filter is enabled. When this bit is "0" the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is "1" the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is "0" the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is "1" a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is "0" the output of the audio band-pass filter is not attenuated.
DAC (Bits 4, 3 and 2)	These three bits set the level of the digital to analogue converter that feeds the negative input of the comparator. The DAC can be set to one of eight levels equally spaced between V_{SS} and V_{BIAS}, not including V_{SS}, but including V_{BIAS}, i.e. with a 5V supply, the lowest level would be 312.5mV set by "000" in bits 2, 3 and 4 and the highest level would be 2.5V set by "111" in bits 2, 3 and 4.
TIMER ENABLE (Bit 1)	When this bit goes to a "1" the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is "0" the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is "1" the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is "0" the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from "1" to "0" while the timer is enabled then the timer will complete the present count before stopping.

Table 11: GENERAL CONTROL Register (Hex address $88)

4.4.8 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (1ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to "1". An interrupt is generated on the $\overline{\text{IRQ}}$ pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is "1" otherwise the GPT IRQ FLAG remains set to "1" and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is "1" then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is "0" then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with "0" will cause the timer circuitry to be disabled (i.e. powersaved).

4.4.9 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7 and 1)	Reserved for future use. These should be set to "0".
GPT IRQ MASK (Bit 6)	When this bit is set to "1" it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 5)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "0" to "1". When this bit is set to "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 4)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "1" to "0". When this bit is set to "0" the interrupt is masked.
TONE IRQ MASK (Bit 3)	When this bit is set to "1" it enables an interrupt that occurs when the TONE IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to "1" it enables an interrupt that occurs when the CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
DCS IRQ MASK (Bit 0)	When this bit is set to "1" it enables an interrupt that occurs when the DCS DECODE/NO DECODE FLAG (Bit 7, SELCALL & SUB-AUDIO STATUS Register $81) changes state. When this bit is set to "0" the interrupt is masked.

Table 12: IRQ MASK Register (Hex address $8E)

4.4.10 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, the bits 0 to 12 define the receive frequency which the fast predictive detector is looking for according to the formula below:

$$A = \frac{f_{XTAL}\,(\text{Hz})}{16 \times f_{TONE}\,(\text{Hz})}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, the bits 0 to 12 control the frequency of the transmitted CTCSS tones according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above. (i.e. Tx Tone = predictive tone).

When Bit 7 in byte (1) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT.

4.4.11 RX TONE PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. The two bytes are used to program the center frequencies of up to 15 tones in either the audio or sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<----------------------- N ----------------------->						<----------------------- R ----------------------->					
0	0	0	1												
0	0	1	0	N is the binary representation of the						R is the nearest 6-bit binary					
0	0	1	1	following decimal number (n):						representation of (r), where:					
0	1	0	0												
0	1	0	1												
0	1	1	0												
0	1	1	1	SUBAUDIO (CTCSS)						SUBAUDIO (CTCSS)					
1	0	0	0	n = INT (948982 x f_{TONE} / f_{XTAL})						r = ((237245/f_{XTAL}) - (n/(4 x f_{TONE}))) x 8400					
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0	INBAND (SELCALL)						INBAND (SELCALL)					
1	1	0	1	n = INT (83036 x f_{TONE} / f_{XTAL})						r = ((20759/f_{XTAL}) - (n/(4 x f_{TONE}))) x 96000					
1	1	1	0												

Table 13: RX TONE PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal in SUBAUDIO (CTCSS) mode.

n = INT (948982 x 100 / 4.032 x 10^6)
= INT (23.536) = 23
N = 010111 (binary)
r = ((237245 / 4.032 x 10^6) - (23 / (4 x 100))) x 8400
= 11.26
R = 11 (rounding up if exactly halfway)
= 001011 (binary)

Thus the 12-bit code is 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SELCALL and SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

4.4.12 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and bits 0 - 5 of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to Table 14.

BYTE 1								BYTE 2						
5	4	3	2	1	0	Mod. 1 Attenuation		5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})		0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB		1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB		1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	11.6dB		1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	11.2dB		1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	10.8dB		1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	10.4dB		1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	10.0dB		1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	9.6dB		1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	9.2dB		1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	8.8dB		1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	8.4dB		1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	8.0dB		1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	7.6dB		1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	7.2dB		1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	6.8dB		1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	6.4dB		1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	6.0dB		1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	5.6dB		1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	5.2dB		1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	4.8dB		1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	4.4dB		1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	4.0dB		1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	3.6dB		1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	3.2dB		1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	2.8dB		1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	2.4dB		1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	2.0dB		1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	1.6dB		1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	1.2dB		1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.8dB		1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.4dB		1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB		1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is "1" the MOD2 attenuator and the SUMMING AMP are enabled. When this bit is "0" they are both disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to "0".

Table 14: AUDIO CONTROL Register (Hex address $8A)

4.4.13 SELCALL TX Register (Hex address $8D)

This is a 16-bit register. Byte (1) is sent first.

When the SELCALL transmitter is enabled, bits 0 to 12 control the frequency of the transmitted SELCALL tones according to the formula below:

$$A = \frac{f_{XTAL}\ (\text{Hz})}{4 \times f_{TONE}\ (\text{Hz})}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming bits 0 through 12 to "0" places the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL Tx.

4.5 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$81	SELCALL & SUB-AUDIO STATUS	DCS DECODE/ NO DECODE	CTCSS FAST TONE	0	TONE DECODE	RX TONE			
						MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
$8F	IRQ FLAG	0	GP TIMER IRQ FLAG	COMP 0 to 1 IRQ FLAG	COMP 1 to 0 IRQ FLAG	TONE IRQ FLAG	CTCSS FAST IRQ FLAG	0	DCS IRQ FLAG

Table 15: 8-bit Read Only Registers

4.6 Read Only Register Description

4.6.1 SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

DCS DECODE/ NO DECODE (Bit 7)	When the DCS decoder is enabled this bit is continuously updated with the result. A "1" indicates a successful decode (with 3 or less errors). A "0" indicates a failure to decode.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SIGNALING CONTROL Register and Bit 3 in the SIGNALING SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to "1" if a periodic tone is detected. If no periodic tone is detected this bit will be "0".
	When bits 5 and 3 are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to "1" if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX FREQUENCY Register is detected. If no match is found this bit will be "0". When Bit 5 in the SIGNALING CONTROL Register is set to "0" this bit will be "0".
(Bit 5)	Reserved for future use. This will be set to "0" but should be ignored by the user's software.

TONE DECODE (Bit 4)	This bit indicates the status of the tone decoder. A "1" indicates a tone has been detected (TONE DECODE) and a "0" indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SIGNALING SET-UP Register bits 7, 6, 5 and 4) and the RX TONE number (See SELCALL and SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SIGNALING CONTROL Register is set to "0" the TONE DECODE bit 4 will be set to "0". Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of "1111" in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone, will cause the NOTONE timer to be started. If loss of tone continues for the duration of the timeout period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the tone decoded according to the tones programmed in the RX TONE PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SIGNALING SET-UP Register, $82) and FREQUENCY (Bits 11 - 0, RX TONE PROGRAM Register, $84).

Table 16: SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

4.6.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as below:

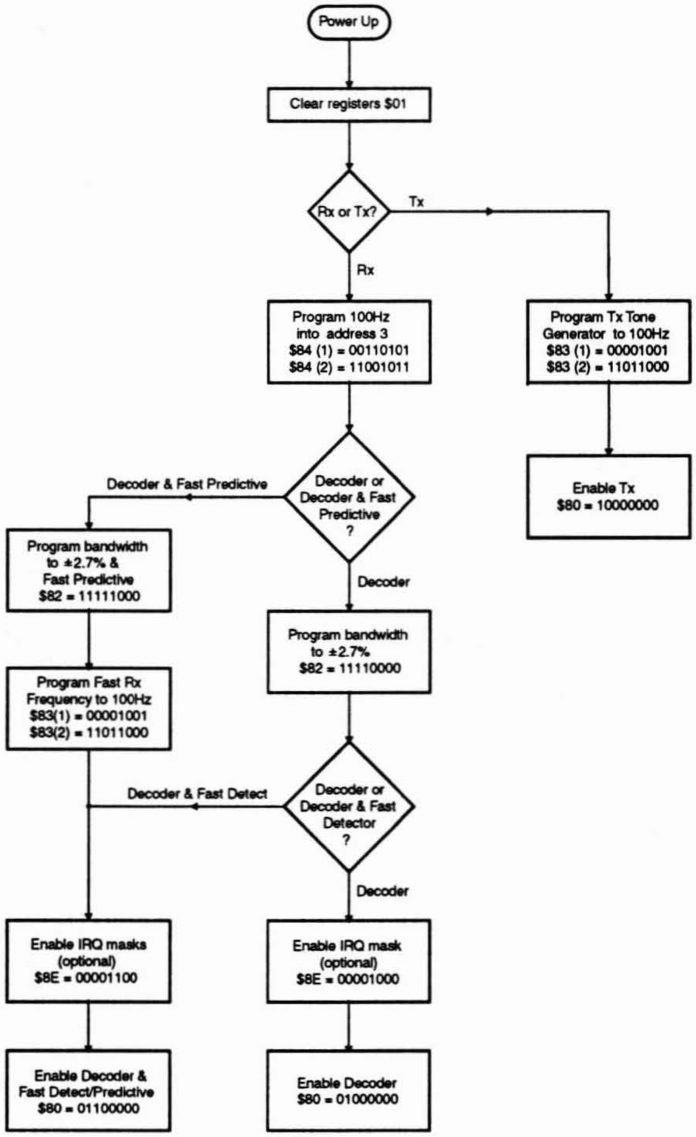
(Bits 7 and 1)	Reserved for future use. These will be set to "0" but should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to "1" to indicate the timeout has expired. This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
COMP 0 to 1 IRQ FLAG (Bit 5)	When the comparator output goes from "0" to "1" (i.e. when the input voltage is above the DAC output voltage) this bit will be set to "1" and an interrupt generated (if bit 5 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
COMP 1 to 0 IRQ FLAG (Bit 4)	When the comparator output goes from "1" to "0" this bit will be set to "1" and an interrupt generated (if bit 4 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
TONE IRQ FLAG (Bit 3)	When RX TONE DECODE (Bit 4, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
DCS IRQ FLAG (Bit 0)	When DCS DECODE/NO DECODE (Bit 7 SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

Table 17: IRQ FLAG Register (Hex address $8F)

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

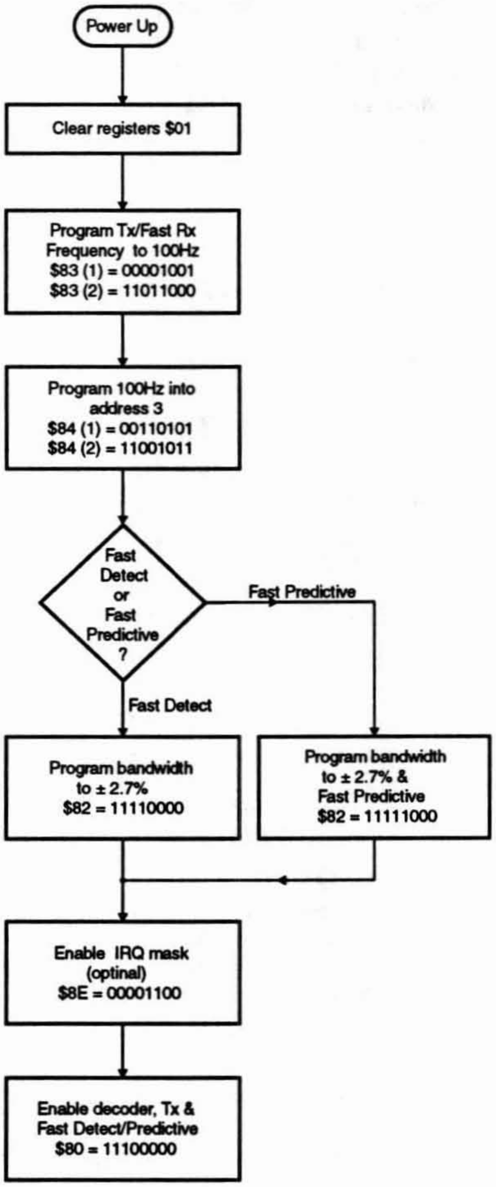
Note: $8X is the Hex address/command.


Power Up
Clear registers $01
Rx or Tx?
Tx
Rx
Program 100Hz into address 3 $84 (1) = 00110101 $84 (2) = 11001011
Program Tx Tone Generator to 100Hz $83 (1) = 00001001 $83 (2) = 11011000
Enable Tx $80 = 10000000
Decoder & Fast Predictive
Decoder or Decoder & Fast Predictive ?
Decoder
Program bandwidth to ±2.7% & Fast Predictive $82 = 11111000
Program bandwidth to ±2.7% $82 = 11110000
Program Fast Rx Frequency to 100Hz $83(1) = 00001001 $83(2) = 11011000
Decoder & Fast Detect
Decoder or Decoder & Fast Detector ?
Decoder
Enable IRQ masks (optional) $8E = 00001100
Enable IRQ mask (optional) $8E = 00001000
Enable Decoder & Fast Detect/Predictive $80 = 01100000
Enable Decoder $80 = 01000000

The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.


Power Up
Clear registers $01
Program Tx/Fast Rx Frequency to 100Hz
$83 (1) = 00001001
$83 (2) = 11011000
Program 100Hz into address 3
$84 (1) = 00110101
$84 (2) = 11001011
Fast Detect or Fast Predictive ?
Fast Predictive
Fast Detect
Program bandwidth to ± 2.7%
$82 = 11110000
Program bandwidth to ± 2.7% & Fast Predictive
$82 = 11111000
Enable IRQ mask (optinal)
$8E = 00001100
Enable decoder, Tx & Fast Detect/Predictive
$80 = 11100000

5. Application

5.1 General

The MX828 is intended for use in radio systems where signaling is required for functions such as trunking, control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permit certainty and signal to noise performance to be traded when congestion or range limits the system performance.

5.2 Transmitters

5.2.1 CTCSS

The CTCSS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX FREQUENCY Register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT (Bits 7 and 5 in the SIGNALING CONTROL Register $80).

5.2.2 The SelCall transmitter

The SelCall transmitter is enabled with Bit 2 in the SIGNALING CONTROL Register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the SELCALL TX Register ($8D) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the SelCall Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL TX ENABLE (Bit 2 in the SIGNALING CONTROL Register $80).

5.2.3 DCS Transmitter

The DCS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx data is set in the DCS BYTE 3, DCS BYTE 2 and DCS BYTE 1 Registers ($85, $86 and $87).

Note: The DCS transmitter produces an inverted output. When the signal is fed through the summing amp, in an inverted configuration, the correct polarity of the DCS signal will be restored (The MOD1 and MOD2 amplifier blocks do not invert).

5.3 Receiver (CTCSS/SelCall Decoder)

The CTCSS/SelCall decoder should first be set up according to the desired characteristics. This entails setting the TONE DECODER MODE Bit 2 of the SIGNALING SET UP Register ($82), and setting the TONE decoder bandwidth in the SIGNALING SET-UP Register ($82), also programming the center frequencies of the desired tones in the RX TONE PROGRAM Register ($84). (It can hold up to 15 different tones). Any tone can be in any location. When the device is decoding, the tones are scanned in the sequence of their location, i.e. $0 first and $E last. Once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The TONE IRQ MASK in the IRQ MASK Register ($8E) should also be set as required.

The TONE DECODER ENABLE in the SIGNALING CONTROL Register ($80) should then be set to "1". While in the CTCSS/SelCall decoder mode the fast/predictive detector may be enabled (see below). (Bit 5 in the SIGNALING CONTROL Register $80).

When the CTCSS/SelCall decoder detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG Register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SELCALL and SUB-AUDIO STATUS Register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (CTCSS Fast/Predictive Detector)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SIGNALING CONTROL Register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK Register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SIGNALING SET-UP Register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX FREQUENCY Register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG Register ($8F), and the CTCSS FAST TONE Bit 6 in the SELCALL and SUB-AUDIO STATUS Register ($81).

5.5 Receiver (DCS Decoder)

The incoming signal is matched with the DCS code programmed into the DCS BYTE 1/2/3 Registers. When the DCS decoder is enabled, the DCS DECODE/NO DECODE FLAG in Bit 7 of the SELCALL and SUB-AUDIO STATUS Register ($81) will be set if the decode is successful (3 or fewer errors). A "0" flag indicates a failure to decode. This flag is updated for every bit of the incoming signal.

In order to detect the DCS turn-off code (134Hz) the CTCSS tone decoder should also be enabled and programmed with this value. Once detected, this will cause a CTCSS tone decoder interrupt, the receiver audio output should then be muted.

5.6 General Purpose Timer (GPT)

This may be used in conjunction with the CTCSS/SelCall decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value in the GENERAL PURPOSE TIMER Register ($8B) set in units of 1msec, an IRQ FLAG in Bit 6 of the IRQ FLAG Register ($8F) and an IRQ MASK in Bit 6 of the IRQ MASK Register ($8E).

5.7 Full Duplex Modes

Although the device is specified as half duplex, the only functions that must operate as such are:

DCS Tx or DCS Rx
DCS Tx or CTCSS Tx
CTCSS decode or SELCALL decode

All other functions are totally independent and therefore a full duplex CTCSS or full duplex SELCALL along with many other combinations are possible.

5.7.1 Tx / Fast Rx Tone Table : CTCSS

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 18: Tx/Fast Rx Tone Table CTCSS

5.7.2 Rx Tone Program Tables : CTCSS

The following table lists the commonly used CTCSS tones together with the values for programming the "RX TONE PROGRAM" register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 19: Rx Tone Program Tables : CTCSS

5.7.3 Tx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'SELCALL TX' register ($8D).

EEA			CCIR			ZVEI 1			ZVEI 2		
Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
1981	01	FD	1981	01	FD	2400	01	A4	2400	01	A4
1124	03	81	1124	03	81	1060	03	B7	1060	03	B7
1197	03	4A	1197	03	4A	1160	03	65	1160	03	65
1275	03	17	1275	03	17	1270	03	1A	1270	03	1A
1358	02	E6	1358	02	E6	1400	02	D0	1400	02	D0
1446	02	B9	1446	02	B9	1530	02	93	1530	02	93
1540	02	8F	1540	02	8F	1670	02	5C	1670	02	5C
1640	02	67	1640	02	67	1830	02	27	1830	02	27
1747	02	41	1747	02	41	2000	01	F8	2000	01	F8
1860	02	1E	1860	02	1E	2200	01	CA	2200	01	CA
1055	03	BB	2400	01	A4	2800	01	68	885	04	73
930	04	3C	930	04	3C	810	04	DC	810	04	DC
2247	01	C1	2247	01	C1	970	04	0F	740	04	0F
991	03	F9	991	03	F9	885	04	73	680	05	CA
2110	01	DE	2110	01	DE	2600	01	84	970	04	0F

Table 20: Tx Tone Program Table : SelCall

5.7.4 Rx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'RX TONE PROGRAM' register ($84) in each Tone Address location as shown.

	EEA			CCIR			ZVEI 1			ZVEI 2		
Tone Address	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq (Hz)	Byte 1 (hex)	Byte 2 (hex)
0	1981	A	A	1981	A	A	2400	C	44	2400	C	44
1	1124	15	C3	1124	15	C3	1060	15	53	1060	15	53
2	1197	26	D	1197	26	D	1160	25	D2	1160	25	D2
3	1275	36	85	1275	36	85	1270	36	83	1270	36	83
4	1358	46	D1	1358	46	D1	1400	47	E	1400	47	E
5	1446	57	4D	1446	57	4D	1530	57	C8	1530	57	C8
6	1540	67	CB	1540	67	CB	1670	68	86	1670	68	86
7	1640	78	4B	1640	78	4B	1830	79	49	1830	79	49
8	1747	88	CD	1747	88	CD	2000	8A	42	2000	8A	42
9	1860	99	84	1860	99	84	2200	9B	43	2200	9B	43
10	1055	A5	51	2400	AC	44	2800	AE	46	885	A4	86
11	930	B4	C4	930	B4	C4	810	B4	14	810	B4	14
12	2247	CB	83	2247	CB	83	970	C4	D8	740	C3	C8
13	991	D5	A	991	D5	A	885	D4	86	680	D3	80
14	2110	EA	C5	2110	EA	C5	2600	ED	45	970	E4	D8

Table 21: Rx Tone Program Table : SelCall

5.7.5 DCS Code Table

The following table gives a list of DCS codes together with the corresponding values (in Hex) which should be programmed into the DCS BYTE registers for a 23-bit DCS sequence.

DCS Code	DCS Byte 3 ($85)	DCS Byte 2 ($86)	DCS Byte 1 ($87)
023	76	38	13
025	6B	78	15
026	65	D8	16
031	51	F8	19
032	5F	58	1A
043	5B	68	23
047	0F	D8	27
051	7C	A8	29
054	6F	48	2C
065	5D	18	35
071	67	98	39
072	69	38	3A
073	2E	68	3B
074	74	78	3C
114	35	E8	4C
115	72	B8	4D
116	7C	18	4E
125	07	B8	55
131	3D	38	59
132	33	98	5A
134	2E	D8	5C
143	37	A8	63
152	1E	C8	6A
155	44	D8	6D
156	4A	78	6E
162	6B	C8	72
165	31	D8	75
172	05	F8	7A
174	18	B8	7C
205	6E	98	85
223	68	E8	93
226	7B	08	96
243	45	B8	A3
244	1F	A8	A4
245	58	F8	A5
251	62	78	A9
261	17	78	B1
263	5E	88	B3
265	43	C8	B5
271	79	48	B9
306	0C	F8	C6
311	38	D8	C9
315	6C	68	CD
331	23	E8	D9
343	29	78	E3
346	3A	98	E6
351	0E	B8	E9
364	68	58	F4
365	2F	08	F5
371	15	88	F9
411	77	69	09
412	79	C9	0A
413	3E	99	0B
423	4B	99	13
431	6C	59	19
432	62	F9	1A
445	7B	89	25
464	27	E9	34
465	60	B9	35
466	6E	19	36
503	3C	69	43
506	2F	89	46
516	41	B9	4E
532	0E	39	5A
546	19	E9	66
565	0C	79	75
606	5D	99	86
612	67	19	8A
624	0F	59	94
627	01	F9	97
631	72	89	99
632	7C	29	9A
654	4C	39	AC
662	24	79	B2
664	39	39	B4
703	22	B9	C3
712	0B	D9	CA
723	39	89	D3
731	1E	49	D9
732	10	E9	DA
734	0D	A9	DC
743	14	D9	E3
754	20	F9	EC

Table 22: DCS Code Table

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308 mV_{RMS} at 1kHz
V_{DD} = 3.3V to 5.0V, T_{AMB}= 25°C, T_{OP} = -40°C to 85°C
Composite Signal = 308 mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31 mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
V_{DD} = 3.3V					
I_{DD}					
All Powersaved	2		0.5	1.0	mA
FAST DETECT Enabled	2		1.7	2.5	mA
Rx Operating					
DCS, FAST DETECT and CTCSS or SelCall	2		3.0	4.5	mA
Tx Operating					
DCS or SelCall or SUB AUDIO	2		1.5	3.0	mA
DCS and SelCall	2		2.5	4.0	mA
V_{DD} = 5.0V					
I_{DD}					
All Powersaved	1, 2		1.0	1.5	mA
FAST DETECT Enabled	1, 2		3.0	4.5	mA
Rx Operating					
DCS, FAST DETECT and CTCSS or SelCall	1, 2		5.5	7.5	mA
Tx Operating					
DCS or SelCall or SUB AUDIO	1, 2		4.5	6.0	mA
DCS and SelCall	1, 2		5.0	6.5	mA
"C-BUS" Interface					
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}
Input Leakage Current Logic "1" or "0"		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic "1" I_{OH} = 120µA		90%			V_{DD}
Output Logic "0" I_{OL} = 360µA				10%	V_{DD}
"Off" State Leakage Current $V_{OUT} = V_{DD}$	6			10	µA
AC Parameters					
TONE Decoder					
Sensitivity Pure Tone	5		-26.0		dB
CTCSS					
Response Time Composite Signal			140		ms
De-response Time Composite Signal			145		ms
Frequency Range		60		253	Hz
SelCall					
Response Time Good Signal			14		ms
De-response Time Good Signal			22		ms
Frequency Range		625		3000	Hz

DCS Decoder						
Bit-Rate Sync Time				2		edges
Sensitivity		1	58		116	mV$_{P-P}$
CTCSS Detector - Fast Detect						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal			56.0		ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Predictive						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal	7		37.0		ms
Frequency Range			60		253	Hz
Decode Bandwidth				40		Hz
CTCSS Encoder						
Frequency Range			60.0		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	+1.0	dB
Total Harmonic Distortion		9		2.0		%
SELCALL Encoder						
Frequency Range			208		3000	Hz
Tone Frequency Resolution					0.2	%
Tone Amplitude Tolerance		1	-1.0		+1.0	dB
Total Harmonic Distortion		9		2.0		%
DCS Encoder						
Bit Rate				134.4		bps
Amplitude Tolerance		1	-1.0		+1.0	dB
Amplitude		1		871		mV$_{P-P}$
Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain (at 1.0kHz)		8		0		dB
Passband Ripple	wrt gain at 1.0kHz	8	-2		+0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz
Output Impedance						
TX AUDIO OUT, TX SUB AUDIO OUT and RX AUDIO OUT						
Enabled		10		2.0		kΩ
Disabled				500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	input = 1mV at 100Hz			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	at 100Hz		10			MΩ
Output Impedance	Open Loop			6.0		kΩ

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Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation	at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error	wrt attenuation at 0dB		-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	at 100Hz			15.0		kΩ
Mod.2 Attenuator						
Attenuation	at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error	wrt attenuation at 0dB		-0.6		0.6	dB
Output Impedance		3		600		Ω
General Purpose Timer						
Timing Period Range			1		255	ms
Count Interval				1		ms
Xtal/Clock Input						
Pulse Width	('High' or 'Low'	4	40.0			ns
Input Impedance	(at 100Hz)		10.0			MΩ
Gain	input = 1mV$_{RMS}$ at 100Hz		20.0			dB
D/A						
Range		1	312.5		2500	mV
Step Size		1		312.5		mV
Step Accuracy		1	-30		30	mV
Input Impedance	COMPIN			10		MΩ
Output Impedance	COMPOUT			1		kΩ

Table 23: Operating Characteristics

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance, at V_{DD} = 5.0V and T_{AMB} = 25°C.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{IRQ}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD 1 or MOD 2 output.
10. SUBAUDIO, SELCALL and DCS.

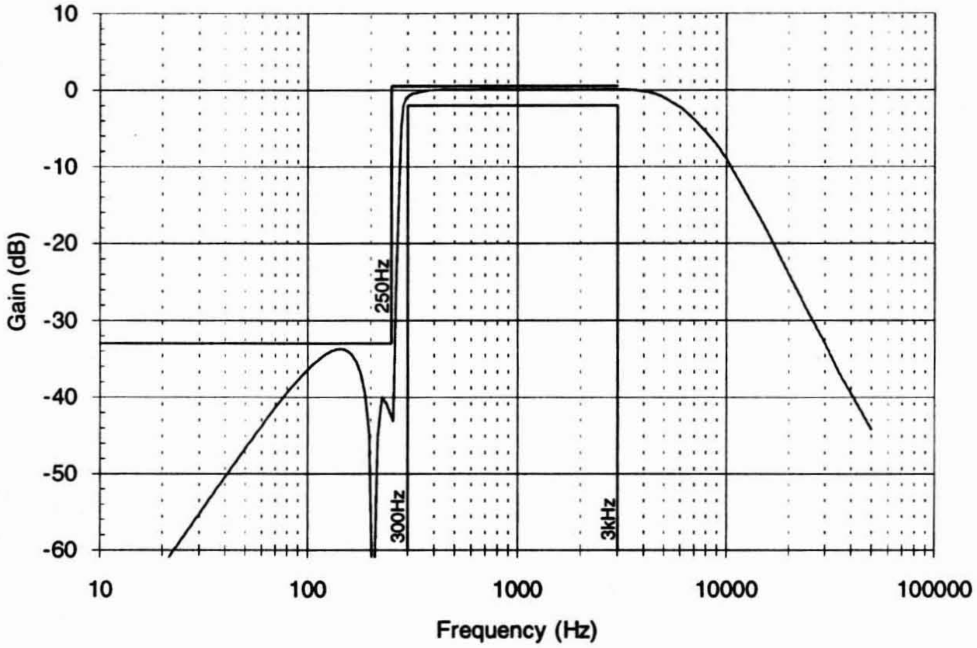


Figure 3: Audio Band-Pass Filter Frequency Response

6.2 Timing Diagrams

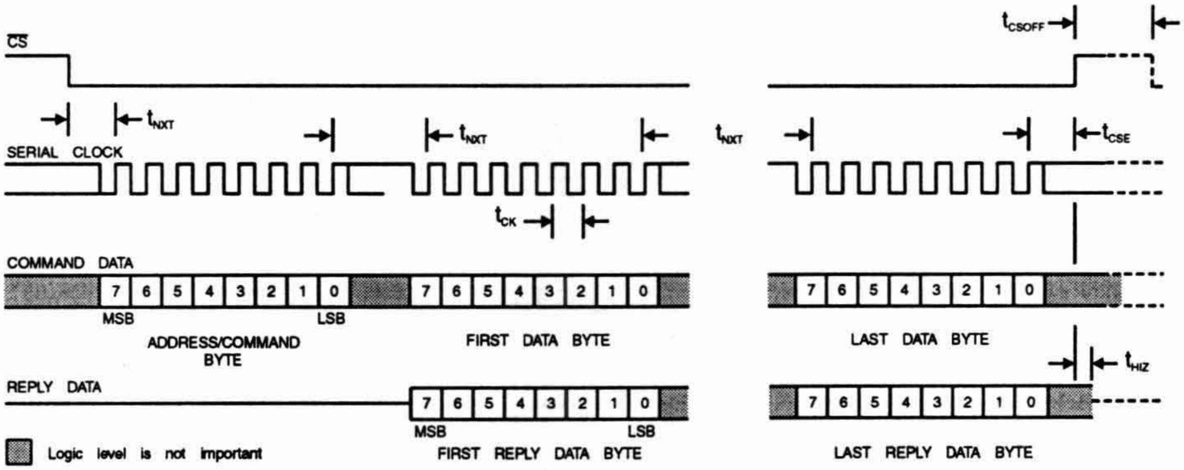
For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = -40°C to +85°C.

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs

Notes:

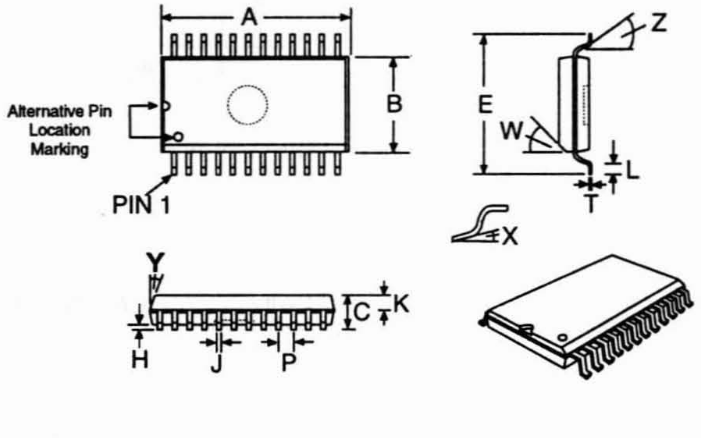
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.



$\overline{CS}$
t_{CSOFF}
t_{NXT}
SERIAL CLOCK
t_{NXT}
t_{NXT}
t_{CSE}
t_{CK}
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
t_{HIZ}
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
▨ Logic level is not important

Figure 4: "C-BUS" Timing

6.3 Packaging

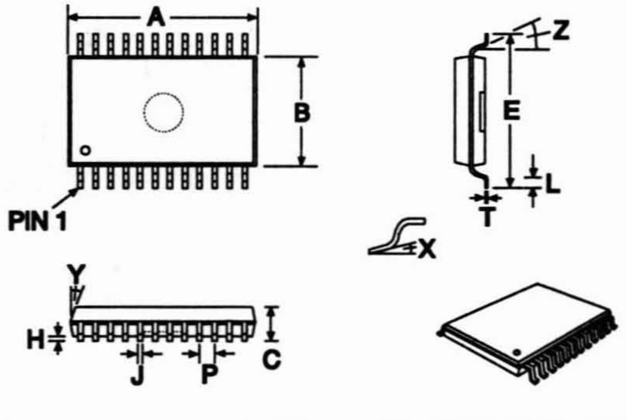


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin SOIC Mechanical Outline: *Order as part no. MX828DW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SSOP Mechanical Outline: *Order as part no. MX828DS*

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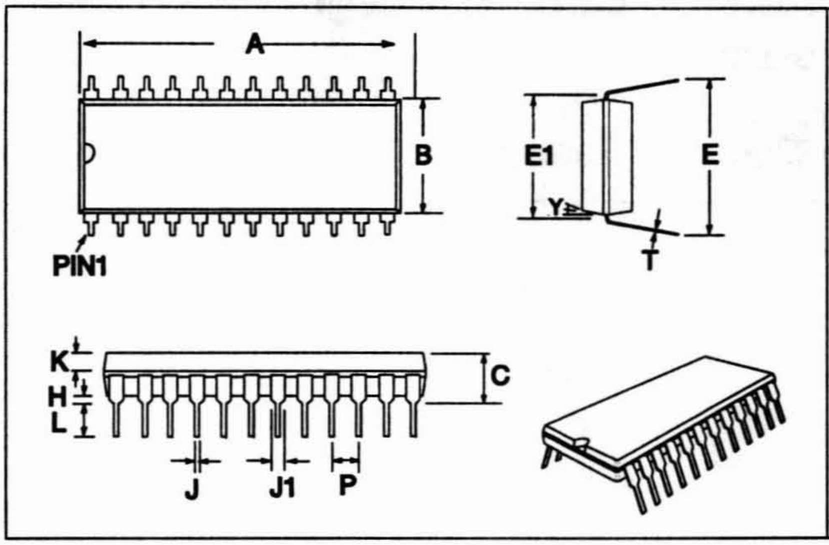


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: Figure 5: 24-pin PDIP Mechanical Outline: Order as part no. MX828P

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX829 Baseband Signal Processor

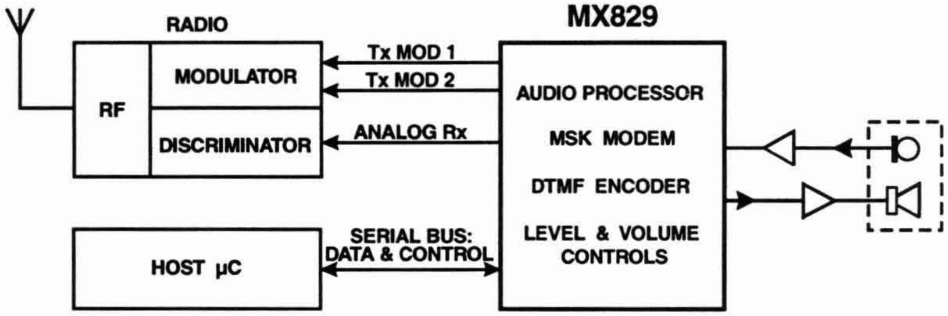
PRELIMINARY INFORMATION

Features

- Rx Audio Processing
- Tx Audio Processing
- 1200/2400 Baud Modem
- DTMF Encoder
- Low Voltage Operation
- "C-BUS" Compatible
- Host µC Interface

Applications

- ETS/MPT/PAA Standards Compatible
- LMR/PAMR/PMR Trunked Systems
- Multi-standard Modem Formats



The MX829 is a low voltage CMOS integrated circuit, designed to provide baseband audio and system signal-processing functions required for LMR/PAMR/PMR trunked radio applications. The MX829 operates in half-duplex mode under the serial-bus control of a host µC.

The MX829 incorporates a dual-rate 1200/2400bps MSK modem, with a software-flexible choice of synchronization codewords, data run-length and CRC checking to suit a wide range of applications. These features allow very flexible handling of user defined data on traffic channels in addition to the network signaling sent on control channels. A 16 character DTMF encoder is available in the transmit mode. Software programmable output level-adjustment facilitates two-point modulation circuits.

The audio processing stages include transmit and receive filtering (based on standards specified for 12.5kHz and 25kHz LMR/PAMR/PMR channel operation), transmit deviation limiting, and a programmable Rx volume control. Power saving is automatic when audio functions are disabled.

The MX829 is designed for use in radios compatible with MPT1327, PAA1382 and ETS 300 086 Trunking Standards. The features and flexibility of the MX829 ensure that it is equally suitable for use with modified or proprietary standards.

The MX829 is available in the following packages: 24-pin SSOP (MX829DS), 24-pin SOIC (MX829DW), and 24-pin PDIP (MX829P).

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1. Block Diagram

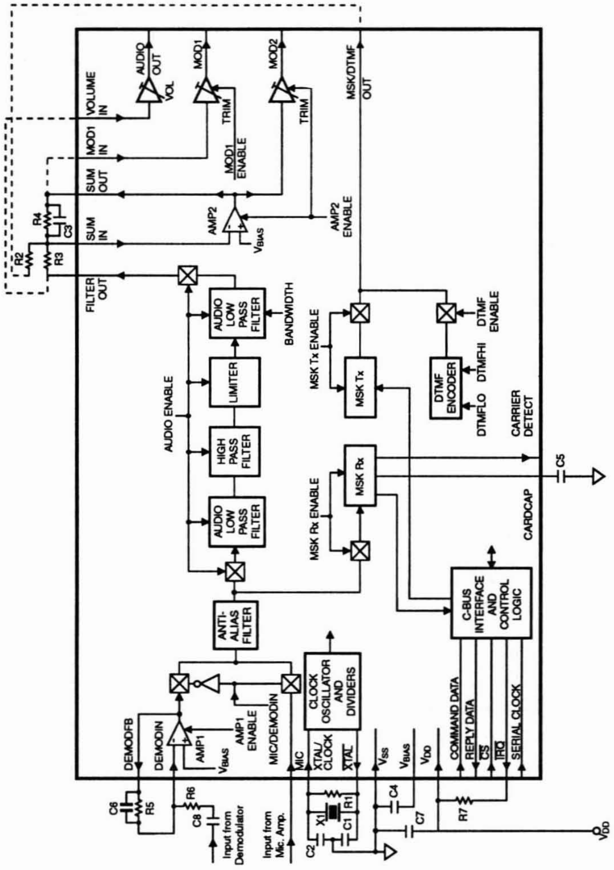
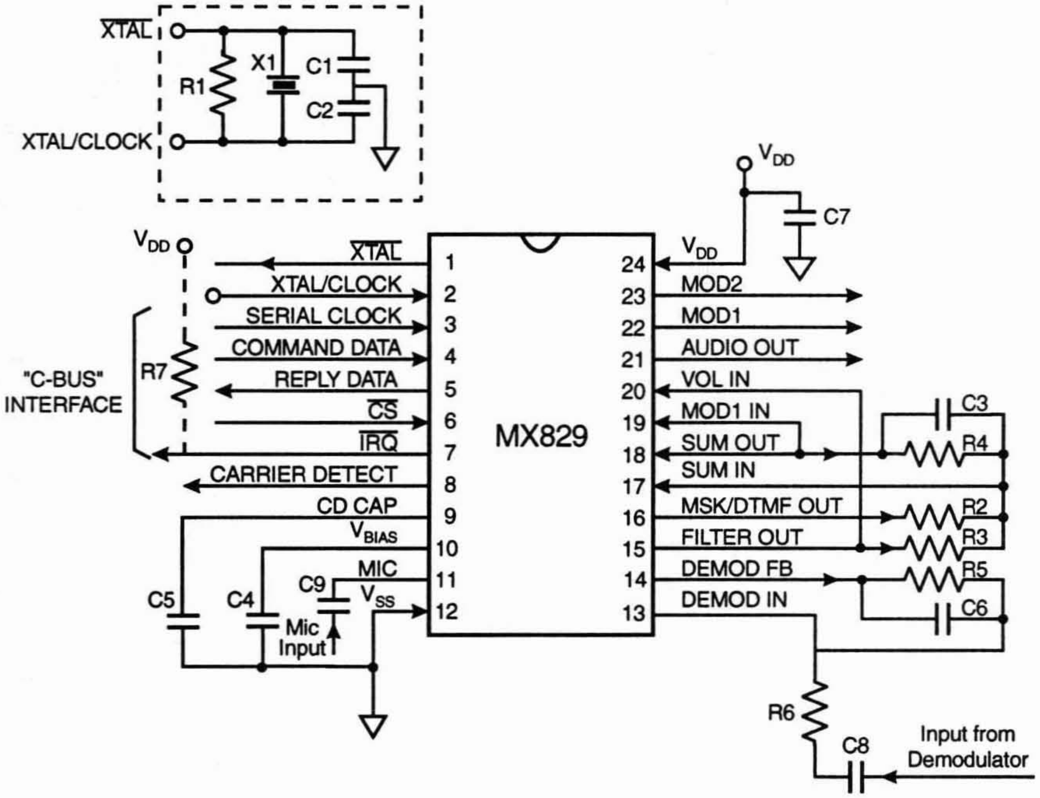

R2
R3
R4
C3
FILTER OUT
SUM IN
SUM OUT
MOD1 IN
VOLUME IN
AUDIO OUT
VOL
MOD1
TRIM
MOD2
TRIM
AMP2
VBIAS
MOD1 ENABLE
AMP2 ENABLE
AUDIO ENABLE
ANTI-ALIAS FILTER
AUDIO LOW PASS FILTER
HIGH PASS FILTER
LIMITER
AUDIO LOW PASS FILTER
BANDWIDTH
MSK Rx ENABLE
MSK Tx ENABLE
MSK Rx
MSK Tx
MSK/DTMF OUT
DTMF ENCODER
DTMFLO
DTMFHI
DTMF ENABLE
CARRIER DETECT
CARDCAP
C5
C6
R5
DEMODFB
DEMODIN
R6
C8
AMP1
VBIAS
AMP1 ENABLE
MIC/DEMODIN
Input from Demodulator
Input from Mic. Amp.
MIC
XTAL/CLOCK
XTAL
C2
X1
C1
R1
CLOCK OSCILLATOR AND DIVIDERS
VSS
VBIAS
VDD
C4
C7
R7
COMMAND DATA
REPLY DATA
CS
IRQ
SERIAL CLOCK
C-BUS INTERFACE AND CONTROL LOGIC
VDD

Figure 1: Block Diagram

2. Signal List

PIN NO	SIGNAL	TYPE	DESCRIPTION
1	$\overline{\text{XTAL}}$	output	Inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	"C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See section 7.1.4
4	COMMAND DATA	input	"C-BUS" serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See section 7.1.4.
5	REPLY DATA	output	"C-BUS" serial data output to the µController. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This 3-state output is held at high impedance when not sending data to the µController. See section 7.1.4.
6	$\overline{\text{CS}}$	input	"C-BUS" data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See section 7.1.4.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pull-up resistor is required. The conditions that cause interrupts are indicated in the STATUS register and are effective if not masked out by a corresponding bit in the CONTROL register. The reading of the Status Register resets the IRQ to a high impedance and sets the contents of the Status Register to 0.
8	CARRIER DETECT	output	The carrier detect output for the MSK Rx.
9	CD CAP	output	The carrier detect integrating capacitor.
10	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to a capacitor mounted close to the device pins.
11	MIC	input	AC coupled Tx audio input (external amplification is required for use as a microphone input).
12	V_{SS}	Power	Negative supply (ground).
13	DEMOD IN	input	AC coupled inverting input to the Rx input amplifier (AMP1).
14	DEMOD FB	output	Output of the Rx input amplifier (AMP1)
15	FILTER OUT	output	Output of the audio filter/limiter section. In powersave mode this output is connected to V_{BIAS} via a 500kΩ resistor.
16	MSK/DTMF OUT	output	The 1200 or 2400 baud MSK Tx output and the DTMF encoder output. When enabled but not transmitting MSK or DTMF signals, or when in powersave mode, this output is connected to V_{BIAS} via a 500kΩ resistor. On power-up, this output can be any level: a General Reset command is required to ensure that this output attains V_{BIAS} initially.
17	SUM IN	input	Input to the audio summing amplifier (AMP2).
18	SUM OUT	output	Output of the audio summing amplifier (AMP2).
19	MOD1 IN	input	Input to MOD1 audio gain control.
20	VOL IN	input	Input to the audio volume control.
21	AUDIO OUT	output	Output of the audio volume control.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

3. External Components



$\overline{XTAL}$
XTAL/CLOCK
R1
X1
C1
C2
V_{DD}
C7
"C-BUS" INTERFACE
R7
1 $\overline{XTAL}$
2 XTAL/CLOCK
3 SERIAL CLOCK
4 COMMAND DATA
5 REPLY DATA
6 $\overline{CS}$
7 $\overline{IRQ}$
8 CARRIER DETECT
9 CD CAP
10 V_{BIAS}
11 MIC
12 V_{SS}
MX829
24 V_{DD}
23 MOD2
22 MOD1
21 AUDIO OUT
20 VOL IN
19 MOD1 IN
18 SUM OUT
17 SUM IN
16 MSK/DTMF OUT
15 FILTER OUT
14 DEMOD FB
13 DEMOD IN
C3
R4
R2
R3
R5
C6
C5
C4
C9
Mic Input
R6
C8
Input from Demodulator

Figure 2: Recommended External Components

C1		22pF	±20%
C2		22pF	±20%
C3		68pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±10%
C6		100pF	±20%
C7		0.1µF	±20%
C8	Note 2		±20%
C9		5.6nF	±20%

R1		1MΩ	±5%
R2	Note 1		±10%
R3	Note 1		±10%
R4		100kΩ	±10%
R5		100kΩ	±10%
R6	Note 2		±10%
R7		22kΩ	±10%
X1	Note 3	4.032MHz	±100ppm

External Component Notes:

1. R2, R3, R4 and C3 form the gain components for the Summing Amplifier (AMP2).

   R2 and R3 should be chosen as required from the system specification, using the following formula:

   $$\text{Audio Gain} = -\frac{R4}{R3} \qquad \text{DTMF Gain} = -\frac{R4}{R2}$$

2. R5, R6, C6 and C8 form the gain components for the Rx Input Amplifier (AMP1).

   R6 should be chosen as required by the signal level, using the following formula:

$$\text{Gain} = -\frac{R5}{R6}$$

   C8 x R6 should be chosen so as not to compromise the low frequency performance of this product.

3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX829 consists of five main sections: the Audio Filter, the Programmable Attenuators, the DTMF encoder, the MSK transmitter, and the MSK receiver. These sections are controlled via a serial ("C-BUS") interface. The five sections are described below.

4.1 Audio Filtering

This consists of an input amplifier and a common audio filter section, which may be switched between Rx and Tx. The filter section comprises an anti-alias filter followed by low-pass and high-pass filtering with an amplitude limiter to set the maximum deviation. Three variable attenuation blocks may be used to set the volume (in Rx) or the modulation level (in Tx). Pre- and de-emphasis can be added externally using resistors and capacitors around AMP1, AMP2 and the microphone amplifiers, see Figure 7,Figure 8, and Figure 9. The anti-alias filter is designed to reduce aliasing effects above 50kHz which is approximately half the internal filter's sample rate.

The filtering is designed to meet the ETS 300 086 specification.

Various powersave modes are incorporated.

4.2 MOD1 and MOD2 Attenuators

The MOD1 input can be connected directly to SUM OUT, so that the MOD1 and MOD2 outputs can then be used for two point modulation. Alternatively, the MOD1 attenuator can be used for auxiliary gain adjustment, in which case the input signal must be ac coupled with a suitable capacitor.

4.3 DTMF Encoder

This generates the standard DTMF tones according to the CONTROL 2 Register settings. It also has a powersave mode.

4.4 MSK Tx

The Tx function of the MSK modem continuously operates in a free format mode, which means that the preamble and frame sync have to be programmed like normal data bytes. However, a 2-byte checksum may be generated automatically by simply marking the beginning and end of the data to be used. Any number of whole bytes may be used to generate the checksum.

After the last byte has been transmitted one additional "hang bit" is automatically added to the end. All Tx operations are programmed from the "C-BUS" via an 8-bit buffer. The Tx part of the MSK Modem has a Powersave mode

The modulation output is one cycle of 1200Hz for a "1" and one and a half cycles of 1800Hz for a "0" at 1200 baud, or one half cycle of 1200Hz for a "1" and one cycle of 2400Hz for a "0" at 2400 baud.

4.5 MSK Rx

In Rx, the modem automatically achieves bit sync and then recognizes the previously selected SYNC and/or SYNT word of the MPT1327, ETS 300 230 or PAA1382 specifications. At the same time as one of the above, it can also recognize a user programmed 16-bit RX SYNC WORD.

On reception of the SYNC, SYNT or RX SYNC WORD, the device will automatically (or manually at any time) start checking the data and checksum. It provides a 1-bit correct/incorrect result every byte, so that any number of bytes can be checked.

The Rx part of the MSK modem operates at 1200 or 2400 baud and has a powersave mode. Both MSK Rx and Tx work in half duplex mode.

5. Software Description

5.1 Address/Commands

Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 14.

Instruction and data transactions to and from the MX829 consist of an Address/Command (A/C) byte followed by either:

1. a further instruction or data (1 or 2 bytes)
2. a status or Rx data reply (1 byte)

5.1.1 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$10	CONTROL 1	AMP1	AMP2	AUDIO	MSKRX	MSKTX	UK/F	MIC	B/W
$11	CONTROL 2	CHKSUM	DTMFEN	DTMFHI	DTMFLO	DTMF3	DTMF2	DTMF1	DTMF0
$13	AUDIO				<---------- GAIN ---------->				
	ATTENUATION	0	0	0	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$40	CONTROL 3/ IRQ ENABLE	0	1200/2400	TXIDLEM	RXDATAM	TXDATAM	RX SYNC WORD PRIME	SYNT PRIME	SYNC PRIME
$43	TXDATA	<---------- TXDATA ---------->							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.1.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$12	MOD LEVELS			MOD 1	<---------- MOD 1 ---------->				
	(1)	0	0	ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
					<---------- MOD 2 ---------->				
	(2)	0	0	0	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$44	RX SYNC	<---------- RX SYNC WORD ---------->							
	WORD (1)	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		<---------- RX SYNC WORD ---------->							
	(2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.2 Write Only Register Description

5.2.1 RESET Register (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific states as listed below:

REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
CONTROL 1	0	0	0	0	0	0	0	0
CONTROL 2	0	0	0	0	0	0	0	0
CONTROL 3/IRQ ENABLE	0	0	0	0	0	0	0	0
AUDIO ATTENUATION	0	0	0	0	0	0	0	0
TXDATA	X	X	X	X	X	X	X	X
MOD LEVELS (1)	0	0	0	0	0	0	0	0
MOD LEVELS (2)	0	0	0	0	0	0	0	0
RX SYNC WORD (1)	X	X	X	X	X	X	X	X
RX SYNC WORD (2)	X	X	X	X	X	X	X	X
STATUS	0	0	0	0	0	0	0	0
RXDATA	X	X	X	X	X	X	X	X

X = undefined

5.2.2 CONTROL1 Register (Hex address $10)

This register is used to control the functions of the device as described below:

AMP1 **(Bit 7)**	When this bit is "1", AMP1 is enabled. When this bit is "0", AMP1 is disabled (i.e. powersaved).
AMP2 **(Bit 6)**	When this bit is "1", both AMP2 and MOD2 are enabled. When this bit is "0", both AMP2 and MOD2 are disabled (i.e. powersaved) and the MOD2 output is pulled to V_{BIAS} via a 1MΩ resistor.
AUDIO **(Bit 5)**	When this bit is "1", the audio filter/limiter section is enabled. When this bit is "0", the audio filter/limiter section is disabled (i.e. powersaved).
MSKRX **(Bit 4)**	When this bit is "1", the MSK Rx is enabled. When this bit is "0", the MSK Rx is disabled (i.e. powersaved).

Note: The MSK Rx and Tx cannot both be enabled at the same time. If both MSKRX and MSKTX are "1", then they will both be disabled (i.e. powersaved).

MSKTX **(Bit 3)**	When this bit is "1", the MSK Tx is enabled. When this bit is "0", the MSK Tx is disabled (i.e. powersaved).

Note: The MSK Tx and Rx cannot both be enabled at the same time. If both MSKTX and MSKRX are "1", then they will both be disabled (i.e. powersaved).

The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then they will both be disabled.

UK/F **(Bit 2)**	When this bit is "1", the SYNC/SYNT is set to the PAA standard of "1011010000110011" (SYNC) When this bit is "0", the SYNC/SYNT is set to the MPT standard of "1100010011010111" (SYNC)
MIC **(Bit 1)**	When this bit is "1", the MIC input is enabled and the AMP1 (DEMODIN) input is disabled. When this bit is "0", the AMP1 (DEMODIN) input is enabled and the MIC input is disabled.
B/W **(Bit 0)**	When this bit is "1", the bandwidth of the audio path is set wide for 20kHz/25kHz RF channel spacing. When this bit is "0", the bandwidth of the audio path is set narrow for 12.5kHz RF channel spacing.

5.2.3 CONTROL 2 Register (Hex address $11)

This register is used to control the functions of the device as described below:

CHKSUM **(Bit 7)**	In the Tx mode, when this bit is "1", the checksum generator is enabled. All complete bytes that are transmitted after this time are used in the checksum calculation. When this bit goes from "1" to "0", the checksum generator will complete its calculations on the current byte and the result will be sent as the next two bytes of transmitted data. In the Rx mode, the "0" to "1" transition of the CHKSUM bit is used at the start of the next byte received at DEMODIN to manually reset the Rx checksum calculation, see Figure 4. The calculation can also be reset automatically by a SYNC, SYNT, or RX SYNC WORD detection - see section 5.2.5. In this case, the Rx checksum calculation starts with the first data byte after the 2-byte sync word has been detected. The CHKSUM bit can be reset to "0" at any time. The result of the checksum is made available in the STATUS Register after the reception of every complete byte (See section 5.3.1). Note that the device is designed to work with any message length, and as a consequence it is not aware of the position of the checksum within the incoming data message. It thus performs a checksum assessment after every received byte. The controlling software should use its knowledge of the system message length in order to determine which RXSUMF reading is valid, i.e. after the second of the two checksum bytes has been received. The timing of data bytes relative to the checksum bit is shown in Figure 3 and Figure 4.

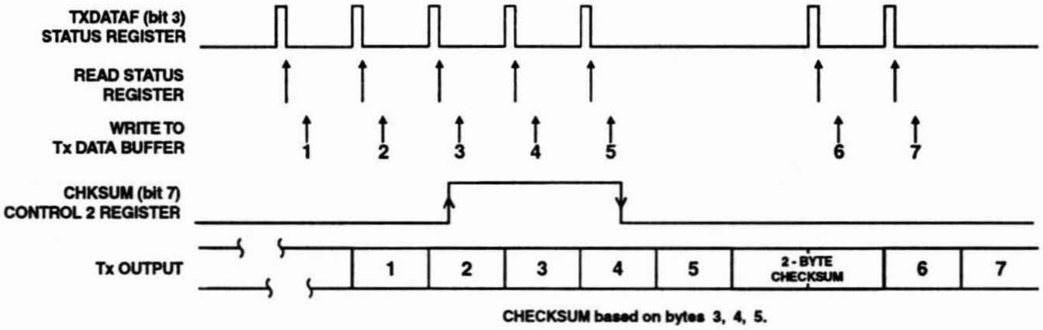

TXDATAF (bit 3)
STATUS REGISTER
READ STATUS
REGISTER
WRITE TO
Tx DATA BUFFER
1
2
3
4
5
6
7
CHKSUM (bit 7)
CONTROL 2 REGISTER
Tx OUTPUT
1
2
3
4
5
2 - BYTE CHECKSUM
6
7
CHECKSUM based on bytes 3, 4, 5.

Figure 3: Checksum Generation in Tx Mode

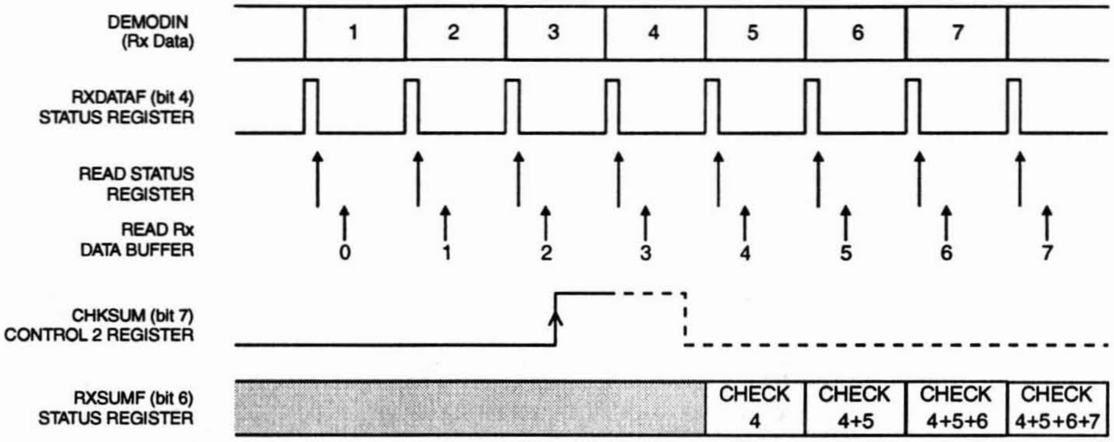

DEMODIN
(Rx Data)
1
2
3
4
5
6
7
RXDATAF (bit 4)
STATUS REGISTER
READ STATUS
REGISTER
READ Rx
DATA BUFFER
0
1
2
3
4
5
6
7
CHKSUM (bit 7)
CONTROL 2 REGISTER
RXSUMF (bit 6)
STATUS REGISTER
CHECK 4
CHECK 4+5
CHECK 4+5+6
CHECK 4+5+6+7

Figure 4: Checksum Calculation in Rx Mode

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DTMFEN **(Bit 6)**	When this bit is "1", the DTMF output is enabled. When this bit is "0", the DTMF output is disabled. As the powersave of the DTMF is performed in the DTMFHI and DTMFLO registers, this bit allows a fast start up time for the tones.

Note: The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then both will be disabled.

DTMFHI **(Bit 5)**	When this bit is "1", the DTMF high frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF high frequency tone generator is disabled (i.e. powersaved).
DTMFLO **(Bit 4)**	When this bit is "1", the DTMF low frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF low frequency tone generator is disabled (i.e. powersaved).
DTMF3, DTMF2, DTMF1, DTMF0 **(Bit 3, Bit 2, Bit 1, Bit 0)**	These four bits define the DTMF tones according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	DTMF Tones	DTMF 'Digit'
0	0	0	0	1209Hz + 697Hz	1
0	0	0	1	1209Hz + 770Hz	4
0	0	1	0	1209Hz + 852Hz	7
0	0	1	1	1209Hz + 941Hz	*
0	1	0	0	1337Hz + 697Hz	2
0	1	0	1	1337Hz + 770Hz	5
0	1	1	0	1337Hz + 852Hz	8
0	1	1	1	1337Hz + 941Hz	0
1	0	0	0	1478Hz + 697Hz	3
1	0	0	1	1478Hz + 770Hz	6
1	0	1	0	1478Hz + 852Hz	9
1	0	1	1	1478Hz + 941Hz	#
1	1	0	0	1634Hz + 697Hz	A
1	1	0	1	1634Hz + 770Hz	B
1	1	1	0	1634Hz + 852Hz	C
1	1	1	1	1634Hz + 941Hz	D

5.2.4 AUDIO ATTENUATION Register (Hex Address $13)

The five least significant bits in this register are used to set the attenuation of the audio volume control according to the table below:

4	3	2	1	0		Audio Attenuation
0	0	0	0	0		Off
0	0	0	0	1		48.0dB
0	0	0	1	0		46.4dB
0	0	0	1	1		44.8dB
0	0	1	0	0		43.2dB
0	0	1	0	1		41.6dB
0	0	1	1	0		40.0dB
0	0	1	1	1		38.4dB
0	1	0	0	0		36.8dB
0	1	0	0	1		35.2dB
0	1	0	1	0		33.6dB
0	1	0	1	1		32.0dB
0	1	1	0	0		30.4dB
0	1	1	0	1		28.8dB
0	1	1	1	0		27.2dB
0	1	1	1	1		25.6dB
1	0	0	0	0		24.0dB
1	0	0	0	1		22.4dB
1	0	0	1	0		20.8dB
1	0	0	1	1		19.2dB
1	0	1	0	0		17.6dB
1	0	1	0	1		16.0dB
1	0	1	1	0		14.4dB
1	0	1	1	1		12.8dB
1	1	0	0	0		11.2dB
1	1	0	0	1		9.6dB
1	1	0	1	0		8.0dB
1	1	0	1	1		6.4dB
1	1	1	0	0		4.8dB
1	1	1	0	1		3.2dB
1	1	1	1	0		1.6dB
1	1	1	1	1		0dB

Note: Bits 5, 6 and 7 should always be set to "0".

5.2.5 CONTROL 3 / IRQ ENABLE Register (Hex address $40)

This register is a mixture of control bits and interrupt mask bits, as detailed below:

Bit 7	Not used, set to zero.
1200/2400 **(Bit 6)**	When this bit is "1", the MSK Rx and Tx are set to operate at 1200 baud. When this bit it "0", the MSK Rx and Tx are set to operate at 2400 baud.
TXIDLEM **(Bit 5)**	When this bit is "1", the TXIDLE interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXIDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RXDATAM **(Bit 4)**	When this bit is "1", the RXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the RXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TXDATAM **(Bit 3)**	When this bit is "1", the TXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RX SYNC WORD PRIME **(Bit 2)**	When this bit is set to "1", it enables the RX SYNC WORD detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNT PRIME **(Bit 1)**	When this bit is set to "1", it enables the SYNT detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNC PRIME **(Bit 0)**	When this bit is set to "1", it enables the SYNC detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

5.2.6 TXDATA Register (Hex Address $43)

This is the Tx data output register. It is double buffered, thus giving the user up to 8 bit periods to load in the next 8 bits. MSK data is transmitted immediately it is loaded if the transmitter is idle. Data is transmitted in 8-bit bytes, bit 7 (MSB) will be transmitted first.

5.2.7 MOD LEVELS Register **(Hex address $12)**

The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the five least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

5	**4**	**3**	**2**	**1**	**0**		**Mod. 1 Attenuation**
0	X	X	X	X	X		Disabled (V_{BIAS})
1	0	0	0	0	0		>40dB
1	0	0	0	0	1		12.0dB
1	0	0	0	1	0		11.6dB
1	0	0	0	1	1		11.2dB
1	0	0	1	0	0		10.8dB
1	0	0	1	0	1		10.4dB
1	0	0	1	1	0		10.0dB
1	0	0	1	1	1		9.6dB
1	0	1	0	0	0		9.2dB
1	0	1	0	0	1		8.8dB
1	0	1	0	1	0		8.4dB
1	0	1	0	1	1		8.0dB
1	0	1	1	0	0		7.6dB
1	0	1	1	0	1		7.2dB
1	0	1	1	1	0		6.8dB
1	0	1	1	1	1		6.4dB
1	1	0	0	0	0		6.0dB
1	1	0	0	0	1		5.6dB
1	1	0	0	1	0		5.2dB
1	1	0	0	1	1		4.8dB
1	1	0	1	0	0		4.4dB
1	1	0	1	0	1		4.0dB
1	1	0	1	1	0		3.6dB
1	1	0	1	1	1		3.2dB
1	1	1	0	0	0		2.8dB
1	1	1	0	0	1		2.4dB
1	1	1	0	1	0		2.0dB
1	1	1	0	1	1		1.6dB
1	1	1	1	0	0		1.2dB
1	1	1	1	0	1		0.8dB
1	1	1	1	1	0		0.4dB
1	1	1	1	1	1		0dB

4	**3**	**2**	**1**	**0**		**Mod. 2 Attenuation**
0	0	0	0	0		>40dB
0	0	0	0	1		6.0dB
0	0	0	1	0		5.8dB
0	0	0	1	1		5.6dB
0	0	1	0	0		5.4dB
0	0	1	0	1		5.2dB
0	0	1	1	0		5.0dB
0	0	1	1	1		4.8dB
0	1	0	0	0		4.6dB
0	1	0	0	1		4.4dB
0	1	0	1	0		4.2dB
0	1	0	1	1		4.0dB
0	1	1	0	0		3.8dB
0	1	1	0	1		3.6dB
0	1	1	1	0		3.4dB
0	1	1	1	1		3.2dB
1	0	0	0	0		3.0dB
1	0	0	0	1		2.8dB
1	0	0	1	0		2.6dB
1	0	0	1	1		2.4dB
1	0	1	0	0		2.2dB
1	0	1	0	1		2.0dB
1	0	1	1	0		1.8dB
1	0	1	1	1		1.6dB
1	1	0	0	0		1.4dB
1	1	0	0	1		1.2dB
1	1	0	1	0		1.0dB
1	1	0	1	1		0.8dB
1	1	1	0	0		0.6dB
1	1	1	0	1		0.4dB
1	1	1	1	0		0.2dB
1	1	1	1	1		0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved). Bits 6 and 7 in the first byte and bits 5, 6 and 7 in the second byte should always be set to "0". MOD LEVELS (1) register is loaded first.

Note: The MOD2 attenuator is enabled by the AMP2 ENABLE signal (bit 6 of CONTROL1 register).

5.2.8 RX SYNC WORD Register (Hex $44)

This is a two byte register that defines the 16-bit programmable synchronization word. This word is compared with the incoming Rx data and, if a match is found, it is indicated in the STATUS register and an interrupt is generated. Bit 15, the MSB of the first byte, is loaded first.

8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$41	STATUS	0	RXSUMF	TXIDLEF	RXDATAF	TXDATAF	RX SYNC WORDF	SYNTF	SYNCF
$42	RXDATA	<-- RXDATA -->							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.3 Read Only Register Description

5.3.1 STATUS Register (Hex address $41)

This register is used to indicate the status of the device as described below:

Note: After reading the contents of the Status Register, all bits in the Status Register are reset to a zero state and the IRQ, externally generated by the MX829, is cleared.

Bit 7	Not used, always set to zero.
RXSUMF (Bit 6)	When this bit is "1", the Rx checksum is correct. When this bit is "0", the Rx checksum is incorrect. This bit is updated and latched in, after reception of every eight bits (see section 5.2.3).
TXIDLEF (Bit 5)	When all the Tx data and any checksum and one "hang-bit" have been transmitted, this bit will be set to "1" to indicate that the transmitter is idle. This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXIDLEM bit in the CONTROL 3 / IRQ ENABLE register.
RXDATAF (Bit 4)	When a full byte of data is received and is available in the RXDATA register, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1" an interrupt may be generated depending on the state of the RXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
TXDATAF (Bit 3)	When the Tx data buffer is empty this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
RX SYNC WORDF (Bit 2)	This bit is only defined when RX SYNC WORD PRIME is enabled. When the data sequence specified in the RX SYNC WORD register has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNTF (Bit 1)	This bit is only defined when SYNT PRIME is enabled. When the data sequence specified by SYNT has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNCF (Bit 0)	This bit is only defined when SYNC PRIME is enabled. When the data sequence specified by SYNC has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

5.3.2 RXDATA Register **(Hex address $42)**

This register contains the last byte of data received. It is updated every 8 bits at the same time as the RXSUMF bit in the STATUS register is updated.

The RXDATA register is double buffered, thus giving the user up to 8 bit periods to read the data before it is overwritten by the next byte.

5.4 MSK Checksum Generation and Checking

5.4.1 Generation

The checksum generator takes the m x 8 bits from the m bytes of information, sequentially loaded into the TXDATA register and divides them modulo-2, by the generating polynomial:

X15 + X14 + X13 + X11 + X4 + X2 + 1

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial m x 8 bits and the 15-bit remainder (with the last bit inverted).

This 16-bit word is used as the "CHECKSUM". See Figure 5.

(m = the number of bytes in the information to be sent)

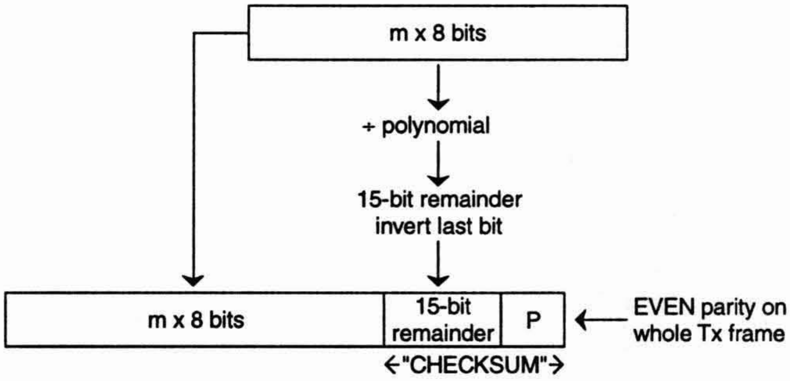

m x 8 bits
÷ polynomial
15-bit remainder
invert last bit
m x 8 bits
15-bit remainder
P
EVEN parity on whole Tx frame
←"CHECKSUM"→

Figure 5: Checksum Generation

5.4.2 Checking

The checksum checker performs two tasks:

It takes the first n-1 bits of a received (n = 8m + 16 bits) message, inverts bit n-1, and divides them modulo-2, by the generating polynomial:

X15 + X14 + X13 + X11 + X4 + X2 + 1

The 15 bits remaining in the polynomial divider are checked for all zero.

Secondly, it generates an EVEN parity bit from the first n-1 bits of a received message and compares this bit with the received parity bit (bit n). See Figure 6.

If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RXSUMF bit (STATUS register bit 6) is set. This is updated and latched every 8 bits, starting at the bit immediately after the initialization of the bit counter. This initialization takes place on detection of frame synchronization, i.e. the matching of received data to the SYNC, SYNT or RX SYNC WORD.

Note that the checksum is calculated on the received data before it is double buffered (see Figure 4).

n = the number of bits in the received message

m = the number of bytes of transmitted data, excluding checksum

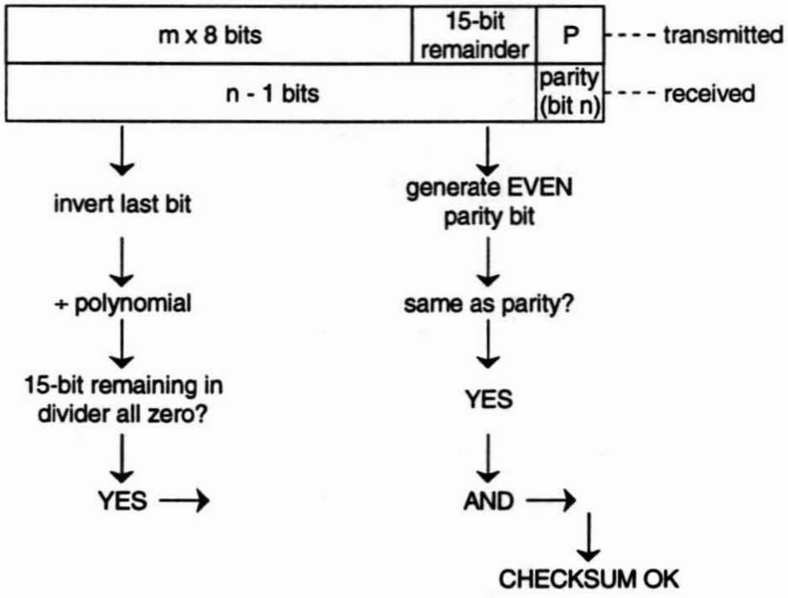

m x 8 bits
15-bit remainder
P
transmitted
n - 1 bits
parity (bit n)
received
invert last bit
+ polynomial
15-bit remaining in divider all zero?
YES
generate EVEN parity bit
same as parity?
YES
AND
CHECKSUM OK

Figure 6: Checksum Checking

6. Application

The following block diagrams show the possible arrangements for the pre- and de-emphasis required by PAA1382 and MPT1327 specifications.

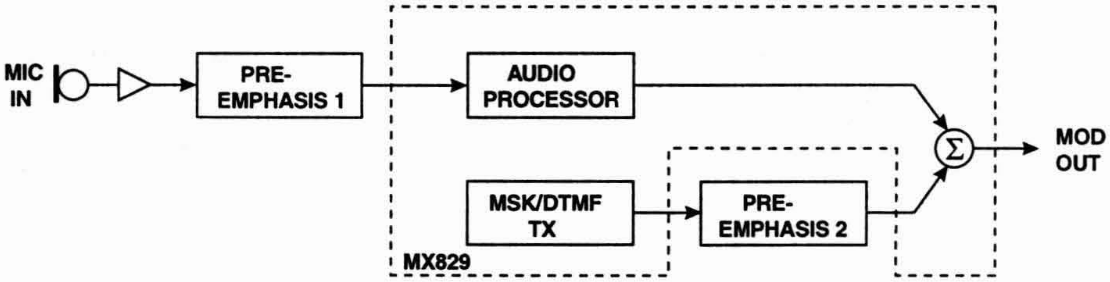

MIC IN
PRE-EMPHASIS 1
AUDIO PROCESSOR
MSK/DTMF TX
PRE-EMPHASIS 2
Σ
MOD OUT
MX829

Figure 7: Transmitter Pre-emphasis

Note: Both pre-emphasis positions shown, as required by the PAA1382 specification. Remove pre-emphasis 2 for the MPT1327 specification requirement.

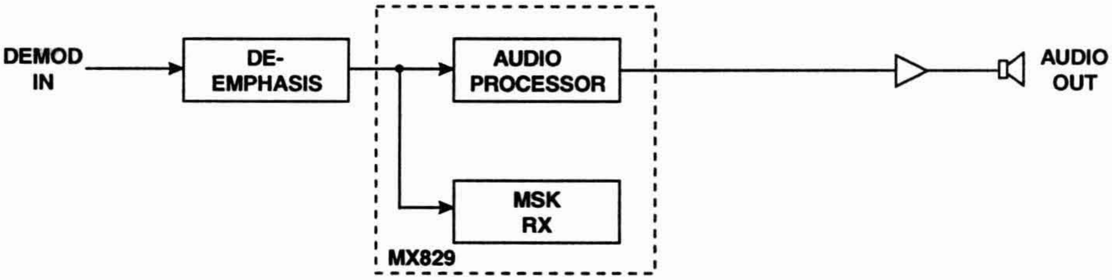

DEMOD IN
DE-EMPHASIS
AUDIO PROCESSOR
MSK RX
AUDIO OUT
MX829

Figure 8: PAA1382 Receiver De-emphasis

Note: De-emphasis shown in all paths, as required by the PAA1382 specification.

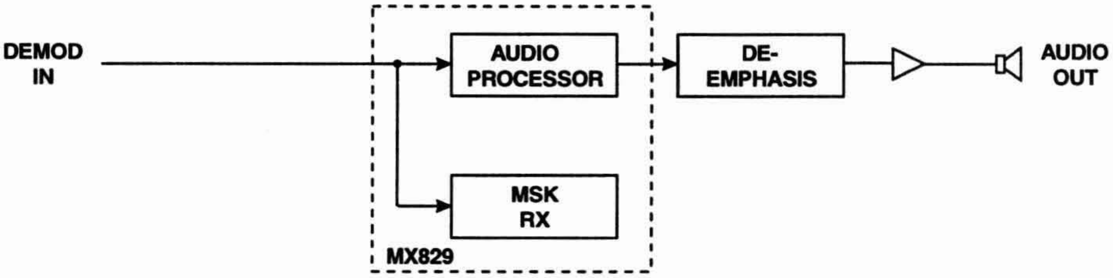

DEMOD IN
AUDIO PROCESSOR
MSK RX
DE-EMPHASIS
AUDIO OUT
MX829

Figure 9: MPT1327 Receiver De-emphasis

Note: De-emphasis shown in audio path only, as required by the MPT1327 specification.

6.1 Programming the MX829

The MX829 should be programmed in the following manner:

1. Perform a General Reset when first applying power to the MX829.
2. Program the MX829 configuration while in powersave.
   e.g. UK/F, MIC, B/W, 1200/2400, DTMF0-3, DTMFHI, DTMFLO, TXIDLEM, RXDATAM, TXDATAM, RX SYNC WORD PRIME, SYNT PRIME, SYNC PRIME, MOD1, MOD2, RX SYNC WORD and AUDIO ATTENUATOR.
3. Take the appropriate parts of the MX829 out of powersave by enabling:
   AMP1, AMP2, MOD1, MOD2, AUDIO and (DTMFEN or MSKTX or MSKRX).
4. In DTMF Tx mode, a DTMF tone will be generated for the duration that DTMFEN is set to "1".
5. In MSK Rx mode, wait for an interrupt ($\overline{\text{IRQ}}$ = "0") or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.
   A. If RXSYNCWORDF, SYNTF or SYNCF become set to "1", the corresponding synchronization word has been detected. This indicates the start of valid Rx data. The checksum calculation will be automatically reset. Note that the timing of RXDATAF will be re-aligned by the generation of a SYNC, SYNT or RX SYNC WORD interrupt.
   B. When RXDATAF subsequently becomes set to "1", read the Rx data from the RXDATA register. (Note that RXDATAF will be set every 8 bits regardless of whether valid Rx data is being received or not. Sync and checksum patterns should be considered for validating the data).
   C. If RXSUMF becomes set to "1", then all of the Rx data sent (starting after the synchronization word and terminating with a checksum) will have been correctly received. Note that it is necessary to know in advance what message length is expected, in order to determine at which point RXSUMF is valid (i.e. after the interrupt for the second checksum data byte being received has occurred). The RXSUMF bit is invalid at all other times. When RXSUMF becomes set to "1", the last two bytes of Rx data received will represent the two-byte checksum transmitted. The first checksum byte will already have been read from the RXDATA register, the last byte is available to be read, as the RXDATAF bit will also have been set to "1".
6. In MSK Tx mode, wait for an interrupt ($\overline{\text{IRQ}}$ = "0") or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.
   A. Do not send Tx data until the TXDATAF bit has been set to "1". When the TXDATAF bit is next set to "1", write the first byte of Tx data to the TXDATA register. If the transmit buffer is empty, this data will be transmitted immediately, causing the TXDATAF bit to be set to "1" approximately one MSK bit-period after the TXDATA register has been loaded with data. (Any TXIDLEF bit set upon entering MSK Tx mode should be ignored).
   B. The next byte of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to "1". Once this has been done, the TXDATAF bit will again be set to "1" eight MSK bit-periods after the TXDATA register was loaded with the second byte of data.
   C. Subsequent bytes of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to"1". After the last byte of Tx data has been loaded, the TXDATAF bit will be set after both 8 and 16 MSK bit-periods followed by the TXIDLEF bit which will be set approximately one MSK bit-period later, to indicate that the final bit has been transmitted.
   D. The TXDATAF bit will continue to be set every 8 MSK bit-periods, regardless of whether Tx data is written to the TXDATA register or not, providing the transmitter is enabled (MSK Tx mode = MSKTX bit set to "1"). Note that while the 2-byte checksum is being generated and transmitted, the TXDATAF bit will not be set for approximately 24 MSK bit-periods.

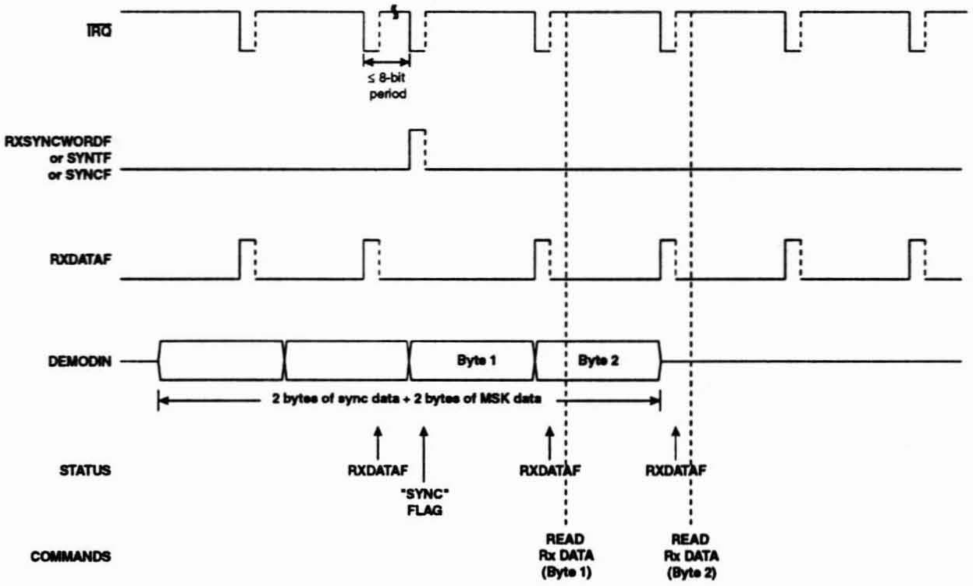

IRQ
≤ 8-bit period
RXSYNCWORDF or SYNTF or SYNCF
RXDATAF
DEMODIN
Byte 1
Byte 2
2 bytes of sync data + 2 bytes of MSK data
STATUS
RXDATAF
"SYNC" FLAG
RXDATAF
RXDATAF
COMMANDS
READ Rx DATA (Byte 1)
READ Rx DATA (Byte 2)

Figure 10: Reception of 2 Bytes of Data

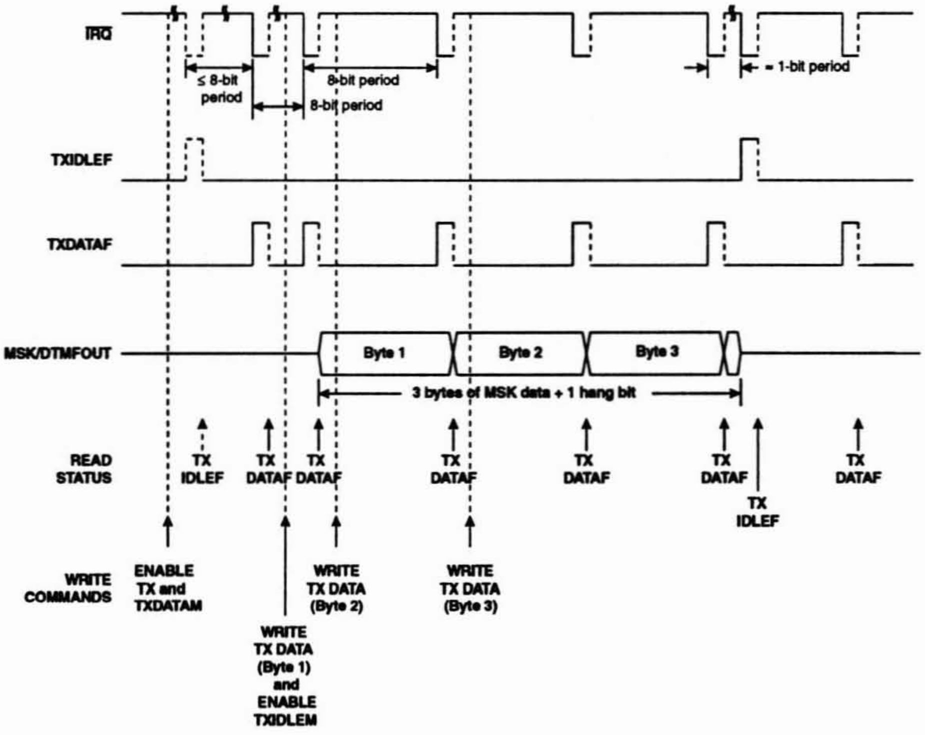

IRQ
≤ 8-bit period
8-bit period
8-bit period
= 1-bit period
TXIDLEF
TXDATAF
MSK/DTMFOUT
Byte 1
Byte 2
Byte 3
3 bytes of MSK data + 1 hang bit
READ STATUS
TX IDLEF
TX DATAF
TX DATAF
TX DATAF
TX DATAF
TX DATAF
TX IDLEF
TX DATAF
WRITE COMMANDS
ENABLE TX and TXDATAM
WRITE TX DATA (Byte 2)
WRITE TX DATA (Byte 3)
WRITE TX DATA (Byte 1) and ENABLE TXIDLEM

Figure 11: Transmission of 3 Bytes of Data

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, Bit Rate = 1.2k bits/sec, Noise Bandwidth = Bit Rate, Audio Level 0dB ref. = 308mVrms at 1kHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (Tx or Rx) (V_{DD} = 3.3V)	2		2.7	4.0	mA
I_{DD} (DTMF encode off for either Tx or Rx) (V_{DD} = 5.0V)	2		5.0	8.0	mA
I_{DD} (DTMF encode on for either Tx or Rx) (V_{DD} = 5.0V)	2			9	mA
I_{DD} (Powersaved) (V_{DD} = 3.3V)	2		0.3	1.0	mA
I_{DD} (Powersaved) (V_{DD} = 5.0V)	2		0.6	1.5	mA
"C-BUS" Interface					
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}
Input Leakage Current (logic "1" or "0")		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic "1" (I_{OH} = 120µA)		90%			V_{DD}
Output Logic "0" (I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current (V_{OUT} = V_{DD})	9			10	µA
AC Parameters					
Input Sensitivity (for 0dB output)					
Tx Audio Input (MIC)	8		308		mV_{RMS}
Rx Audio Input (DEMODFB)	8		308		mV_{RMS}
Output Drive Level					
For 60% Deviation	1, 6, 8	291	308	326	mV_{RMS}
For 100% Deviation	1, 6, 7, 8		1440		mV_{P-P}
Audio Filters					
Gain at 1kHz	5		0		dB
Passband Ripple	5	-2.0		0.5	dB
SINAD	5, 14		59		dBp
Signal Path Noise	5		-55		dB
Narrow Audio Bandwidth Setting					
Passband Frequencies	5	300		2550	Hz
Stopband Attenuation					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		5.5		dB
(f = 6000Hz)	5	10.5	24		dB
(f = 12500Hz)	5	25	49		dB
Wide Audio Bandwidth Setting					
Passband Frequencies	5	300		3000	Hz
Stopband Attenuation:					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		3.0		dB
(f = 6000Hz)	5	10.5	19		dB
(f = 25000Hz)	5	39.5	68		dB

	Notes	Min.	Typ.	Max.	Units
Amp 1 and Amp 2					
Open Loop Gain (INPUT = 1mV at 100Hz)			70		dB
Unity Gain Bandwidth			5.0		MHz
Input Impedance (at 100Hz)		10			MΩ
Output Impedance					
Open Loop			6.0		kΩ
Closed Loop			600		Ω
Distortion (DTMF)			2	5	%
MSK/DTMF TX OUT					
Tx output impedance (not powersaved)	3		1.0	2.5	kΩ
Tx output impedance (powersaved)	3	300	500		kΩ
Signal Level					
MSK	1	-1	0	1	dB
DTMF High Tone	1		2.0		dB
DTMF Low Tone	1		0		dB
Distortion (DTMF)			2	5	%
MSK TX OUT					
Isochronous Distortion:					
(1200Hz - 1800Hz)			25	40	μs
(1800Hz - 1200Hz)			25	40	μs
(1200Hz - 2400Hz)			20	30	μs
(2400Hz - 1200Hz)			20	30	μs
Third Harmonic Distortion			2	3	%
Deviation Limiter					
Threshold	1		1300		mV_{P-P}
Gain		-0.5		0.5	dB
Transmitter Modulator Drives					
Input Impedance (MOD1 IN, VOLUME IN at 100Hz)			15.0		kΩ
Mod.1 Attenuator					
Nominal Adjustment Range		0		12.0	dB
Attenuation Accuracy		-1.0		1.0	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance	3		600		Ω
Mod.2 Attenuator					
Nominal Adjustment Range		0		6.0	dB
Attenuation Accuracy		-0.6		0.6	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance	3		600		Ω
Audio Output Attenuator					
Nominal Adjustment Range		0		48.0	dB
Attenuation Accuracy		-1.5		1.5	dB
Step Size			1.6		dB
Output Impedance	3		600		Ω

	Notes	Min.	Typ.	Max.	Units
MSK Receiver					
Signal Input Dynamic Range (SNR = 50dB)	10, 11	100	230	1000	mV$_{RMS}$
Bit Error Rate					
SNR = 12dB at 1200 Baud	11		2.5		10^{-4}
SNR = 12dB at 2400 Baud	11		1.5		10^{-3}
SNR = 20dB at 1200/2400 Baud	11		1.0		10^{-8}
Receiver Synchronization (SNR = 12dB)	12				
Probability of Bit 16 being correct			0.995		%
Carrier Detect					
Sensitivity	12, 13			150	mV$_{RMS}$
Probability of Carrier Detection					
After Bit 16 (SNR = 12dB)			0.995		%
With 230mV$_{RMS}$ Noise (No Signal)			0.05		%
Miscellaneous Impedance					
FILTER OUT			600		Ω
Tx Audio Input (MIC) (at 100Hz)		10			MΩ
Xtal/Clock Input					
'High' pulse width	4	40			ns
'Low' pulse width	4	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (INPUT = 1mV$_{RMS}$ at 100Hz)		20			dB

Operating Characteristics Notes:

1. Signal levels are proportional to VDD.
2. Not including any current drawn from the modem pins by external circuitry.
   A. Powersaved = all functions disabled.
   B. Tx or Rx = device configured into any half-duplex operating mode.
3. Small signal impedance. A minimum load resistance of 6kΩ is suggested.
4. Timing for an external input to the XTAL/CLOCK pin.
5. Between MIC or AMP1 inputs to Modulator and Audio outputs, see Figure 12 and Figure 13.
6. It is recommended that these output levels are used to produce 60% cr 100% deviation in the transmitter.
7. With the Tx Audio input level 20dB above the level required to produce 0dB at the Output Drives.
8. With output gains set to 0dB.
9. $\overline{\text{IRQ}}$ pin.
10. See Figure 16 (variation of BER with Input Signal Level).
11. SNR = Signal to Noise Ratio in the Bit Rate Bandwidth.
12. For a "10101010101 ...01" pattern.
13. Measured with a 150mVRMS input signal (no noise).
14. dBp represents a psophometrically weighted measurement.

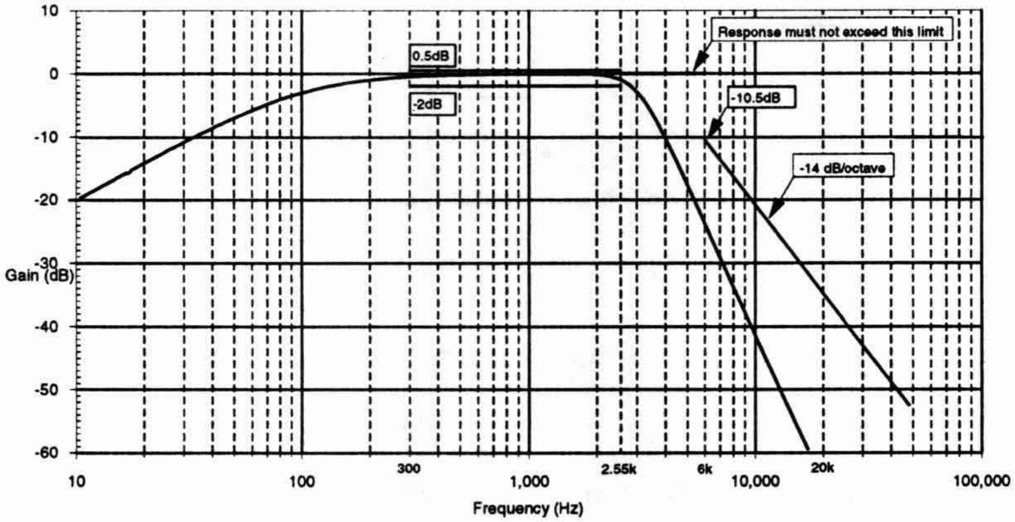


Figure 12: Overall Audio Frequency Response for 12.5kHz Channel Separation

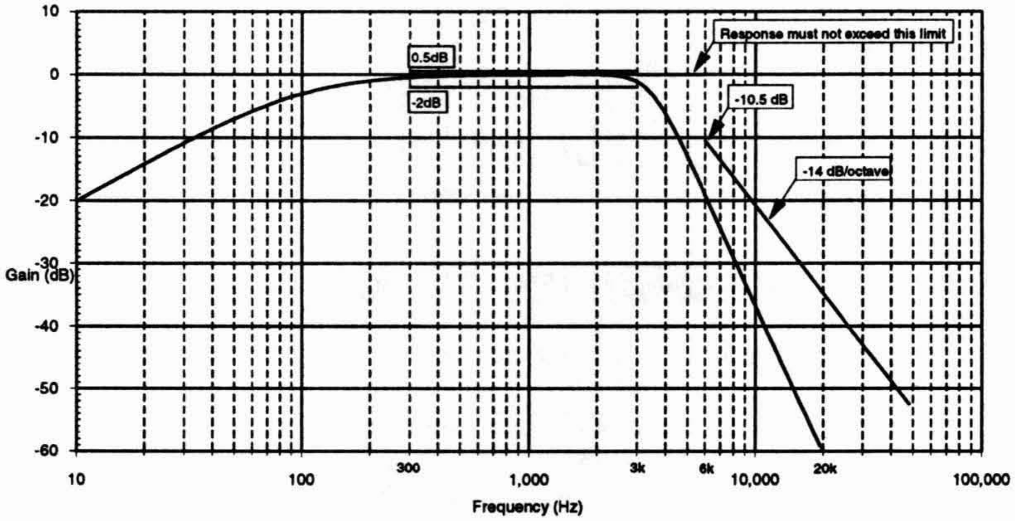


Figure 13: Overall Audio Frequency Response for 20kHz/25kHz Channel Separation

7.1.4 Timing

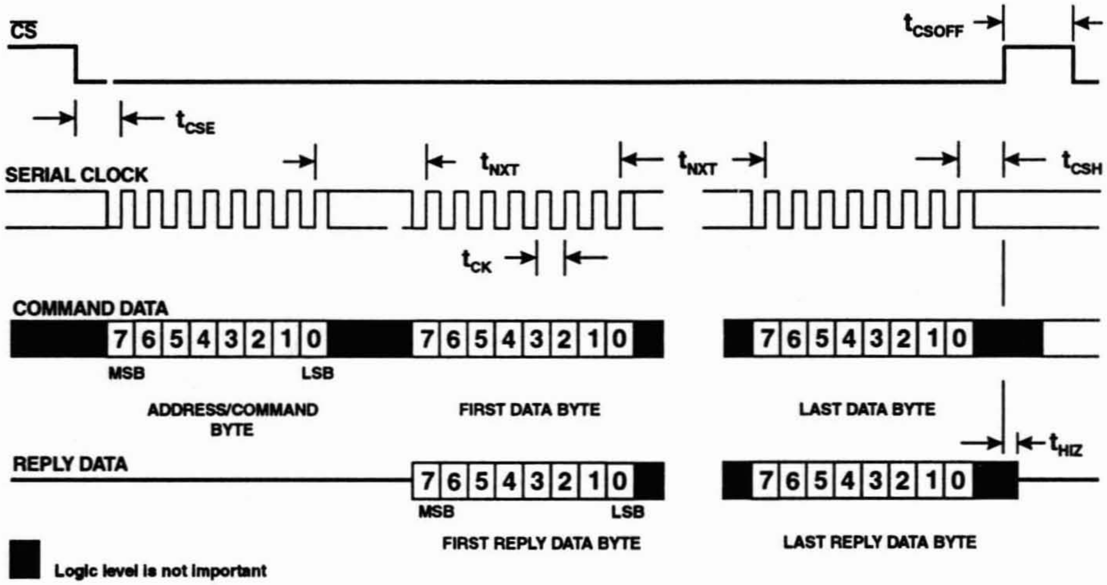
For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"		2.0			µs
t_{CSH}	Last "Clock-High to CS-High"		4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"				2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0			µs
t_{NXT}	"Inter-Byte" Time		4.0			µs
t_{CK}	"Clock-Cycle" time		2.0			µs

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. REPLY DATA is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.



CS
tCSOFF
tCSE
SERIAL CLOCK
tNXT
tNXT
tCSH
tCK
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
tHIZ
REPLY DATA
MSB
LSB
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
Logic level is not important

Figure 14: "C-BUS" Timing

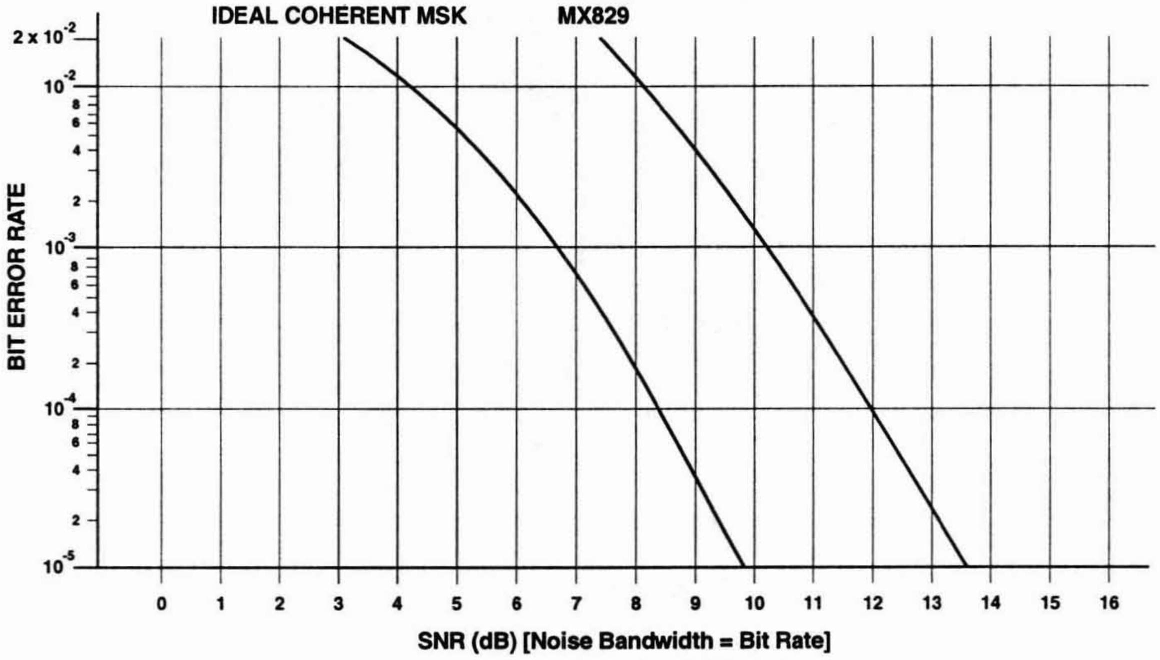


Figure 15: Bit Error Rate Graph

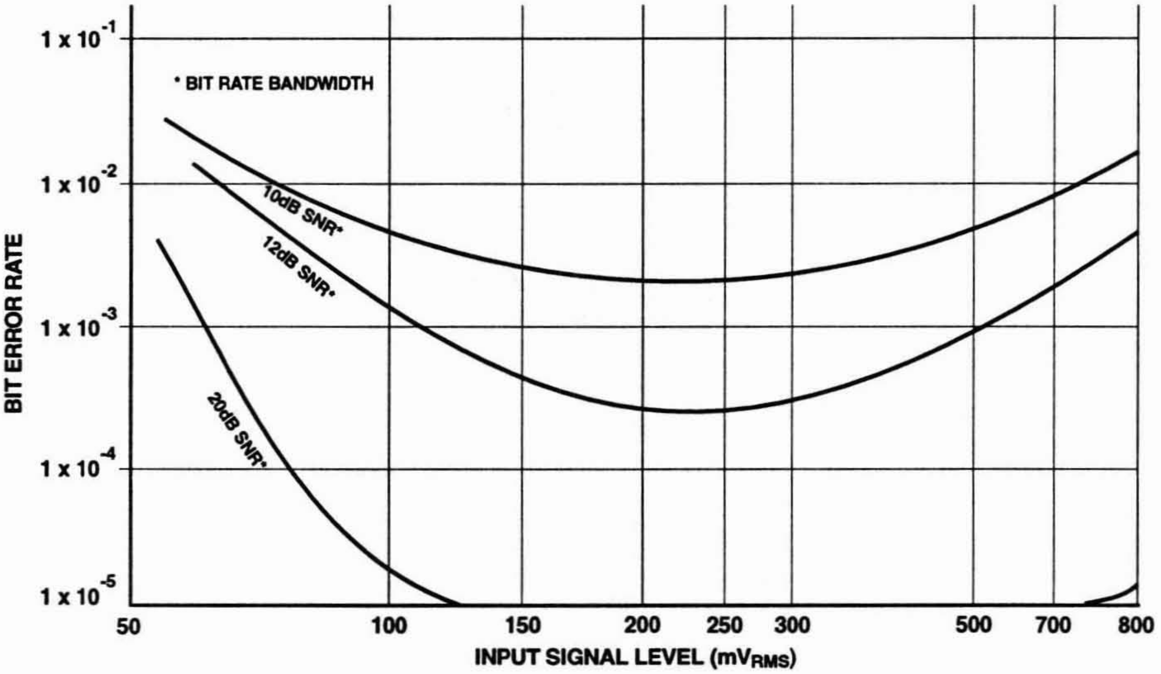
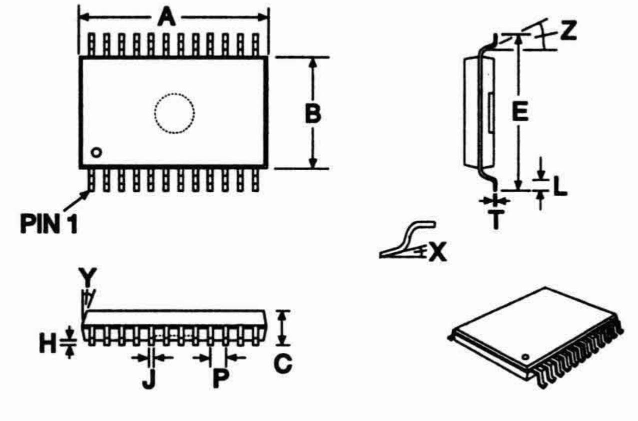


Figure 16: Typical Variation of Bit Error Rate with Input Signal Level

7.2 Packaging

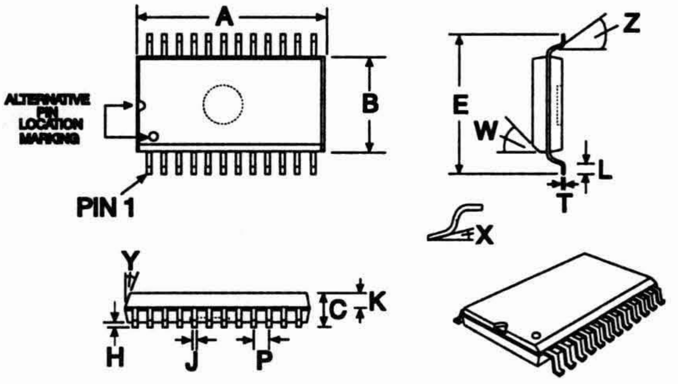


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin SSOP Mechanical Outline: ***Order as part no. MX829DS***

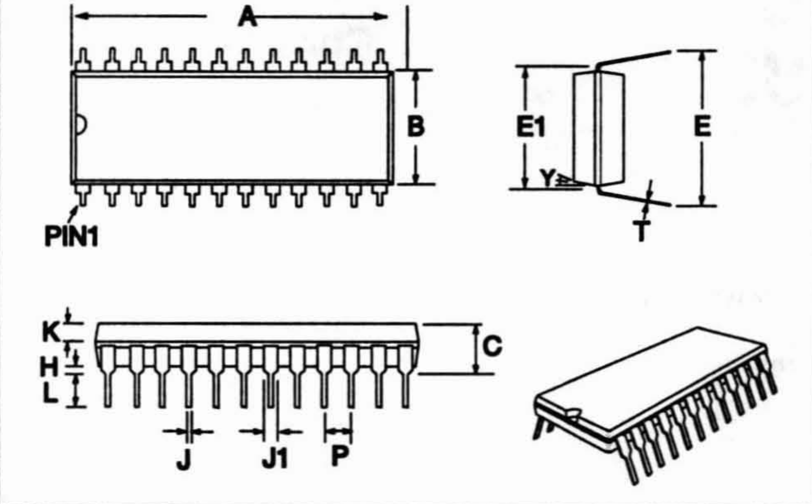


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 18: 24-pin SOIC Mechanical Outline: Order as part no. MX829DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 19: 24-pin PDIP Mechanical Outline: ***Order as part no. MX829P***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX839

Digitally Controlled Analog I/O Processor

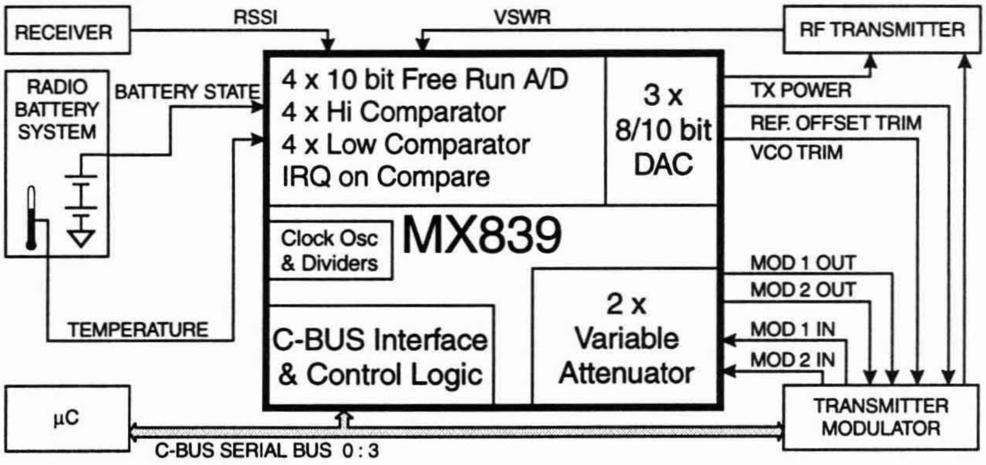
PRELIMINARY INFORMATION

Features

- 4 input intelligent 10 bit A/D monitoring subsystem
    - 4 High and 4 Low Comparators
    - External IRQ Generator
    - Free Running Operation
- Three 8/10 bit DACs
- Two Variable Attenuators
- Selectable A/D Clock Frequencies
- Full Control via 4-wire Serial Interface
- Low Power 3.0 Operation

Applications

- PCS, Cellular, LMR, Wireless Transceivers, and General Purpose
- Monitor and Control:
    - RSSI, Battery State, Temperature, VSWR, and Error Voltages
- Digital Trim and Calibration:
    - VCOs, TCXO, Power Output, Bias, Current, IF Gain, Deviation, Modulation Depth, and Baseband Gain


RECEIVER
RSSI
VSWR
RF TRANSMITTER
RADIO BATTERY SYSTEM
BATTERY STATE
4 x 10 bit Free Run A/D
4 x Hi Comparator
4 x Low Comparator
IRQ on Compare
3 x 8/10 bit DAC
TX POWER
REF. OFFSET TRIM
VCO TRIM
Clock Osc & Dividers
MX839
MOD 1 OUT
MOD 2 OUT
2 x Variable Attenuator
MOD 1 IN
MOD 2 IN
TEMPERATURE
C-BUS Interface & Control Logic
µC
TRANSMITTER MODULATOR
C-BUS SERIAL BUS 0 : 3

The MX839 is a low power CMOS µC peripheral device which provides digitally controlled calibration, trimming, and monitoring functions for PCS, cellular, LMR, wireless transceivers, and general purpose applications.

Featuring a four input intelligent 10 bit A/D monitoring subsystem, an interrupt generator, three 8/10 bit DACs, and two variable attenuator functions, the MX839 automatically monitors, produces, and trims up to nine analog signals via a simple four wire serial control bus. The free running A/D intelligent monitoring subsystem includes independent high and low limit comparators for each of four analog input signals which can be configured to generate external µC interrupts.

The MX839's high level of integration reduces end product parts count, component size, and software complexity. MX839 digital trimming functions also reduce manufacturing costs by eliminating manual trimming operations.

Featuring an operating range of 3.0V to 5.5V the MX839 is available in 24-pin SSOP (MX839DS), 24-pin SOIC (MX839DW), and 24-pin PDIP (MX839P) packages.

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

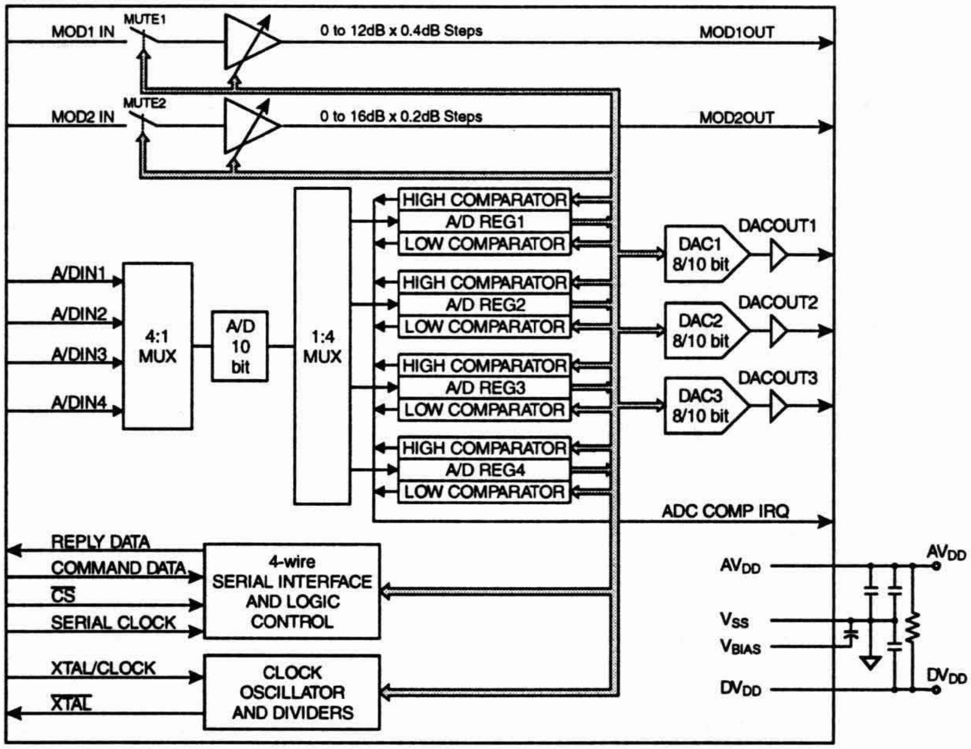

MOD1 IN
MUTE1
0 to 12dB x 0.4dB Steps
MOD1OUT
MOD2 IN
MUTE2
0 to 16dB x 0.2dB Steps
MOD2OUT
A/DIN1
A/DIN2
A/DIN3
A/DIN4
4:1 MUX
A/D 10 bit
1:4 MUX
HIGH COMPARATOR
A/D REG1
LOW COMPARATOR
HIGH COMPARATOR
A/D REG2
LOW COMPARATOR
HIGH COMPARATOR
A/D REG3
LOW COMPARATOR
HIGH COMPARATOR
A/D REG4
LOW COMPARATOR
DAC1 8/10 bit
DACOUT1
DAC2 8/10 bit
DACOUT2
DAC3 8/10 bit
DACOUT3
ADC COMP IRQ
REPLY DATA
COMMAND DATA
CS
SERIAL CLOCK
4-wire SERIAL INTERFACE AND LOGIC CONTROL
XTAL/CLOCK
XTAL
CLOCK OSCILLATOR AND DIVIDERS
AVDD
VSS
VBIAS
DVDD
AVDD
DVDD

Figure 1: Block Diagram

2 Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The output of the on-chip oscillator inverter.
2	XTAL/CLOCK	input	The input to the on-chip oscillator inverter, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The 'C-BUS' serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 5.
4	COMMAND DATA	input	The 'C-BUS' serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 5.
5	REPLY DATA	output	The 'C-BUS' serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 5.
6	$\overline{\text{CS}}$	input	The 'C-BUS' data loading control function. This input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Figure 5.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic '0'. This is a 'wire-ORable' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic '0' when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not disabled.
8	A/DIN1	input	Analog to digital converter input 1 (A/D1)
9	A/DIN2	input	Analog to digital converter input 2 (A/D2)
10	A/DIN3	input	Analog to digital converter input 3 (A/D3)
11	A/DIN4	input	Analog to digital converter input 4 (A/D4)
12	V_{SS}	power	Negative supply (ground) for both analog and digital supplies.
13	V_{BIAS}	output	An analog bias line for the internal circuitry, held at $AV_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	N/C		No internal connection. Do not make any connection to this pin.
15	DACOUT1	output	Digital to analog converter No. 1 output (DAC1)
16	DACOUT2	output	Digital to analog converter No. 2 output (DAC2)
17	DACOUT3	output	Digital to analog converter No. 3 output (DAC3)
18	N/C		No internal connection. Do not make any connection to this pin.
19	AV_{DD}	power	Positive analog supply. Analog levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.
20	MOD1 IN	input	Input to MOD1 variable attenuator.
21	MOD2 IN	input	Input to MOD2 variable attenuator.
22	MOD1	output	Output of MOD1 variable attenuator.
23	MOD2	output	Output of MOD2 variable attenuator.
24	DV_{DD}	power	Positive digital supply. Digital levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

3 External Components

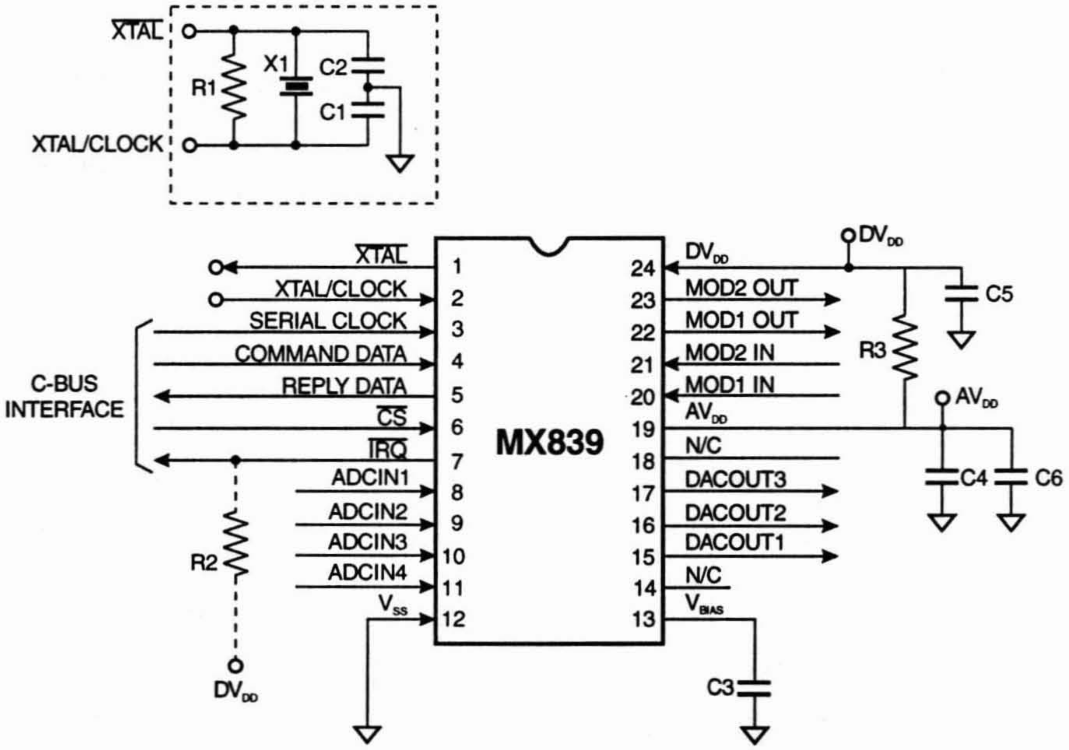

XTAL
XTAL/CLOCK
R1
X1
C2
C1
XTAL
XTAL/CLOCK
SERIAL CLOCK
COMMAND DATA
REPLY DATA
CS
IRQ
C-BUS INTERFACE
ADCIN1
ADCIN2
ADCIN3
ADCIN4
V_{SS}
R2
DV_{DD}
1
2
3
4
5
6
7
8
9
10
11
12
MX839
24
23
22
21
20
19
18
17
16
15
14
13
DV_{DD}
MOD2 OUT
MOD1 OUT
MOD2 IN
MOD1 IN
AV_{DD}
N/C
DACOUT3
DACOUT2
DACOUT1
N/C
V_{BIAS}
C3
DV_{DD}
C5
R3
AV_{DD}
C4
C6

Figure 2: Recommended External Components

R1		1MΩ	±5%
R2		22kΩ	±10%
R3	Note 1	10Ω	±10%
C1		22pF	±20%
C2		22pF	±20%
C3		0.1µF	±20%

C4	Note 1	0.1µF	±20%
C5		0.1µF	±20%
C6	Note 1	10.0µF	±20%
X1	Note 2, 3		±100ppm

Table 1: Recommended External Components

Notes:

1. These values should be determined in regard to the amount of supply filtering required for D/A outputs.
2. If an external clock is to be used, then it should be connected to Pin 2 and the components C1, C2, R1, and X1 omitted. The ADC clock frequency is derived from the crystal or external clock by means of internal programmable dividers. See Section 6 for details of crystal or external clock frequency range.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4 General Description

The device comprises four groups of related functions: variable attenuators, digital to analog converters, a multiplexed analog to digital converter with multiplexer, clock generator and four 8-bit magnitude comparators with variable reference levels. These functions are all controlled by the 'C-BUS' serial interface and are described below:

4.1 Variable Attenuators

The two variable attenuators have a range of 0 to -12dB and 0 to -6dB respectively and may be controlled independently.

4.2 Digital to Analog Converters

Three DACs are provided with default resolutions of 8 bits, which are defined at the initial chip reset. In this mode the 'C-BUS' data is transferred in a single byte. An option is provided to define any one or more of the DAC resolutions to be 10 bits, then the DAC requires the transfer of two 'C-BUS' data bytes.

The upper and lower DAC reference voltages are defined internally as AV_{DD} and V_{SS} respectively. The output voltage is expressed as:

$$V_{OUT} = AV_{DD} \times (DATA / 2^n) \quad \text{[Volts]}$$

Where, n is the DAC resolution (8 or 10 bits) and DATA is the decimal value of the input code. For example: n = 8 and binary code = 11111111 therefore DATA = 255

$$V_{OUT} = AV_{DD} \times (255 / 256) \quad \text{[Volts]}$$

Any one of the three DAC input latches might be loaded by sending an address/command byte followed by one or two data bytes to the 'C-BUS' interface. The data is then latched and the static voltage is updated at the appropriate output.

When a DAC is disabled, its output is defined as open-circuit.

4.3 Analog to Digital Converter and A/D Clock Generator

A single successive approximation A/D is provided with four multiplexed inputs. After a general reset command $01, the A/D converter subsystem is disabled. To start conversions the Clock Control ($D0) and A/D control ($D7) registers must be written (refer to Tables 2,6, and 8). Please note that A/D channel 1 must be active for any other channel to work. Also note that A/D control register bit 5 ($\overline{\text{READ}}$) should be set low prior to issuing a 'READ A/D DATA x' command to disable conversions so the data being read does not change during the read which could otherwise result in erroneous data being read. To re-enable conversions the A/D control register bit 5 ($\overline{\text{READ}}$) bit must be set back high.

The internal A/D clock frequency (f_{A/D_CLK}) is generated with a programmable clock generator. Users have flexible control of this clock signal via the Clock Control Register ($D0), DIVIDER set per Table 6, and the choice of an external system clock signal or a dedicated crystal. f_{A/D_CLK} should be chosen not to exceed 1MHz.

Since the typical application is for monitoring slowly changing control voltages, a Sample and Hold circuit is not included at the input of the A/D. Thus, for the analog to digital conversion to be accurate, the input signal should not change significantly during the conversion time. For 'n-bit' accuracy (with a maximum error of 1LSB) the maximum signal 'linear rate of change,' 'S,' is defined by:

$$S = \frac{AV_{DD} \quad f_{A/D\_CLK}}{2^n \quad 1000 \quad (n+2)} \qquad \text{[mV/}\mu\text{S]}$$

where: n is the number of bits of accuracy with a maximum error of 1 LSB

where: $f_{A/D\_CLK} = \frac{f_{XTAL}}{DIVIDER}$, DIVIDER is selected per Table 6.

For Example: The most significant bits (n) of accuracy.

For (n = 6) bit accuracy with AV_{DD}=5V and f_{A/D_CLK} = 1MHz

$S = 9.77$ [mV/µS]

For (n = 8) bit accuracy with AV_{DD}=5V and f_{A/D_CLK} = 1MHz

$S = 1.95$ [mV/µS]

For (n = 10) bit accuracy with AV_{DD}=3.3V and f_{A/D_CLK} = 1MHz

$S = 0.27$ [mV/µS]

The input signal should therefore be band limited to ensure the maximum signal 'linear rate of change' is not exceeded for the desired accuracy.

After enabling conversions the user must allow time for all enabled channels to be digitized before reading the results via the 'C-BUS'. The minimum required time to wait is:

$$T_{\text{CONV\_MAX}} = \frac{(10+2)\quad \text{'Number of Enabled Inputs'}}{f_{\text{A/D\_CLK}}} \qquad \text{[Seconds]}$$

Upon disabling conversions the data for the most recent conversion completed for each channel will be available via the 'C-BUS' commands 'READ A/D DATA x' (addresses $DC, $DD, $DE, $DF) for input channels 1 through 4 respectively.

Do not forget to re-enable conversions by setting A/D control register bit 5, the $\overline{\text{READ}}$ bit, back high after reading the desired A/D results. Note that the Magnitude Comparators (see section 4.4) can be configured to monitor the A/D channel data in order to minimize the software burden of continuously reading the A/D channel data. It is not recommended to issue 'READ A/D DATA x' commands without first setting A/D control register bit 5, the $\overline{\text{READ}}$ bit, low.

An Example C-BUS transaction to do a conversion and read of A/D Channel 1:

HEX ADDRESS/ COMMAND	WRITE DATA BYTE 1	READ DATA BYTE 1	READ DATA BYTE 2	COMMENT
$01	N/A	N/A	N/A	Reset Device
$D0	$03	N/A	N/A	Set $f_{\text{A/D\_CLK}}$ DIVIDER = 4
$D7	$70	N/A	N/A	Enable conversion on A/D Channel 1
$D7	$50	N/A	N/A	Disable conversions after waiting $T_{\text{CONV\_MAX}}$
$DC	N/A	xxxxxxxx	000000xx	Read A/D Channel 1 Data
$D7	$70	N/A	N/A	Re-enable conversion on A/D Channel 1

4.4 Magnitude Comparators and Interrupt Request

High and low digital comparator reference levels are provided for the four digital magnitude comparators via the 'C-BUS' interface. The digital input to the comparators is provided by the most significant 8 data bits of each A/D channel

When the sampled data falls outside the high or low digital comparator reference levels the status register is updated and the $\overline{\text{IRQ}}$ pin is pulled low. When a reference level is set to '0', its IRQ is disabled.

4.5 Software Description

4.5.1 Address/Commands

Instructions and Data are transferred via the 'C-BUS' in accordance with the timing information provided in Figure 5.

Instruction and data transactions to and from the FX839 consist of an Address/Command byte followed by either:

(i) a control or DAC data write (1 or 2 bytes) or,

(ii) a status or A/D data read (1 or 2 bytes)

4.5.2 Write Only Register (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$D0	CLOCK CONTROL	0	0	0	0	0	DIVIDER		
							BIT 2	BIT 1	BIT 0
$D2	VARIABLE ATTENUATOR (1)	0	0	MOD1 ENABLE	MOD1				
					BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	VARIABLE ATTENUATOR (2)	0	0	MOD2 ENABLE	MOD2				
					BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$D3	DAC CONTROL	NBIT DAC1	NBIT DAC2	NBIT DAC3	0	DAC1 ENABLE	DAC2 ENABLE	DAC3 ENABLE	0
$D4	DAC1 DATA (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$D5	DAC2 DATA (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$D6	DAC3 DATA (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$D7	A/D CONTROL	0	1	$\overline{\text{READ}}$	A/DIN1 ACTIVE	A/DIN2 ACTIVE	A/DIN3 ACTIVE	A/DIN4 ACTIVE	0
$D8	MAG COMP ONE LEVELS (1)	MAGNITUDE COMPARATOR UPPER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP ONE LEVELS (2)	MAGNITUDE COMPARATOR LOWER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$D9	MAG COMP TWO LEVELS (1)	MAGNITUDE COMPARATOR UPPER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP TWO LEVELS (2)	MAGNITUDE COMPARATOR LOWER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$DA	MAG COMP THREE LEVELS (1)	MAGNITUDE COMPARATOR UPPER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP THREE LEVELS (2)	MAGNITUDE COMPARATOR LOWER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$DB	MAG COMP FOUR LEVELS (1)	MAGNITUDE COMPARATOR UPPER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP FOUR LEVELS (2)	MAGNITUDE COMPARATOR LOWER LEVEL							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Table 2: Write Only Register (8-Bit and 16-Bit)

Note

1. A second byte is expected by the 'C-BUS' interface only when the 'NBIT DAC*n*' bit of the 'DAC Control Register' is set high. Otherwise, the data transfer is a single byte (Bit 7 to Bit 0).

4.6 Read Only Registers (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$D1	IRQ FLAGS	HIRQF 4	LIRQF 4	HIRQF 3	LIRQF 3	HIRQF 2	LIRQF 2	HIRQF 1	LIRQF 1
$DC	A/D DATA1 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DD	A/D DATA2 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DE	A/D DATA3 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DF	A/D DATA4 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8

Table 3: Read Only Registers (8-Bit and 16-Bit)

4.7 Write Only Register Description

4.7.1 RESET Register (Hex Address $01)

The reset command has no data attached to it. It sets the device registers into the specific states listed below:

REGISTER NAME		BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
CLOCK CONTROL		0	0	0	0	0	0	0	0
DAC CONTROL		0	0	0	0	0	0	0	0
DAC1 DATA[1]		0	0	0	0	0	0	0	0
DAC2 DATA[1]		0	0	0	0	0	0	0	0
DAC3 DATA[1]		0	0	0	0	0	0	0	0
A/D CONTROL		0	0	0	0	0	0	0	0
VARIABLE ATTENUATOR	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP ONE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP TWO LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP THREE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP FOUR LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0

Table 4: RESET Register (Hex Address $01)

Note

1. Default resolution is defined as 8-Bits.

4.7.2 CLOCK CONTROL Register (Hex Address $D0)

This register controls the A/D clock divide ratio:

Bits 7 to 3	Reserved for future use. These bits should be set to '0'.
DIVIDER (Bit 2 - Bit 0)	The Xtal input clock divide ratio, which sets the A/D sample clock frequency, is defined in the following table.

Table 5: CLOCK CONTROL Register (Hex Address $D0)

Bit 2	Bit 1	Bit 0	Function
0	0	0	Powersave
0	0	1	÷1
0	1	0	÷2
0	1	1	÷4
1	0	0	÷8
1	0	1	÷16
1	1	0	÷32
1	1	1	÷64

Table 6: DIVIDER (Bit 2 - Bit 0)

4.7.3 VARIABLE ATTENUATOR Register (Hex address $D2)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to enable and set the attenuation of the Modulator 1 amplifier. Bits 0 - 5 of the second byte in this register are used to enable and set the attenuation of the Modulator 2 amplifier. See Table 7.

5	4	3	2	1	0	Mod. 1 Attenuation	5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})	0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB	1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB	1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	11.6dB	1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	11.2dB	1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	10.8dB	1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	10.4dB	1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	10.0dB	1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	9.6dB	1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	9.2dB	1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	8.8dB	1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	8.4dB	1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	8.0dB	1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	7.6dB	1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	7.2dB	1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	6.8dB	1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	6.4dB	1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	6.0dB	1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	5.6dB	1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	5.2dB	1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	4.8dB	1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	4.4dB	1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	4.0dB	1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	3.6dB	1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	3.2dB	1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	2.8dB	1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	2.4dB	1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	2.0dB	1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	1.6dB	1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	1.2dB	1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.8dB	1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.4dB	1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB	1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is '1' the MOD1 attenuator is enabled. When this bit is '0' the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is '1' the MOD2 attenuator is enabled. When this bit is '0' the MOD2 attenuator is disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to '0'.

Table 7: VARIABLE ATTENUATOR Register (Hex address $D2)

4.7.4 DAC CONTROL Register (Hex address $D3)

This register controls the resolution and the number of enabled DAC outputs:

NBIT DAC1 (Bit 7) **NBIT DAC2 (Bit 6)** **NBIT DAC3 (Bit 5)**	These bits define the input resolutions for each of the four DACs. When 'NBIT DAC*n*' is '0' the resolution of DAC*n* is 8-Bits. When 'NBIT DAC*n* is '1' the resolution of DAC*n* is 10-Bits.
(Bit 4)	Reserved for future use. This bit should be set to '0'.
DAC1 ENABLE (Bit 3) **DAC2 ENABLE (Bit 2)** **DAC3 ENABLE (Bit 1)**	These bits allow any one or more of the three DACs to be powered up. When '0' the DAC*n* is powered down and the output is high impedance. When '1' the DAC is powered on and the output voltage is defined by the DAC Data Registers.
(Bit 0)	Reserved for future use. This bit should be set to '0'.

4.7.5 DAC1 DATA Register (Hex Address $D4)

4.7.6 DAC2 DATA Register (Hex Address $D5)

4.7.7 DAC3 DATA Register (Hex Address $D6)

The data in these three registers sets the analog voltage at the output of DAC1, DAC2 and DAC3. This data will consist of one or two bytes depending on the defined input resolution that is set by bits 7, 6 and 5 of the DAC Control Register. When operating with 10-bit resolution Bit 7 to Bit 2 of the DAC*n* DATA Register second data byte must be set to "0".

4.7.8 A/D CONTROL Register (Hex Address $D7)

This register sets which channels are active and enables conversion mode or read mode.

(Bit 7)	Reserved for future use. This bit should be set to '0'.
(Bit 6)	Reserved for future use. This bit should be set to '1'.
$\overline{\text{READ}}$ **(Bit 5)**	When this bit is set to '1' all active channels are continuously sampled and the latest converted data stored for each channel. When this bit is set to '0' all conversions are stopped so that they may be read.
A/D1 ACTIVE (Bit 4) **A/D2 ACTIVE (Bit 3)** **A/D3 ACTIVE (Bit 2)** **A/D4 ACTIVE (Bit 1)**	These bits allow any one or more of the four A/D input channels to be enabled. When '0' the A/DIN*n* input voltage is not converted. When '1' the A/DIN*n* input is defined as active and the input voltage is converted. A/D1 must be active for any other channel to be active.
(Bit 0)	Reserved for future use. This bit should be set to '0'.

Table 8: A/D CONTROL Register (Hex Address $D7)

4.7.9 MAG COMP ONE LEVELS (Hex Address $D8)

4.7.10 MAG COMP TWO LEVELS (Hex Address $D9)

4.7.11 MAG COMP THREE LEVELS (Hex Address $DA)

4.7.12 MAG COMP FOUR LEVELS (Hex Address $DB)

Each address controls the relevant numbered A/D magnitude comparator.

The first byte, transmitted with the most significant bit first, sets the magnitude comparator upper reference level and the second byte sets the magnitude comparator lower reference level.

When a reference level's value is set to '0' its IRQ is disabled.

In general, if a reference level's value is R (unsigned decimal value of data byte)

$$V_{REF} = AV_{DD} \times \frac{R}{256} \quad \text{[Volts]}$$

4.8 Read Only Register Description

4.8.1 IRQ FLAGS Register (Hex Address $D1)

HIRQF1 (Bit 1) **HIRQF2 (Bit 3)** **HIRQF3 (Bit 5)** **HIRQF4 (Bit 7)**	These bits are set if the relevant digital magnitude comparator input exceeds its upper reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.
LIRQF1 (Bit 0) **LIRQF2 (Bit 2)** **LIRQF3 (Bit 4)** **LIRQF4 (Bit 6)**	These bits are set if the relevant digital magnitude comparator input falls below its lower reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.

Table 9: IRQ FLAGS Register (Hex Address $D1)

4.8.2 A/D DATA1 Register (Hex Address $DC)

4.8.3 A/D DATA2 Register (Hex Address $DD)

4.8.4 A/D DATA3 Register (Hex Address $DE)

4.8.5 A/D DATA4 Register (Hex Address $DF)

This data will consist of two bytes each. Bit 7 to Bit 2 of the second data byte will be set to '0'. Bits 0-7 of the first byte are the lease significant 8 bits while Bits 0-1 of the second byte are the most significant 2 bits of the 10 bit conversion.

The analog input (V_{IN}) is converted to a 10-bit digital word (w) according to:

$$w = \frac{V_{IN}}{AV_{DD}} \times 1024$$

The bits of word (w) are returned in 2 bytes as follows:

	7	6	5	4	3	2	1	0
Return Byte 1	w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0
Return Byte 2	0	0	0	0	0	0	w_9	w_8

5 Application

5.1 C-Bus Clock

Although this is specified as a 500kHz clock for compatibility with other C-BUS devices, the MX839 C-BUS will operate over a much wider range. Users should ensure that the C-BUS clock is at least 4 times slower than the crystal or external clock on Pin 2 of the MX839.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})		-0.3	7.0	V
Voltage on any pin to V_{SS}		-0.3	V_{DD} + 0.3	V
Current				
AV_{DD}		-30	30	mA
DV_{DD}		-30	30	mA
V_{SS}		-30	30	mA
Any other pin		-20	20	mA
AV_{DD} - DV_{DD}	Note 1, 2	-100	100	mV
DW / P Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			800	mW
Derating above 25°C			13	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C
DS Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C

Note:

1. It is recommended that AV_{DD} be connected to DV_{DD} through a filter.
2. It is also recommended that AV_{DD} and DV_{DD} Voltages be tightly AC coupled to V_{SS} with a capacitor.

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})	3.0	5.5	V
Operating Temperature	-40	85	°C
Xtal Frequency	0.5	6.0	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
$AV_{DD} = DV_{DD} = V_{DD}$ = 3.3V to 5.0V, T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
Supply Voltage		3.0	5.0	5.5	V
Supply Difference ($AV_{DD} - DV_{DD}$)		-100		100	mV
I_{DD}					
V_{DD} = 5V					
powersaved			250	400	µA
not powersaved			4.5	7.0	mA
V_{DD} = 3.3V					
powersaved			150	250	µA
not powersaved			2.5	4.0	mA
'C-BUS' Interface					
Input Logic '1'		70%			DV_{DD}
Input Logic '0'				30%	DV_{DD}
Input Leakage Current (Logic '1' and '0')		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic '1' (I_{OH} = 120µA)		90%			DV_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	DV_{DD}
DACs and Output Buffers (Guaranteed monotonic)					
Un-loaded Performance					
Resolution			8 or 10		Bits
Internal DAC Settling Time (to 0.5 lsb)				10.0	µs
Integral non-linearity Figure 4	7				
8 Bit mode				3.0	LSBs
10 Bit mode				5.0	LSBs
Differential non-linearity Figure 3	6				
8 Bit mode				1.0	LSBs
10 Bit mode				1.0	LSBs
Buffer Slew Rate (with 20pF load)				TBD	V/µs
Buffer Output Resistance				200	Ω
Zero Error (For 0000_{HEX} code input)		-20	0	20	mV
RMS Output Noise Voltage	1		10		µV
Loaded Performance	2				
Output voltage with 5kΩ resistive load to ground					
Digital code = $3FF_{HEX}$	3	4.79			V
Digital code = 200_{HEX}, 10 Bit	3		2.495		V
Digital code = 80_{HEX}, 8 Bit	3		2.495		V
Output voltage with 5kΩ resistive load to V_{DD}					
Digital code = 000_{HEX}	3			200	mV
Minimum Resistive Load	4	1.0			kΩ

		Notes	Min.	Typ.	Max.	Units
A/Ds and Multiplexed Inputs (Guaranteed monotonic)						
Resolution				10		Bits
Input signal 'linear rate of change' V_{DD} = 3.3V, and f_{A/D_CLK} = 1MHz	For 1 Bit error				0.27	mV/µs
Conversion Time	f_{A/D_CLK} = 1MHz			12		µs
Integral non-linearity	Figure 4	7			2.0	LSBs
Differential non-linearity	Figure 3	6			1.0	
Zero error			-20		20	mV
A/D Clock Frequency (f_{A/D_CLK})				1.0	TBD	MHz
Input Capacitance				TBD		pF
Variable Attenuators						
Nominal Adjustment Range						
MOD1 Attenuator			0		12.0	dB
MOD2 Attenuator			0		6.0	dB
Attenuation Accuracy			-1.0		1.0	dB
Step Size						
MOD1			0.2	0.4	0.6	dB
MOD2			0.1	0.2	0.3	dB
Output Impedance		5		600		Ω
Bandwidth (-3dB)				100		kHz
Input Impedance				15		kΩ
Magnitude Comparators and Interrupt Request						
Resolution				8		Bits
Output Logic '0' at $\overline{IRQ}$ (I_{OL}= 360µA and pull-up resistor R2 = 22kΩ ± 10% to DV_{DD})					10%	DV_{DD}
'Off' State Leakage Current at $\overline{IRQ}$	$V_{OUT} = DV_{DD}$				10	µA
Xtal/Clock Input						
Frequency Range		8	0.5		6.0	MHz
'High' pulse width			40			ns
'Low' pulse width			40			ns
Input Impedance (at 100Hz)				10		MΩ
Gain (input = 1mV_{RMS} at 100Hz)				20		dB

Operating Characteristics Notes:

1. Measured over a 0 to 30kHz Band.
2. The extremes of the DAC output range (when resistively loaded) is affected by the output impedance of the DAC buffer. Under these conditions, the output impedance can approach 200Ω. However; when the output is operating well within the supply; the output impedance will be significantly lower, thereby improving the loaded performance.
3. $R_{LOAD} = 5k\Omega$ $AV_{DD} = 5.0V$.
4. Loads less than 1kΩ will produce output distortion.
5. Small signal impedance, at $AV_{DD} = 5V$ and $T_{AMB} = 25°C$.
6. Differential non-linearity is defined as the difference in width between adjacent code midpoints and the width of an ideal LSB, divided by the width of an ideal LSB. See Figure 3.
7. Integral non-linearity is defined as the width difference between an actual code midpoint and the line of best fit through all code midpoints, divided by the width of an ideal LSB. See Figure 4.
8. 6MHz operation at $V_{DD} = 5.0V$ only. The 'C-BUS' clock must be at lest 4 times slower than the XTAL/CLOCK frequency.

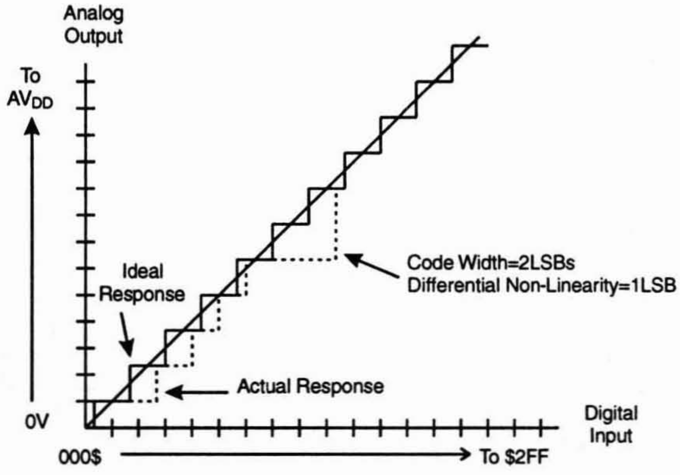


Figure 3: Differential Non-Linearity of a D/A Converter

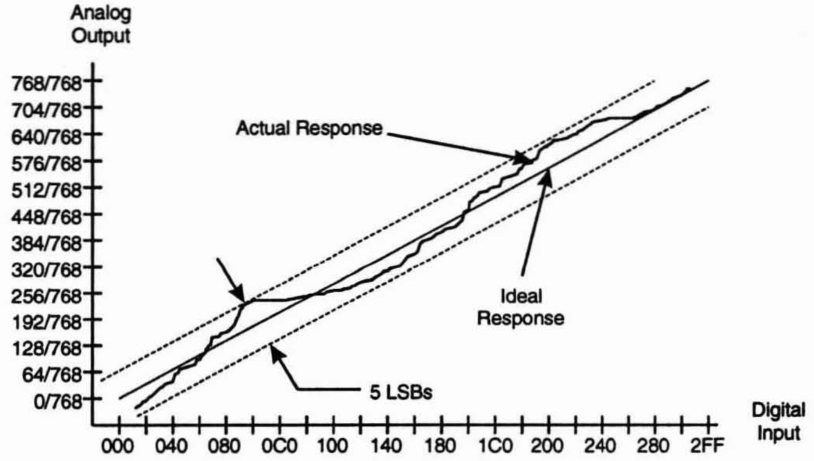


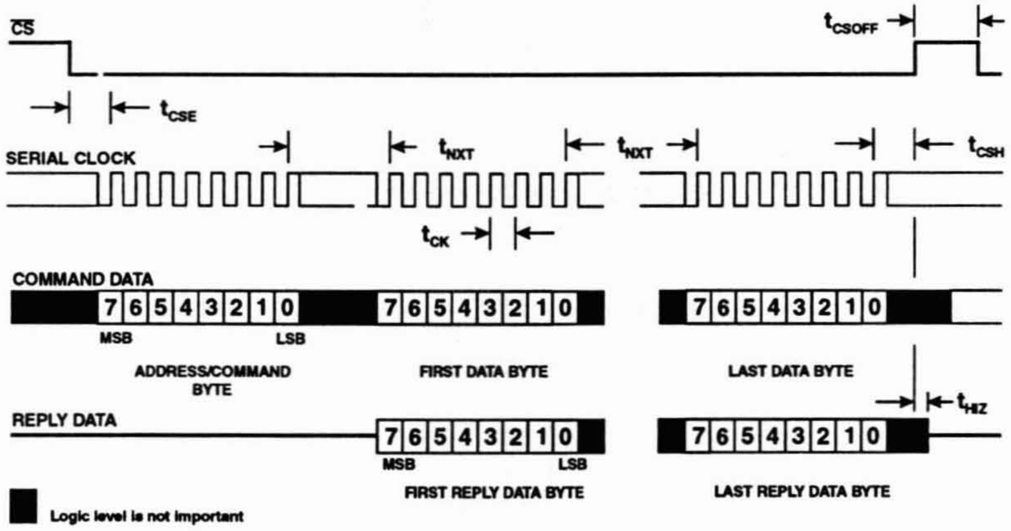
Figure 4: Integral Non-Linearity of a D/A Converter

6.1.4 Timing

For the following conditions unless otherwise specified:

DV_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs



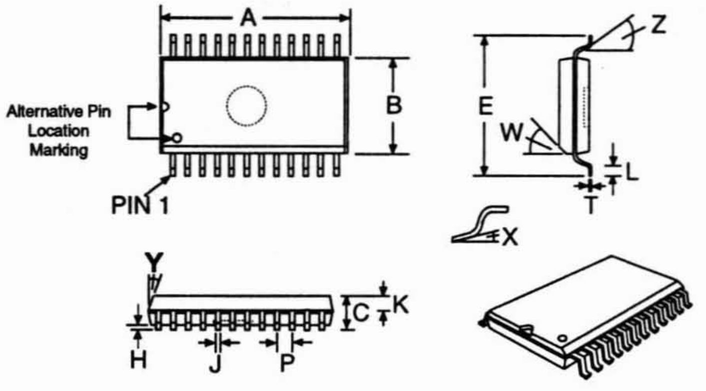
CS
tCSOFF
tCSE
SERIAL CLOCK
tNXT
tNXT
tCSH
tCK
COMMAND DATA
7 6 5 4 3 2 1 0
MSB
LSB
ADDRESS/COMMAND BYTE
FIRST DATA BYTE
LAST DATA BYTE
REPLY DATA
tHIZ
FIRST REPLY DATA BYTE
LAST REPLY DATA BYTE
Logic level is not important

Figure 5: 'C-BUS' Timing

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats 'C-BUS' compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

6.2 Packaging

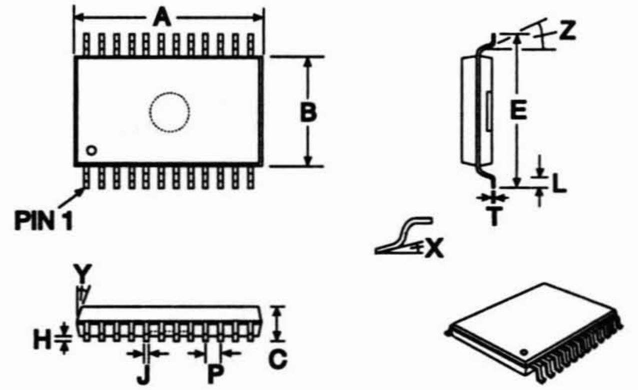


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SOIC Mechanical Outline: ***Order as part no. MX839DW***

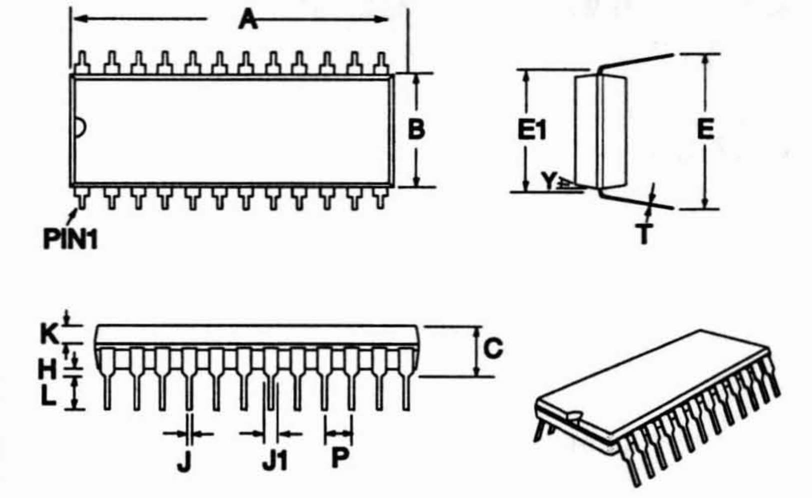


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin SSOP Mechanical Outline: ***Order as part no. MX839DS***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PDIP Mechanical Outline: ***Order as part no. MX839P***

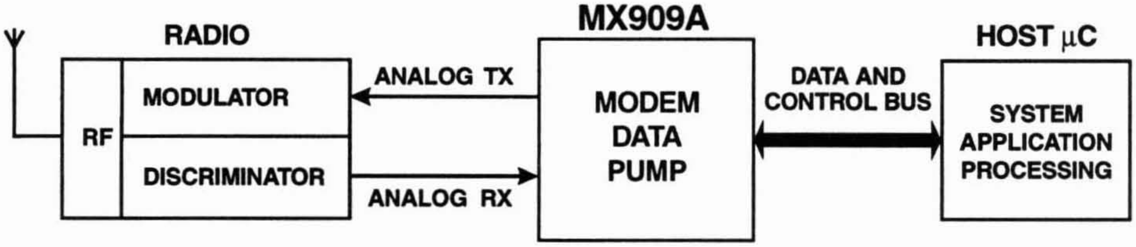
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX909A GMSK MODEM DATA PUMP

PRELIMINARY INFORMATION

- **GMSK Modulation**
- **RX or TX up to 19.2k bits/sec**
- **Full Data Packet Framing**
- **Mobitex™ Compatible**
- **Flexible Operating Modes**
- **Host µC Interface**
- **Low Power 3.3V/5.0V Operation**
- **24-Pin Small Form Package Option**



The MX909A is a low power CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance GMSK Wireless Packet Data Modem. The MX909A interfaces with a host µC and radio modulation/demodulation circuits to deliver reliable two-way transfer of application data over a wireless link.

The MX909A assembles application data received from the host µC, adds forward error correction (FEC), and error detection (CRC) codes, time-spreads this data by interleaving (burst-error protection) and scrambles (randomizes) the bit pattern. After automatically adding bit and frame sync codewords, the data packet is converted into analog GMSK signals for modulating into the radio transmitter.

In the receive mode, the MX909A performs the reverse function using the analog signals from the receivers discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host µC. Any CRC detected residual uncorrected errors in the data will be flagged. Readout of the SNR value during receipt of a packet is also provided.

The MX909A uses data block sizes and FEC/CRC algorithms compatible with the Mobitex™ Wide Area Network over-air standard. The format used is suitable for other private applications where the high-speed transfer of data over narrow-band wireless links is required. The MX909A is programmable to operate at standard bit-rates from a wide choice of XTAL/CLOCK frequencies.

The MX909A may be used with a 3.0V to 5.5V power supply and is available in the following packages: 24-pin SSOP (MX909ADS), 24-pin SOIC (MX909ADW), 24-pin PLCC (MX909ALH), and 24-pin PDIP (MX909AP).

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1 Block Diagram

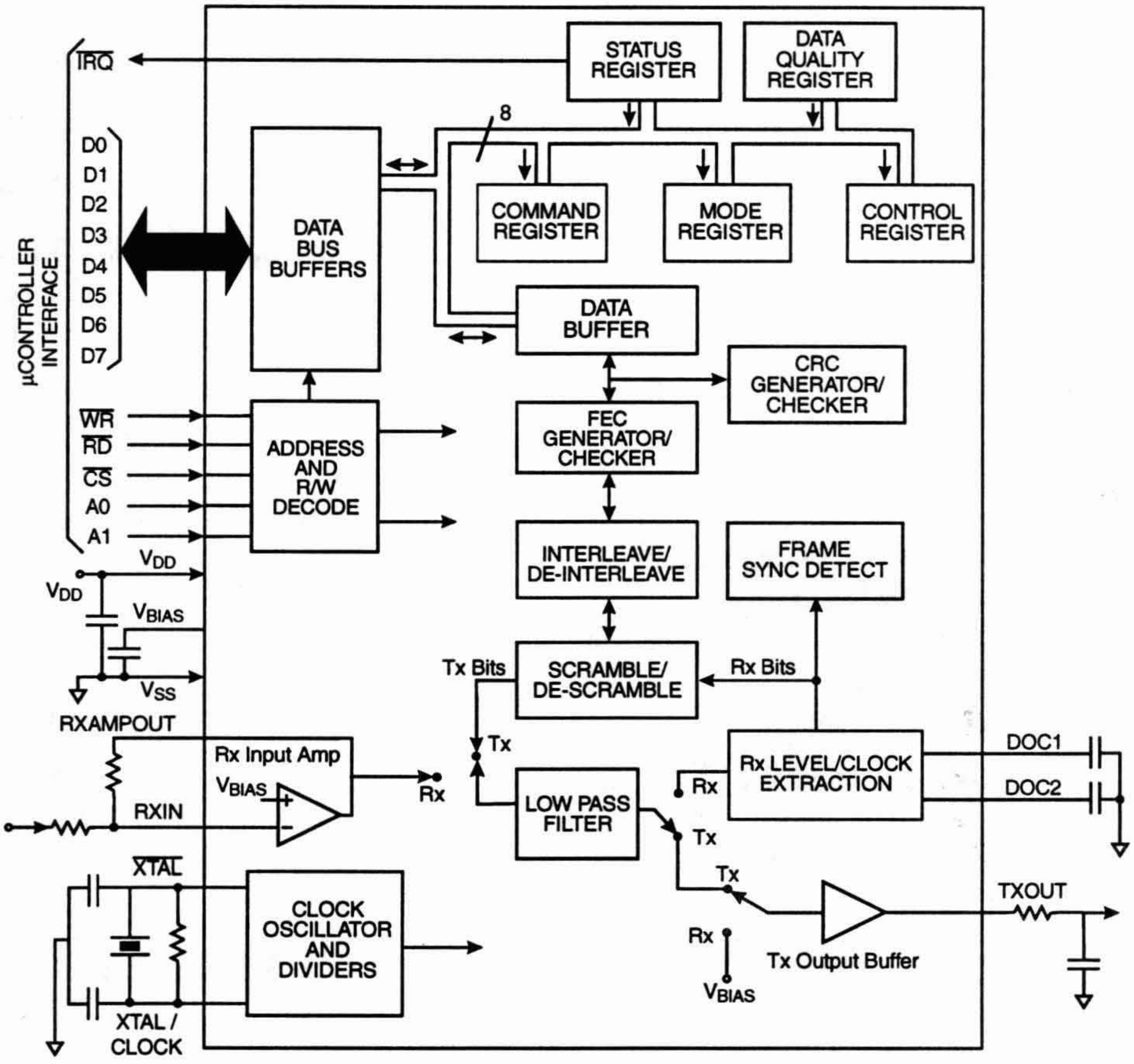

IRQ
D0
D1
D2
D3
D4
D5
D6
D7
µCONTROLLER INTERFACE
WR
RD
CS
A0
A1
STATUS REGISTER
DATA QUALITY REGISTER
8
DATA BUS BUFFERS
COMMAND REGISTER
MODE REGISTER
CONTROL REGISTER
DATA BUFFER
CRC GENERATOR/ CHECKER
ADDRESS AND R/W DECODE
FEC GENERATOR/ CHECKER
INTERLEAVE/ DE-INTERLEAVE
FRAME SYNC DETECT
VDD
VDD
VBIAS
VSS
Tx Bits
SCRAMBLE/ DE-SCRAMBLE
Rx Bits
RXAMPOUT
Rx Input Amp
VBIAS
Rx
RXIN
Tx
LOW PASS FILTER
Rx
Tx
Rx LEVEL/CLOCK EXTRACTION
DOC1
DOC2
XTAL
CLOCK OSCILLATOR AND DIVIDERS
Tx
Rx
VBIAS
Tx Output Buffer
TXOUT
XTAL / CLOCK

Figure 1: Block Diagram

2 Signal List

Pin No	Signal	Type	Description
1	$\overline{\text{IRQ}}$	output	This pin is a 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7 - D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{\text{RD}}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{\text{WR}}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply. (ground).
13	$\overline{\text{CS}}$	input	Chip Select. An active low logic level input to the modem. It is used to enable a data read or write operation.
14	A0	input	Logic level modem register select input.
15	A1	input	Logic level modem register select input.
16	$\overline{\text{XTAL}}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for an external CLOCK or XTAL circuit.
18	DOC 2	output	Connects to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
19	DOC 1	output	Connects to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
20	TXOUT	output	Tx output signal from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	The output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Voltage levels are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

3 External Components

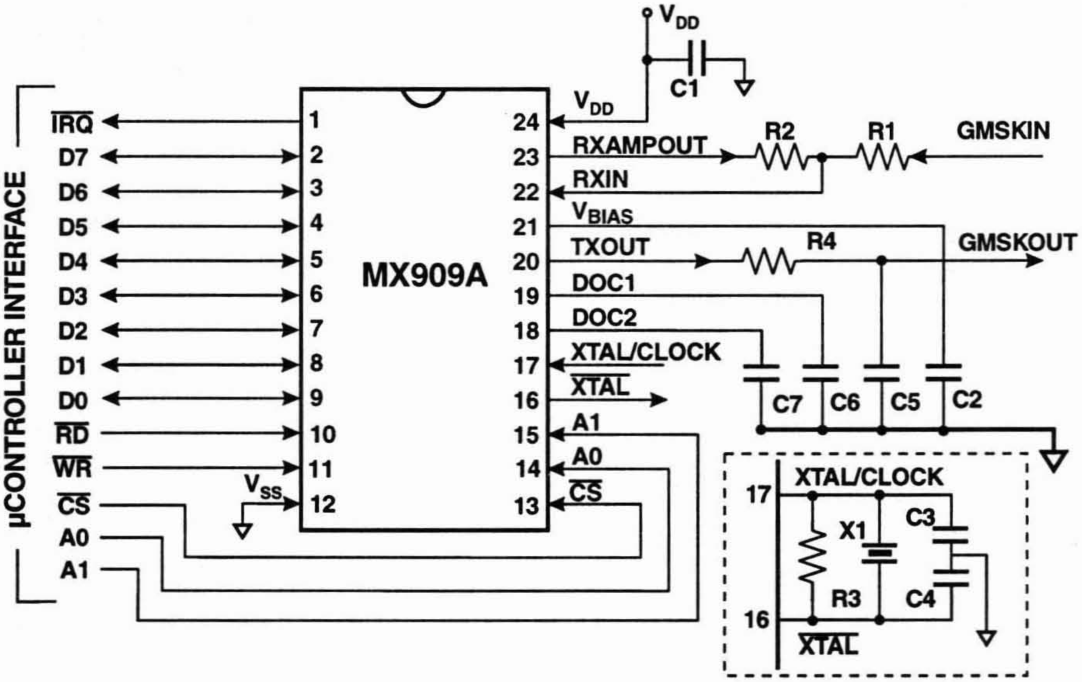

VDD
C1
IRQ
D7
D6
D5
D4
D3
D2
D1
D0
RD
WR
CS
A0
A1
µCONTROLLER INTERFACE
VSS
MX909A
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
RXAMPOUT
RXIN
VBIAS
TXOUT
DOC1
DOC2
XTAL/CLOCK
XTAL
A1
A0
CS
R2
R1
GMSKIN
R4
GMSKOUT
C7
C6
C5
C2
17
16
XTAL/CLOCK
X1
C3
R3
C4
XTAL

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±10%
R3		1MΩ	±20%
R4	2		±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	3		±20%
C4	3		±20%
C5	2		±10%
C6	4		±20%
C7	4		±20%
X1	3		

Recommended External Component Notes:

1. See section 4.1.10.
2. See section 4.1.12.
3. See section 4.4.3.
4. C6 and C7 values should satisfy the following formula:

$$C \text{ (Farads)} = 120 \times 10^{-6} / \text{Data Rate (bits/second)}$$

Data Rate (kbits/sec)	4.0	4.8	8.0	9.6	16.0	19.2
C6 / C7 (uF)	0.03	0.022	0.015	0.012	0.0068	0.0068

4 General Description

This product has been designed to be compliant with the appropriate sections of the "Mobitex™ Interface Specification".

4.1 Description of Data Blocks

4.1.1 Data Bus Buffers

8 bi-directional, 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input $\overline{CS}$), and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address, and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory mapped, as shown in Figure 3.

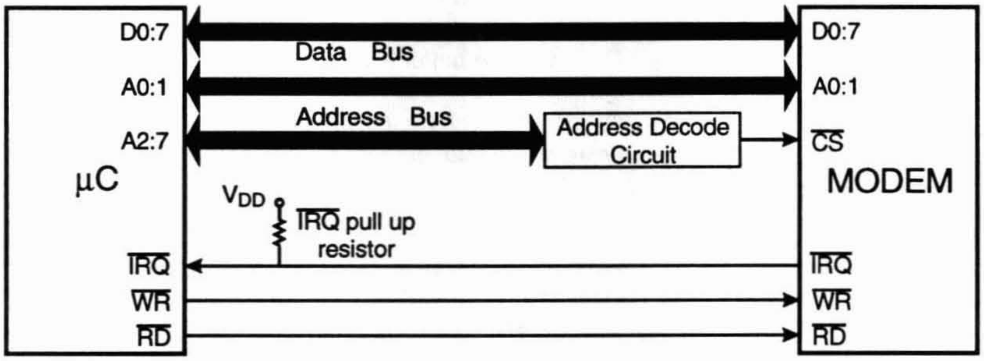


Figure 3: Typical Modem µC Connections

4.1.3 Status and Data Quality Registers

8-bit registers which the µC can read to determine the status of the modem and the received data quality.

4.1.4 Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

An 18-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which are included in transmitted Mobitex™ data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode this circuit calculates and adds the Forward Error Correction (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that have occurred in a Mobitex™ Data Block or in the Frame Head control bytes.

4.1.8 Interleave / De-interleave Buffer

This circuit interleaves data bits within a data block before transmission and de-interleaves the received data block so the FEC system is best able to handle short noise bursts or signal fades.

4.1.9 Frame Sync Detect

This circuit, (only active in receive mode), is used to look for the user specified 16-bit Frame Synchronization pattern which is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give (0.2 x V_{DD})V_{P-P} at the RXAMPOUT pin for a received '...11110000...' sequence.

A capacitor may be fitted if AC coupling of the received signal is desired (see section 5.4), otherwise the DC level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} (V_{DD}/2).

4.1.11 Tx/Rx Low Pass Filter

This filter, which is used in both transmit and receive modes, is a low pass transitional Gaussian filter having a loss of 3dB at 0.3 times the selected bit rate (BT = 0.3). See Figure 4.

In transmit mode, the bits are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode this filter is used with an increased BT factor (0.56) to reject HF noise, so the signal is suitable for extraction of the received data.

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 2 bit periods to prevent unwanted signals, from the low pass filter, at the output. When the modem is set to powersave mode, the buffer is turned off and the TXOUT pin connected to V_{BIAS} via a high value resistance. When exiting from power save mode the Tx output is only reconnected to the buffer after 2 bit periods, to prevent unwanted signals, from the low pass filter, at the output.

Note: The RC low pass filter formed by the external components R4 and C5 between the Tx Output Buffer and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any DC level-shifting and gain adjustment circuitry. The ground connection to the capacitor C5 should be positioned to give maximum attenuation of high frequency noise into the modulator. R4 and C5 should be chosen so that the product of the resistance of R4 and capacitance of C5 is 0.34/bit rate (bit rate in bits per second). R4 should be not less than 47kΩ and the value used for the external capacitor should take into account parasitic capacitance.

Suitable values being:

	R4	C5
8000 bits/sec	100kΩ	430pF
4800 bits/sec	100kΩ	710pF

The signal at the TXOUT pin is centered around V_{BIAS} and is approx. (0.2 x V_{DD})V_{P-P}, going positive for a logic '1' and negative for a logic '0', if the modem is not inverting the Tx data.

A capacitor may be fitted if AC coupling of the input to the frequency modulator is desired, see section 5.4.

The 'eye' diagram of the transmitted signal (after the external R4/C5 network) is shown in Figure 5.

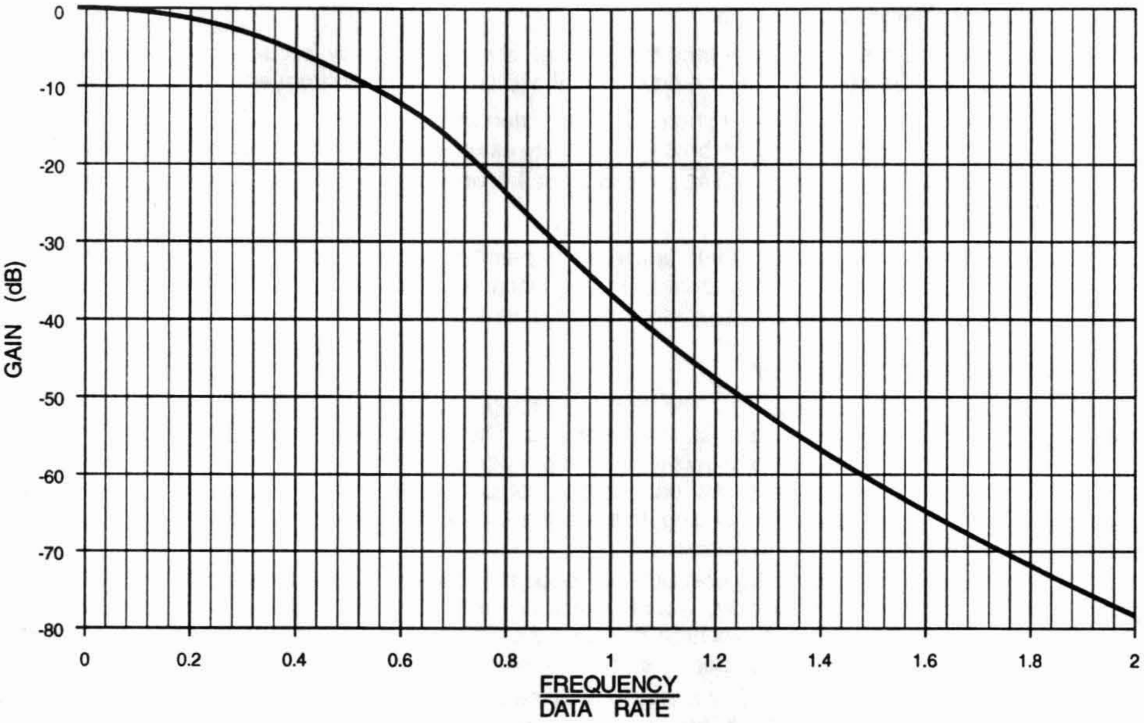


Figure 4: Typical Tx Filter Frequency Response (after the external RC Filter)

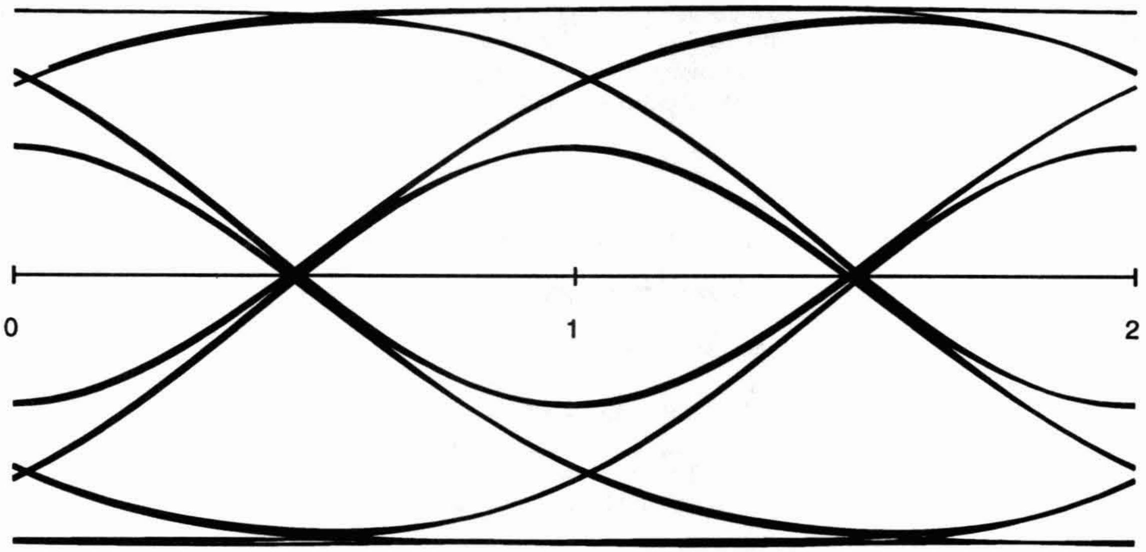


Figure 5: Transmitted Eye Signal Diagram (after the external RC Filter)

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, extract a bit rate clock from the received signal and measure the received signal amplitude and DC offset. This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

4.1.14 Clock Oscillator and Dividers

This circuit derives the transmit bit rate (and the nominal receive bit rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then the external clock source should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4, and R3 not fitted.

4.1.15 Scramble/De-scramble

This block may be used to scramble/de-scramble the transmitted/received data blocks. It does this by modulating the data with a 511-bit pseudorandom sequence, as described in section 4.5.4, smoothes the transmitted spectrum, especially when repetitive sequences are to be transmitted.

4.2 Modem - µC Interaction

In general, data is transmitted over air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted data blocks. The Frame Head includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, Interleaving and Scrambling. Details of the message formats handled by this modem are given in section 4.3.

To reduce the processing load on the host µC, this modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting / de-formatting and (when in receive mode) in searching for and synchronizing onto the Frame Head. In normal operation the modem will only require servicing by the µC once per received or transmitted data block.

Thus, to transmit a block, the host µC has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with Forward Error Correction coding, interleave then scramble the bits before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct them (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data, to allow the transmission of special Bit and Frame Synchronization sequences or test patterns.

4.3 Data Formats

4.3.1 General Purpose Formats

In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be: transmitted as:

TQB (bit and frame sync) + TQB (addresses) + (n x TDB) + TSB

received as:

SFS + RSB + RSB + RSB + RSB + (n x RDB)

Note: It is important to have established frame Synchronization before receiving data to enable the receiving device to decode synchronously. The user may add, by way of algorithms performed on the controlling device, additional data correction with the bytes in the data block task.

4.3.2 Mobitex™ Frame Structure

The Mobitex™ format for transmitted data is in the form of a Frame Head immediately followed by a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes:

2 bytes of bit sync:

1100110011001100 from base,
0011001100110011 from mobile
bits are transmitted from left to right

Mobitex™ Frame Structure cont...

- 2 bytes of frame sync:
  - System specific.
- 2 bytes of control data.
- 1 byte of FEC code, 4 bits for each of the control bytes:
  - bits 7-4 (leftmost) operate on the first control byte.
  - bits 3-0 (rightmost) operate on the second control byte.
- Each byte in the Frame Head is transmitted bit 7 (MSB) first to bit 0 (LSB) last.

The Data Block consists of:

- 18 bytes of data.
- 2 bytes of CRC calculated from the 18 data bytes.
- 4 bits of FEC code for each of the data and CRC bytes
- The resulting 240 bits are interleaved and scrambled before transmission.

The over air signal is composed of Frame Sync and Bit Sync patterns, Control bytes, and Data Blocks as shown in Figure 6.

The binary data transferred between the modem and the host µC is shown in the Frame Head and Data Block of Figure 6 as shaded areas.

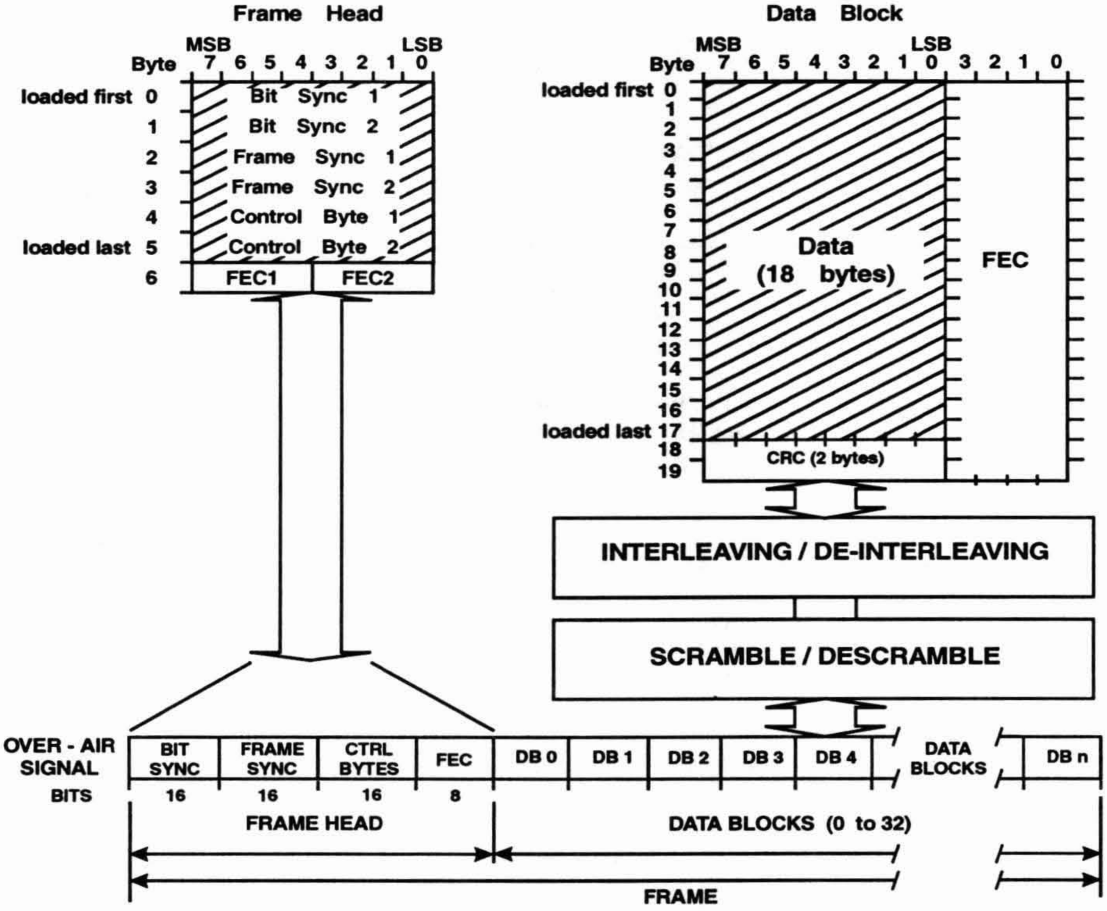

Frame Head
MSB
LSB
Byte 7 6 5 4 3 2 1 0
loaded first 0
1
2
3
4
loaded last 5
6
Bit Sync 1
Bit Sync 2
Frame Sync 1
Frame Sync 2
Control Byte 1
Control Byte 2
FEC1
FEC2
Data Block
MSB
LSB
Byte 7 6 5 4 3 2 1 0 3 2 1 0
loaded first 0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
loaded last 17
18
19
Data (18 bytes)
FEC
CRC (2 bytes)
INTERLEAVING / DE-INTERLEAVING
SCRAMBLE / DESCRAMBLE
OVER - AIR SIGNAL
BITS
BIT SYNC
FRAME SYNC
CTRL BYTES
FEC
16
16
16
8
DB 0
DB 1
DB 2
DB 3
DB 4
DATA BLOCKS
DB n
FRAME HEAD
DATA BLOCKS (0 to 32)
FRAME

Figure 6: Mobitex™ Over Air Signal Format

4.4 The Programmer's View

The modem appears to the programmer as 4 write only 8-bit registers shadowed by 3 read only registers, individual registers being selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

4.4.1 Data Buffer

This is an 18-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality and control information) between the modem and the host µC.

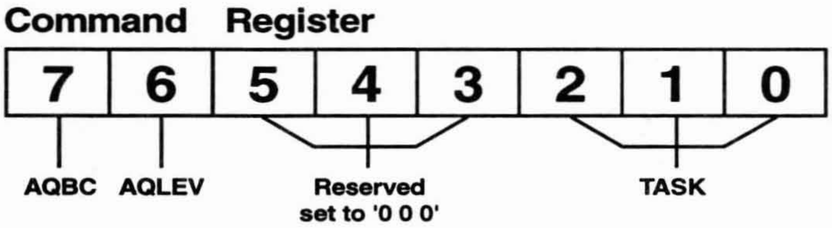
It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode (except when loading Frame Sync detection bytes while in Rx mode).

4.4.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQBC bits.



When there is no action to perform and not 'powersaved', the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract bits from the received signal, supplying them to the de-interleave buffer, otherwise the received data is ignored.

4.4.2.1 Command Register B7: AQBC - Acquire Bit Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with AQBC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve bit timing Synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing Synchronization is achieved, until the 'normal' value set by the PLLBW bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQBC bit set to '1'.

The AQBC bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock Synchronization quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQBC bit '0' if it is known that clock Synchronization does not need to be re-established. More details of the bit clock acquisition sequence are given in section 5.3.

4.4.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then

Command Register B6: AQLEV - Acquire Receive Signal Levels (cont...)

gradually increasing their response time, thereby improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels. Further information of the level measurement acquisition sequence is provided in section 5.3.

The error rate is highest immediately after an AQBC and AQLEV sequence is triggered and rapidly reduces to its static value soon after. These erroneous bits could incorrectly trigger the frame sync detection circuits. It is suggested that an SFH or SFS task be set 12 bits after setting either of the AQLEV or AQBC sequences.

4.4.2.3 Command Register B5, B4, B3

These bits should be set to '0'.

4.4.2.4 Command Register B2, B1, B0: TASK - Task

Operations such as transmitting a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL, RESET and TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µC should wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE (Buffer Free) bit of the Status Register to '0'.
>
> Take the data from the Data Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.
>
> Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{\text{IRQ}}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

In this way the µC can write a task and the associated data to the modem while the modem is still transmitting the data from the previous task. See Figure 7.

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE bit of the Status Register to '0'.
>
> Wait until enough received bits are in the De-interleave Buffer.
>
> Decode them as needed, and transfer any resulting data to the Data Buffer
>
> Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{\text{IRQ}}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µC can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-interleave Buffer. See Figure 8.

The above is not true for loading the Frame Sync detection bytes (LFSB): the bytes to be compared with the incoming data must be loaded prior to the task bits being written.

Detailed timings for the various tasks are given in Figure 9 and Figure 10.

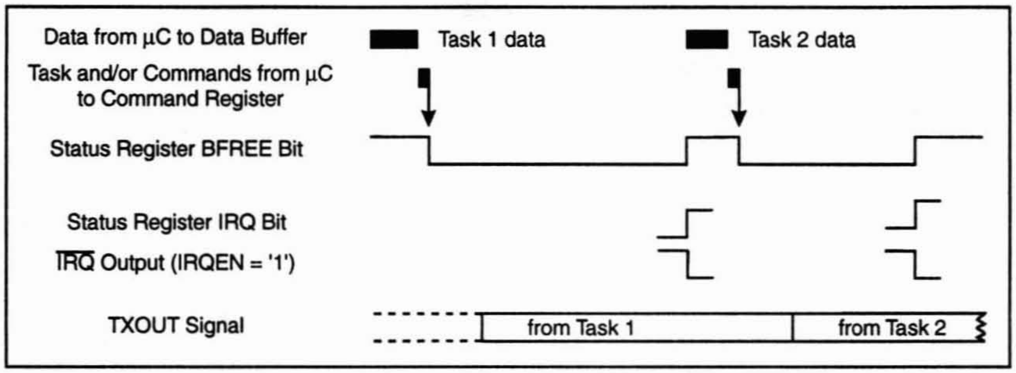

Data from µC to Data Buffer
Task 1 data
Task 2 data
Task and/or Commands from µC to Command Register
Status Register BFREE Bit
Status Register IRQ Bit
IRQ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 7: Transmit Process

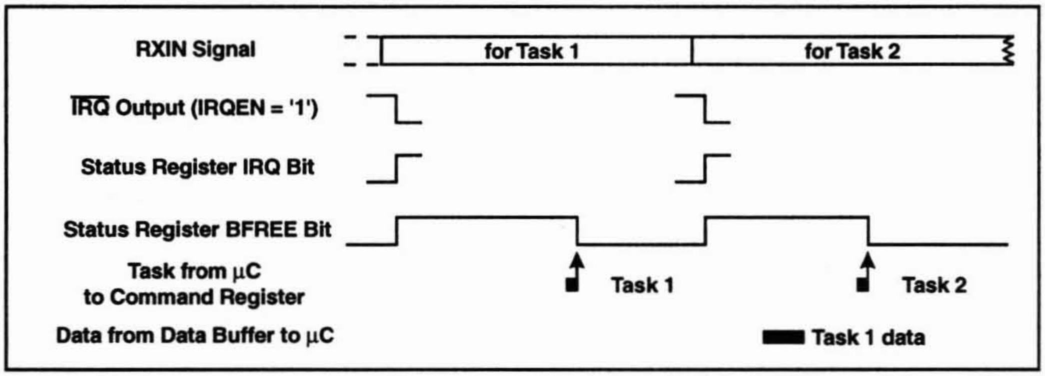

RXIN Signal
for Task 1
for Task 2
IRQ Output (IRQEN = '1')
Status Register IRQ Bit
Status Register BFREE Bit
Task from µC to Command Register
Task 1
Task 2
Data from Data Buffer to µC
Task 1 data

Figure 8: Receive Process

Mobitex™ Modem Tasks

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFH	Search for Frame Head	T7H	Transmit 7 byte Frame Head
0	1	0	R3H	Read 3 byte Frame Head		Reserved
0	1	1	RDB	Read Data Block	TDB	Transmit Data Block
1	0	0	SFS	Search for Frame Sync	TQB	Transmit 4 Bytes
1	0	1	RSB	Read Single Byte	TSB	Transmit Single Byte
1	1	0	LFSB	Load Frame Sync Bytes	TSO	Transmit Scrambler Output
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.4.2.5 NULL - No effect

This task is provided so that a AQBC or AQLEV command can be initiated without loading a new task.

4.4.2.6 SFH - Search for Frame Head

Causes the modem to search the received signal for a Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data (see Figure 6). The search will continue until a Frame Head has been found, or until the RESET task is loaded.

The search is carried out by first attempting to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error). When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes, these bytes will be checked, and corrected if necessary, using the FEC bits. The two Frame Head Data bytes are then placed into the Data Buffer.

The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µC may read the 2 Frame Head Data bytes from the Data Buffer and write the next task to the Command Register. If the FEC indicates uncorrectable errors the modem will set the CRCFEC bit in the Status Register to a logic '1'.

The MO/$\overline{\text{BA}}$ bit (Mobile or Base) in the Status Register will be set according to the polarity of the 3 bits preceding the Frame Sync pattern.

4.4.2.7 R3H - Read 3-byte Frame Head

This task, which would normally follow an SFS task, will place the next 3 bytes directly into the Data Buffer. It also causes the modem to check the 3 bytes as Frame Head control data bytes and will set the CRCFEC bit to a logic '1' only if the FEC bits indicate uncorrectable errors.

Note: This task will not correct any errors and, due to the Mobitex™ FEC specification, will not detect all possible uncorrectable error patterns. The BFREE and IRQ bits of the Status Register will be set to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register.

The CRCFEC bit in the Status Register will be set according to the validity of the received FEC bits.

4.4.2.8 RDB - Read Data Block

This task causes the modem to read the next 240 bits as a Mobitex™ Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 18 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: In receive mode the CRC checksum circuits are initialized on completion of any task other than NULL.

4.4.2.9 SFS - Search for Frame Sync

This task, which is intended for special test and channel monitoring purposes, performs the first part only of a SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the Frame Synchronization pattern with up to any 1 bit in error.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' and update the MO/$\overline{\text{BA}}$ bit. The µC may then write the next task to the Command Register.

4.4.2.10 RSB - Read Single Byte

This task causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task.

4.4.2.11 LFSB - Load Frame Sync Bytes

This task takes 2 bytes from the Data Buffer and updates the Frame Sync detect bytes. The MSB of byte '0' is compared to the first bit of a received Frame Sync pattern and the LSB of byte '1' is compared to the last bit of a received Frame Sync pattern. This task does not enable Frame Sync detection.

Unlike other Rx tasks, the data buffer must be loaded before the task is issued and the task must only be issued 'between' received messages, i.e. before the first task for receiving a message and after the last data is read out of the data buffer.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task to the modem.

4.4.2.12 T7H - Transmit 7-byte Frame Head

This task takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes '4' and '5' then transmits the result as a complete Mobitex™ Frame Head.

Bytes '0' and '1' form the bit sync pattern, bytes '2' and '3' form the frame sync pattern and bytes '4' and '5' are the frame head control bytes. Bit 7 of byte '0' of the Data Buffer is sent first, bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

4.4.2.13 TQB - Transmit 4 Bytes

This task takes 4 bytes of data from the Data Buffer and transmits them, bit 7 first.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

4.4.2.14 TDB - Transmit Data Block

This task takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex™ Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialized on completion of any task other than NULL.

4.4.2.15 TSB - Transmit Single Byte

This task takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first.

Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

4.4.2.16 TSO - Transmit Scrambler Output

This task, intended for channel set-up, enables the scrambler and transmits its output.

When the modem has started the task, the Status Register bits will not be changed and an IRQ will not be raised. The µC may write the next task and its data to the modem at any time and the scrambler output will stop when the new task has produced its first data.

4.4.2.17 RESET - Stop any current action

This task takes effect immediately, and terminates any current action (task, AQBC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied to set the modem into a known state.

Note: Due to delays in the internal switched capacitor filter, it will take approximately 3 bit times for any change to become apparent at the TXOUT pin.

4.4.2.18 Task Timings

The device should not be given a new task for at least 2 bit times after the following:

Changing from powersave state to normal operation.

Changing the $Tx/\overline{Rx}$ bit.

Resetting or after power is applied to the device.

This is to ensure that the internal operation of the device is initialized correctly for the new task.

Note: This only applies to the Command Register, other registers may be accessed as normal.

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Ref. Figure 9 and Figure 10		Task	Typical (bit-times)
t_1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t_2	Time from application of first bit of task to TX Low Pass Filter until BFREE goes to a logic 1	T7H	36
		TQB	24
		TDB	20
		TSB	1
t_3	Time to transmit all bits of task	T7H	56
		TQB	32
		TDB	240
		TSB	8
t_4	Max time allowed from BFREE going to a logic 1 for next task (and data) to be written to the modem	T7H	18
		TQB	6
		TDB	218
		TSB	6
t_5	Time to receive all bits of task	SFH	56
		R3H	24
		RDB	240
		RSB	8
t_6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem	SFH	14
		R3H	18
		RDB	218
		RSB	6
t_7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1'	Any	1

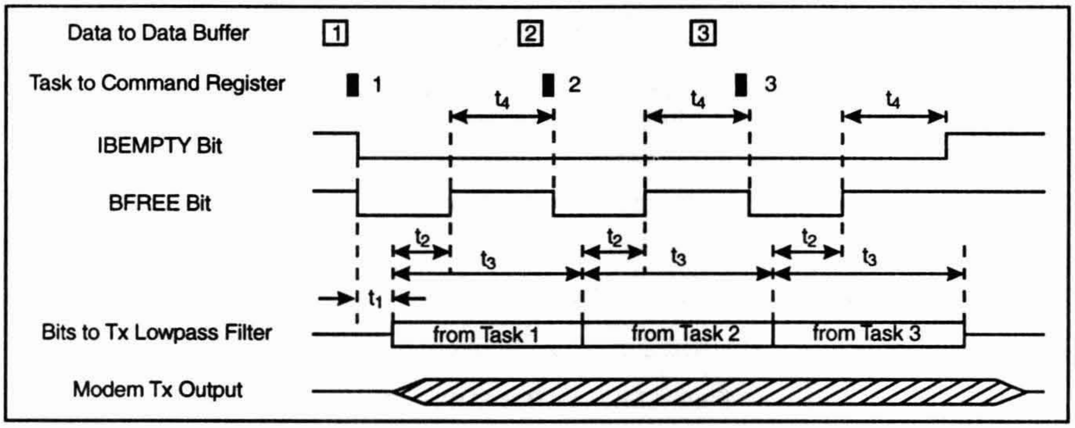

Data to Data Buffer
1
2
3
Task to Command Register
1
2
3
t4
t4
t4
IBEMPTY Bit
BFREE Bit
t2
t3
t2
t3
t2
t3
t1
Bits to Tx Lowpass Filter
from Task 1
from Task 2
from Task 3
Modem Tx Output

Figure 9: Transmit Mode Timing Diagram

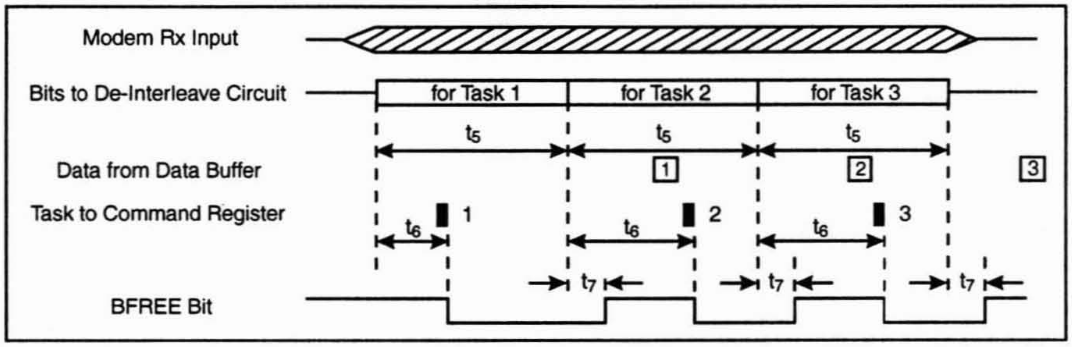

Modem Rx Input
Bits to De-Interleave Circuit
for Task 1
for Task 2
for Task 3
t_5
t_5
t_5
Data from Data Buffer
1
2
3
Task to Command Register
t_6
1
t_6
2
t_6
3
t_7
t_7
t_7
BFREE Bit

Figure 10: Receive Mode Timing Diagram

4.4.2.19 Tx/Rx Low Pass Filter Delay

The previous task timing figures are based on the signal at the input to the Tx Low Pass filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 2 bit times in both transmit and receive modes due to the Tx/Rx Low Pass filter, as illustrated in Figure 11.

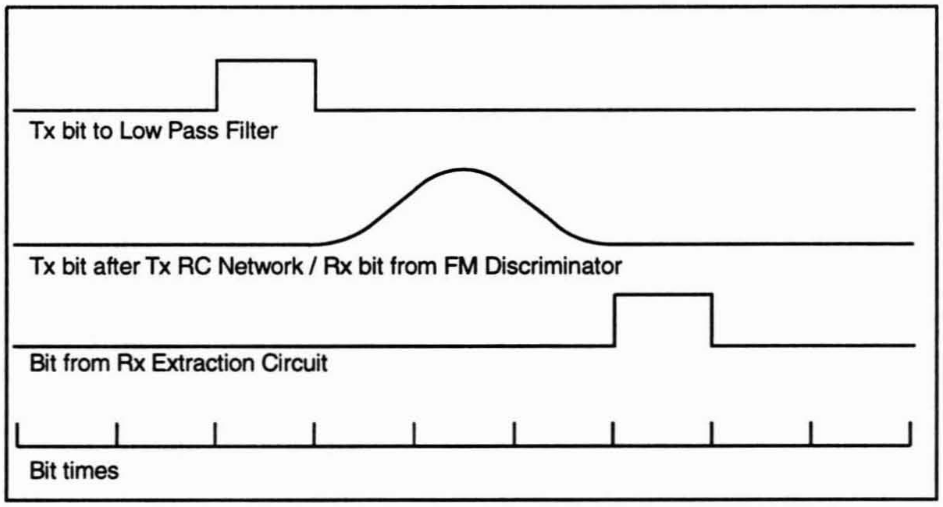
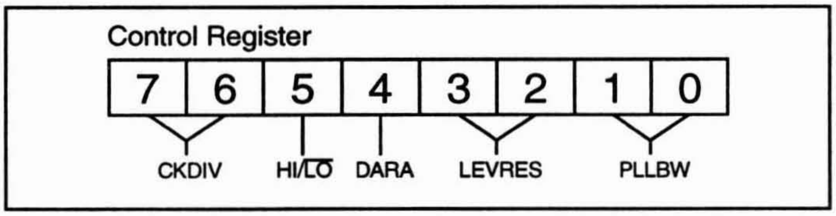

Tx bit to Low Pass Filter
Tx bit after Tx RC Network / Rx bit from FM Discriminator
Bit from Rx Extraction Circuit
Bit times

Figure 11: Low Pass Filter Delay

4.4.3 Control Register

This 8-bit write only register controls the modem's bit rate, the response times of the receive clock extraction and signal level measurement circuits and the internal analog filters.


Control Register
7
6
5
4
3
2
1
0
CKDIV
HI/$\overline{\text{LO}}$
DARA
LEVRES
PLLBW

4.4.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio and B5: HI/$\overline{\text{LO}}$ - Xtal Range Selection

These bits control a frequency divider driven from the clock signal present at the $\overline{\text{XTAL}}$ pin, which determines the nominal bit rate. The table below shows how bit rates of 4000/8000/16000 or 4800/9600/19200 bits/sec may be obtained from common Xtal frequencies:

		B5		**XTAL / CLOCK Frequency (MHz)**					
		1		8.192	9.8304	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
			0	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)	1.024	1.2288
B7	**B6**	**Division Ratio:** **XTAL Frequency / Data Rate**		**Data Rates (bits per second)**					
0	0	256	128			16000	19200	8000	96000
0	1	512	256	16000	19200	8000	9600	4000	4800
1	0	1024	512	8000	9600	4000	4800		
1	1	2048	1024	4000	4800				

Note: Device operation is not guaranteed below 4000 or above 19200 bits/sec.

The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide; C3 = C4 = 33pF for X1 < 5MHz, and C3 = C4 = 18pF for X1 > 5MHz.

4.4.3.2 Control Register B4: DARA - Data Rate

This bit operates in both transmit and receive modes, optimizing the modem's internal signal filtering according to the relevant bit rate.

If the bit rate used is above 10k bits/sec then this bit should be set to '1' , if not, then it should be set to '0'.

4.4.3.3 Control Register B3, B2: LEVRES - Level Measurement Response Time

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' response time of the Rx signal amplitude and DC offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

B3	**B2**		
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detect
1	1	Lossy Peak Detect	Track input signal using lossy peak detection

For Mobitex™ systems, and most general purpose applications using the modem, these bits should normally be set to 'Peak Averaging', except when the µC detects a receive signal fade, when 'Hold' should be selected.

The 'Lossy Peak Detect' setting is intended for systems where the µC cannot detect signal fades or the start of a received message, as it allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note: Since the measured levels are stored on the external capacitors C6 and C7, they will decay gradually towards V_{BIAS} when the 'Hold' setting is chosen, the discharge time-constant being approximately 2000 bit times. Further information of the level measurement system is provided in section 5.3.

4.4.3.4 Control Register B1, B0: PLLBW

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQBC command.

B1	B0	PLL Bandwidth	Suggested use
0	0	Hold	Signal fades
0	1	Narrow	± 20ppm or better Xtals
1	0	Medium	Wide tolerance Xtals or long preamble acquisition
1	1	Wide	Quick acquisition

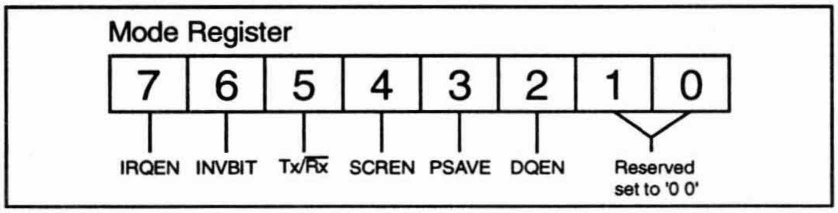
The 'hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the transmit and receive modem bit rate tolerances should be chosen.

The wide and medium bandwidth settings are intended for systems where the µC cannot detect signal fades or the start of a received message, as they allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note: Further information of the clock extraction system is provided in section 5.3.

4.4.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.4.4.1 Mode Register B7: IRQEN- $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

4.4.4.2 Mode Register B6: INVBIT - Invert Bits

This bit controls inversion of transmitted and received bit voltages. When set to '1' all data is inverted in the Tx and Rx data paths so a transmitted '1' is a voltage below V_{BIAS} at the TXOUT pin and a received '0' is a voltage above V_{BIAS} at the RXIN pin. Data will be inverted immediately after this bit is set to '1'.

4.4.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. When changing from Rx to Tx there must be a 2-bit pause before setting a new task to allow the filter to stabilize. (See also PSAVE bit).

Note: Changing between receive and transmit modes will cancel any current task

4.4.4.4 Mode Register B4: SCREN - Scramble Enable

The scrambler only takes effect during the transmission or reception of a Mobitex™ Data Block and during a TSO task. Setting this bit to '1' enables scrambling, clearing it to '0' disables scrambling.

The scrambler is only operative, if enabled by this control bit, during TSO, RDB or TDB, it is held in a reset state at all other times.

This bit should not be changed while the modem is decoding or transmitting a Mobitex™ Data Block.

4.4.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx bit and Clock extraction circuits and the Tx output buffer will be disabled, and the TXOUT pin will be connected to V_{BIAS} through a high value resistance. The Xtal Clock oscillator and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

Note: The internal filters will take approximately 2 bit times to settle after the PSAVE bit is taken from '1' to '0'.

4.4.4.6 Mode Register B2: DQEN - Data Quality IRQ Enable

In receive mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new Data Quality reading is ready. (The DQRDY bit of the Status Register will also be set to '1' at the same time.)

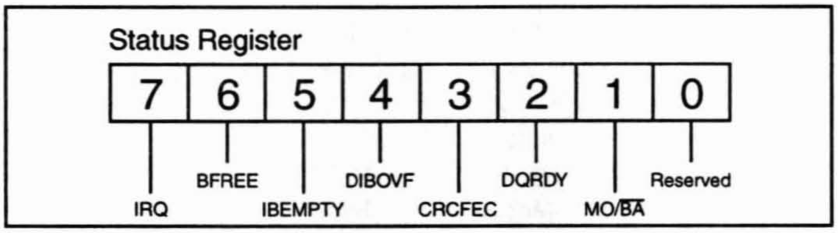
In transmit mode this bit has no effect.

4.4.4.7 Mode Register B1, B0

These bits should be set to '0'.

4.4.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.4.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register PSAVE or TX/$\overline{RX}$ bits.

The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register PSAVE or TX/$\overline{RX}$ bits.

The Status Register DQRDY bit going from '0' to '1' (If DQEN = '1').

The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (to V_{SS}) whenever the IRQ bit is '1'.

4.4.5.2 Status Register B6: BFREE - Data Buffer Free

This bit reflects the availability of the Data Buffer and is cleared to '0' whenever a task other than NULL, RESET or TSO is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1', but without setting the IRQ bit, by a RESET task or when the Mode Register PSAVE or TX/$\overline{RX}$ bits are changed.

4.4.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1', also setting the IRQ bit, when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' by writing a task other than NULL, RESET or TSO to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level voltage (V_{BIAS}) will be applied to the Tx low pass filter.

In receive mode this bit will be '0'.

4.4.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' by reading the Status Register or by writing a RESET task to the Command Register or by changing the PSAVE or TX/$\overline{RX}$ bits of the Mode Register.

In transmit mode this bit will be '0'.

4.4.5.5 Status Register B3: CRCFEC - CRC or FEC Error

In receive mode this bit will be updated at the end of a Mobitex™ Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A '0' indicates that the CRC was received correctly or the FEC did not find uncorrectable errors, a '1' indicates that errors are present.

The bit is cleared to '0' by a RESET task or by changing the PSAVE or TX/$\overline{\text{RX}}$ bits of the Mode Register.

In transmit mode this bit will be '0'.

4.4.5.6 Status Register B2: DQRDY - Data Quality Reading Ready

In receive mode, this bit is set to '1' whenever a Data Quality reading has been completed. See section 4.4.6.

The bit is cleared to '0' by a read of the Data Quality Register.

Immediately after a RESET task, or a change in the PSAVE or TX/$\overline{\text{RX}}$ bits to '0', the DQRDY bit may be set and generate an interrupt. The value in the Data Quality Register will not be valid in this case.

4.4.5.7 Status Register B1: MO/$\overline{\text{BA}}$ - Mobile or Base Bit Sync Received

In receive mode this bit is updated at the end of the SFS and SFH tasks. This bit is set to '1' whenever the 3 bits immediately preceding a detected Frame sync are '011' (received left to right), with up to any one bit in error. The bit is set to '0' if the bit pattern is '100', again with up to any one bit in error. Thus, if this bit is set to '1' then the received message is likely to have originated from a Mobile and if it is set to '0' from a Base Station. See section 4.3.

In transmit mode this bit is a logic '0'.

4.4.5.8 Status Register B0

This bit will always be set to '0'.

4.4.6 Data Quality Register

This is intended to indicate the quality of the receive signal during a Mobitex™ Data Block or 30 single bytes. In receive mode, the modem measures the 'quality' of the received signal by comparing the actual received zero crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the DQRDY bit in the Status Register is updated.

Note: An interrupt will only occur at this time if the DQEN bit = '1'.

To provide Synchronization with Data Blocks, and to ensure the Data Quality Register is updated in preparation to be read when the RDB task finishes, the measurement process is reset at the end of tasks SFH, SFS, RDB and R3H.

In transmit mode all bits of the Data Quality Register will be '0'.

Figure 12 shows how the value (0-240) read from the Data Quality Register varies with received signal to noise ratio.

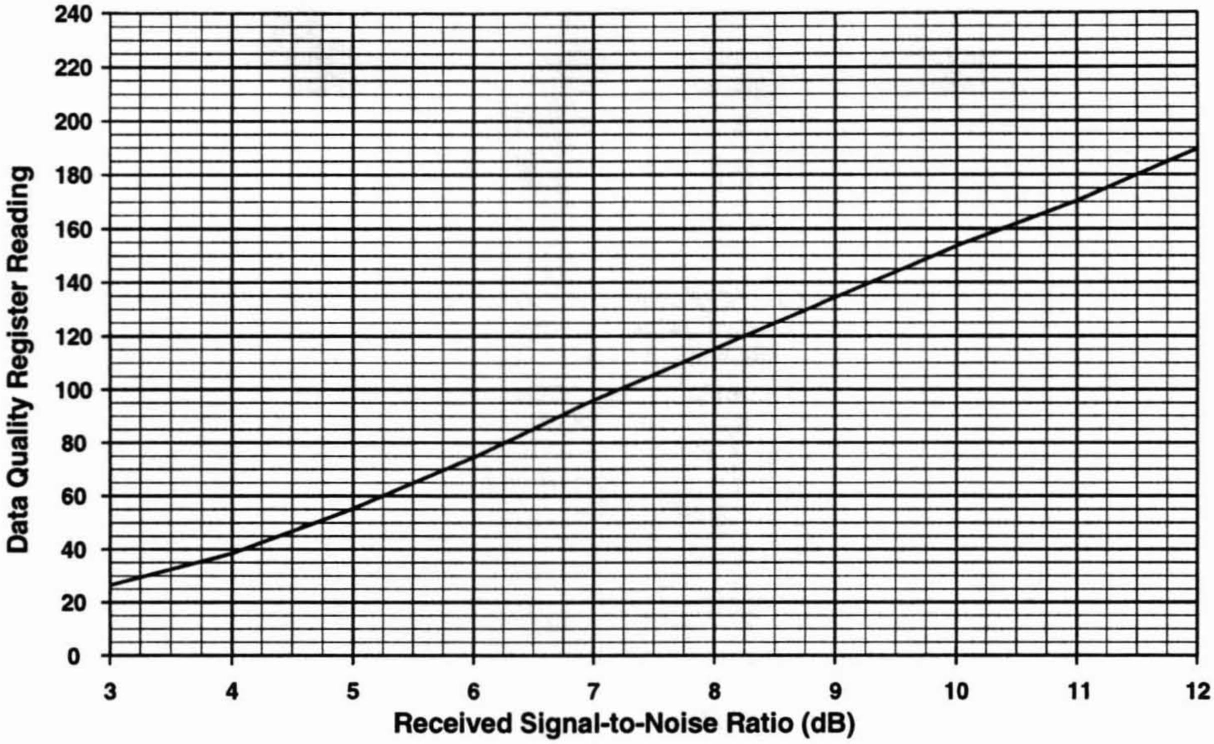


Figure 12: Typical Data Quality Reading (after 240 bits) vs. S/N, (noise in bit rate bandwidth)

4.5 CRC, FEC, Interleaving and Scrambling Information

4.5.1 CRC

This is a 16-bit CRC code used in the Mobitex™ Data Block. In transmit it is calculated by the modem from the 18 data bytes using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

i.e. CRC - CCITT X.25.

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC register is initialized to all '1s' and the CRC is calculated octet by octet starting with the least significant bit of 'byte 0'. The CRC calculated is bit-wise inverted and appended to the data bytes with the most significant bit transmitted earliest.

In receive mode, a 16-bit CRC code is generated from the 18 data bytes of each Mobitex™ Data Block as above and the bit-wise inverted value is compared with the received CRC bytes. If a mismatch is present, then an error has been detected.

4.5.2 FEC

In transmit mode, during T7H and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte. The FEC is defined by the following H matrix:

$$H = \begin{array}{cc} 7\_\_\_\_\_\_0 & 3\_\_0 \\ 11101100 & 1000 \\ 11010011 & 0100 \\ 10111010 & 0010 \\ 01110101 & 0001 \end{array}$$

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

In checking the FEC, the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble is all zero then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occurred.

This code can correct any single error that has occurred in each 12-bit (8 data + 4 FEC) section of the message.

Example:

If the byte to be coded is '00101100' then the FEC is derived as follows:

H matrix row:	1	2	3	4
A	11101100	11010011	10111010	01110101
B	00101100	00101100	00101100	00101100
A AND B	00101100	00000000	00101000	00100100
Even Parity:	1	0	0	0

Where A is bits 7 - 0 of one row of the H matrix and B is the byte to be coded. The even parity bits apply to the result of 'A AND B'.

So the word formed will be: '00101100 1000' sent left to right

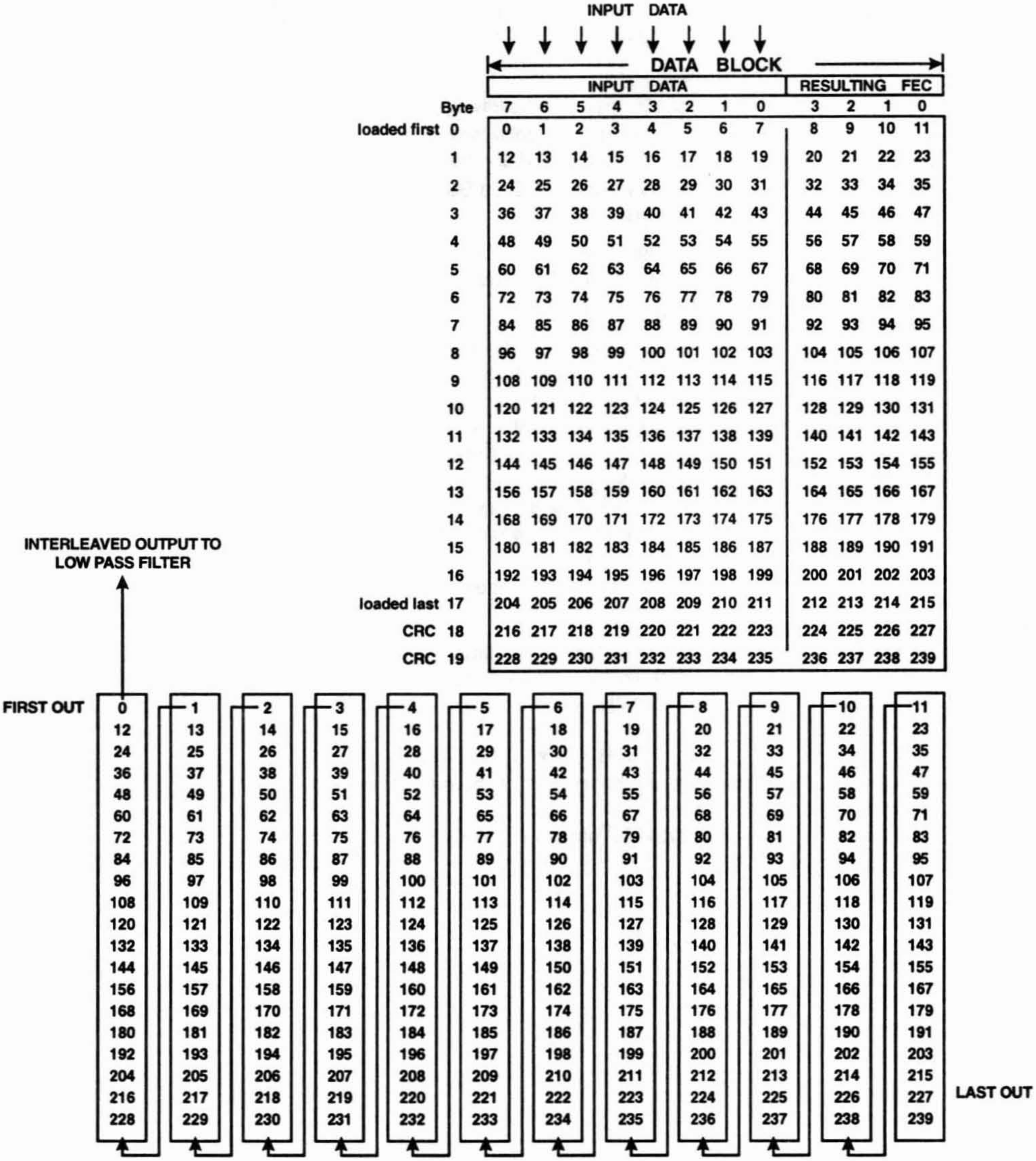
When the same process is carried out on these 12 bits as above, using all 12 bits of each H matrix row, the resulting 4 parity bits will be '0000'.

4.5.3 Interleaving

The 240 bits of a Mobitex™ Data Block are interleaved by the modem before transmission to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex™ Frame Head.

Considering the 240 bits to be numbered sequentially before interleaving as 0 to 239
('0' = bit 7 of byte 0, '11' = bit 0 of FEC for byte 0, ... ,'239' = bit 0 of FEC for byte 19 - see Figure 6), then they will be transmitted as shown in Figure 13.

The modem performs the inverse operation (de-interleaving) in receive mode on Mobitex™ Data Blocks.



	INPUT DATA								RESULTING FEC			
Byte	7	6	5	4	3	2	1	0	3	2	1	0
loaded first 0	0	1	2	3	4	5	6	7	8	9	10	11
1	12	13	14	15	16	17	18	19	20	21	22	23
2	24	25	26	27	28	29	30	31	32	33	34	35
3	36	37	38	39	40	41	42	43	44	45	46	47
4	48	49	50	51	52	53	54	55	56	57	58	59
5	60	61	62	63	64	65	66	67	68	69	70	71
6	72	73	74	75	76	77	78	79	80	81	82	83
7	84	85	86	87	88	89	90	91	92	93	94	95
8	96	97	98	99	100	101	102	103	104	105	106	107
9	108	109	110	111	112	113	114	115	116	117	118	119
10	120	121	122	123	124	125	126	127	128	129	130	131
11	132	133	134	135	136	137	138	139	140	141	142	143
12	144	145	146	147	148	149	150	151	152	153	154	155
13	156	157	158	159	160	161	162	163	164	165	166	167
14	168	169	170	171	172	173	174	175	176	177	178	179
15	180	181	182	183	184	185	186	187	188	189	190	191
16	192	193	194	195	196	197	198	199	200	201	202	203
loaded last 17	204	205	206	207	208	209	210	211	212	213	214	215
CRC 18	216	217	218	219	220	221	222	223	224	225	226	227
CRC 19	228	229	230	231	232	233	234	235	236	237	238	239

0	1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59
60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83
84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107
108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131
132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155
156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179
180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203
204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227
228	229	230	231	232	233	234	235	236	237	238	239

Figure 13: Interleaving - Input / Output

4.5.4 Scrambling

All formatted bits of a Mobitex™ Data Block are passed through a 9-bit scrambler. This scrambler is initialized at the beginning of the first Data Block in every Frame. The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages XOR'ed and fed back to the input of the first stage. The scrambler is disabled during all other tasks, apart for TSO.

5 Application

5.1 Transmit Frame Example

If the device is required to send a Mobitex™ Frame the following control signals and data should be issued to the modem, provided the device is not starting from a powersave state, TX/$\overline{\text{RX}}$ is set to '1' and that SCREN, DARA, CKDIV, and DQEN have been set as required after power was applied to the device:

1. 6 bytes forming the Frame Head are loaded into the Data Buffer, followed by a 2-bit pause to let the filter stabilize, followed by setting T7H task.
2. Device interrupts host µC with $\overline{\text{IRQ}}$ when the 6th byte is read from the Data Buffer.
3. Status Register is read and 18 bytes are loaded, followed by setting TDB task.
4. Device interrupts host µC with $\overline{\text{IRQ}}$ when 18th byte is read from the Data Buffer.
5. Status Register is read, host may load data and set next task as required:

GOTO '1'	if the last Data Block for this Frame has been transmitted and another Frame is to be immediately transmitted
GOTO '3'	if another Data Block in this Frame is to be transmitted
GOTO '6'	if no more data is to be immediately sent

6. 1 byte representing the 'hang byte' is loaded into the Data Buffer, followed by setting the TSB task.

If the 'hang byte' has been transmitted and no further data is to be sent, then a new task does not need be written and the µC can wait for the IBEMPTY interrupt ,when after a few bits, to allow for the Tx filter delay, it can shut down the Tx RF circuits.

A top level flowchart of the transmit process is shown in Figure 14.

5.1.1 Hang Byte

The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be spread across 3 bit times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8-bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex™ frame are:

T7H + (n x TDB) + TSB

When receiving this data, the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.

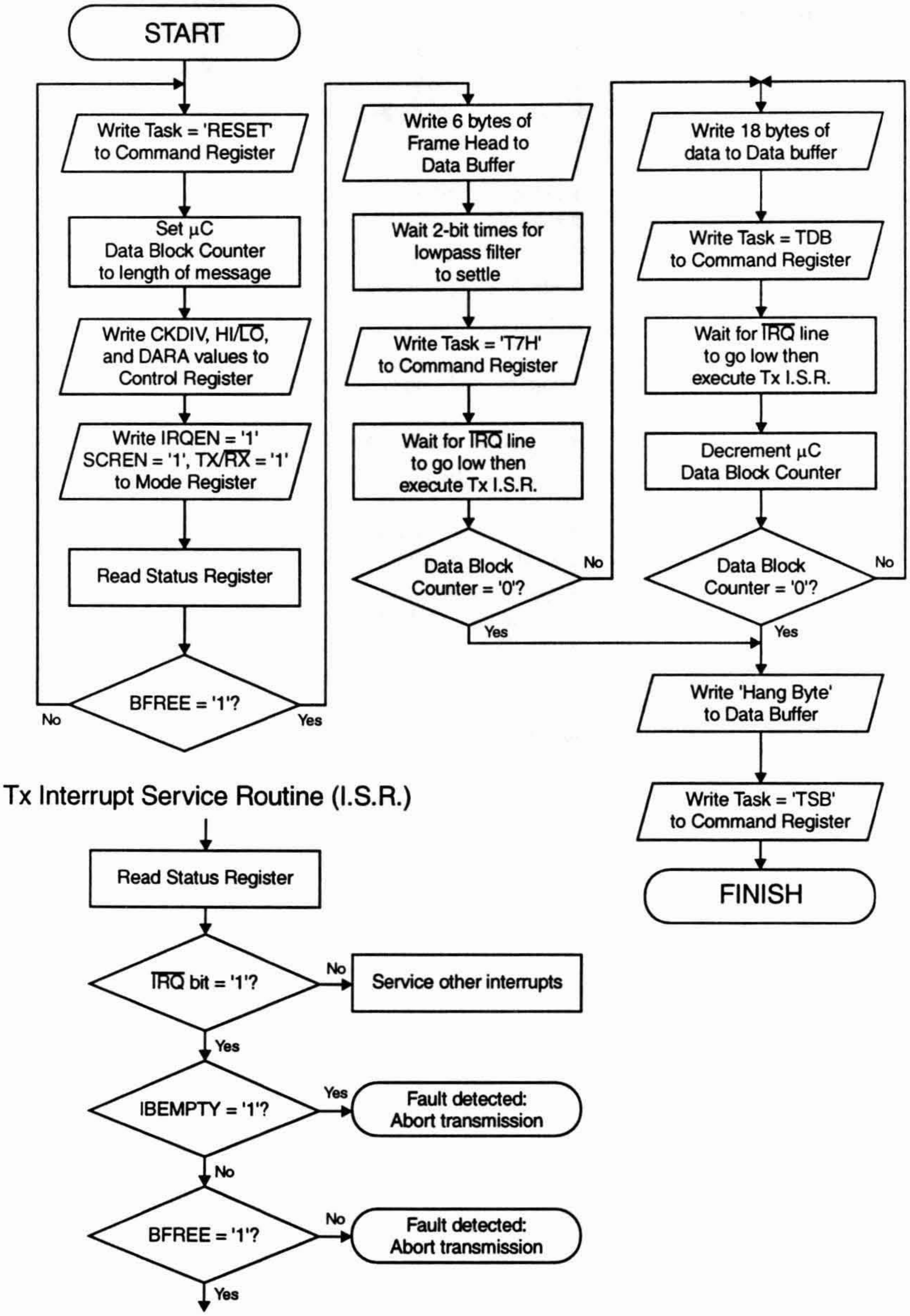

START
Write Task = 'RESET' to Command Register
Set µC Data Block Counter to length of message
Write CKDIV, HI/$\overline{LO}$, and DARA values to Control Register
Write IRQEN = '1' SCREN = '1', TX/$\overline{RX}$ = '1' to Mode Register
Read Status Register
BFREE = '1'?
No
Yes
Write 6 bytes of Frame Head to Data Buffer
Wait 2-bit times for lowpass filter to settle
Write Task = 'T7H' to Command Register
Wait for $\overline{IRQ}$ line to go low then execute Tx I.S.R.
Data Block Counter = '0'?
No
Yes
Write 18 bytes of data to Data buffer
Write Task = TDB to Command Register
Wait for $\overline{IRQ}$ line to go low then execute Tx I.S.R.
Decrement µC Data Block Counter
Data Block Counter = '0'?
No
Yes
Write 'Hang Byte' to Data Buffer
Write Task = 'TSB' to Command Register
FINISH
Tx Interrupt Service Routine (I.S.R.)
Read Status Register
$\overline{IRQ}$ bit = '1'?
No
Service other interrupts
Yes
IBEMPTY = '1'?
Yes
Fault detected: Abort transmission
No
BFREE = '1'?
No
Fault detected: Abort transmission
Yes

Figure 14: Transmit Process Flow Chart

5.2 Receive Frame Example

If the device is required to decode a Mobitex™ Frame the following control signals should be issued to the modem, assuming the device is initially not in powersave, PLLBW, LEVRES, SCREN are set as required, TX/$\overline{\text{RX}}$ bit is set to '0', the Frame Sync bytes have not been set and the carrier has been detected, or a Frame Head is expected:

1. 2 Frame Sync bytes are loaded.
2. 2 bits after the carrier has been detected, an LFSB task is loaded, along with setting the AQLEV and AQBC bits, to initiate the level acquisition and bit clock extraction sequences.
3. Device interrupts host µC with $\overline{\text{IRQ}}$ when 2nd byte is read from Data Buffer.
4. Status Register is read, 12 bits later task is set to SFH to search for a Mobitex™ Frame Head.
5. Device will interrupt host µC with $\overline{\text{IRQ}}$ when valid Frame Sync is detected and header bytes decoded.
6. Host µC reads Status Register, checks MO/$\overline{\text{BA}}$ and CRCFEC bit and reads out 2 Frame Head control bytes.
7. Host µC sets the task to RDB to receive a Mobitex™ Data Block.
8. Device will interrupt host µC with $\overline{\text{IRQ}}$ when the Data Block has been received and the CRC has been calculated.
9. Host µC reads Status Register, checks CRC validity and reads 18 Data Block bytes. The Data Quality Register can also be read to obtain the received S/N level.
10. Host µC sets task if more information is expected:
    GOTO '4' if last Data Block and another Frame Head are expected.
    GOTO '7' if another Mobitex™ Data Block is expected.

If the last Data Block has been decoded and no further information is expected, then the task bits do not need to be set, as the device will automatically select the idle state.

A top level flowchart of the receive process is shown in Figure 15.

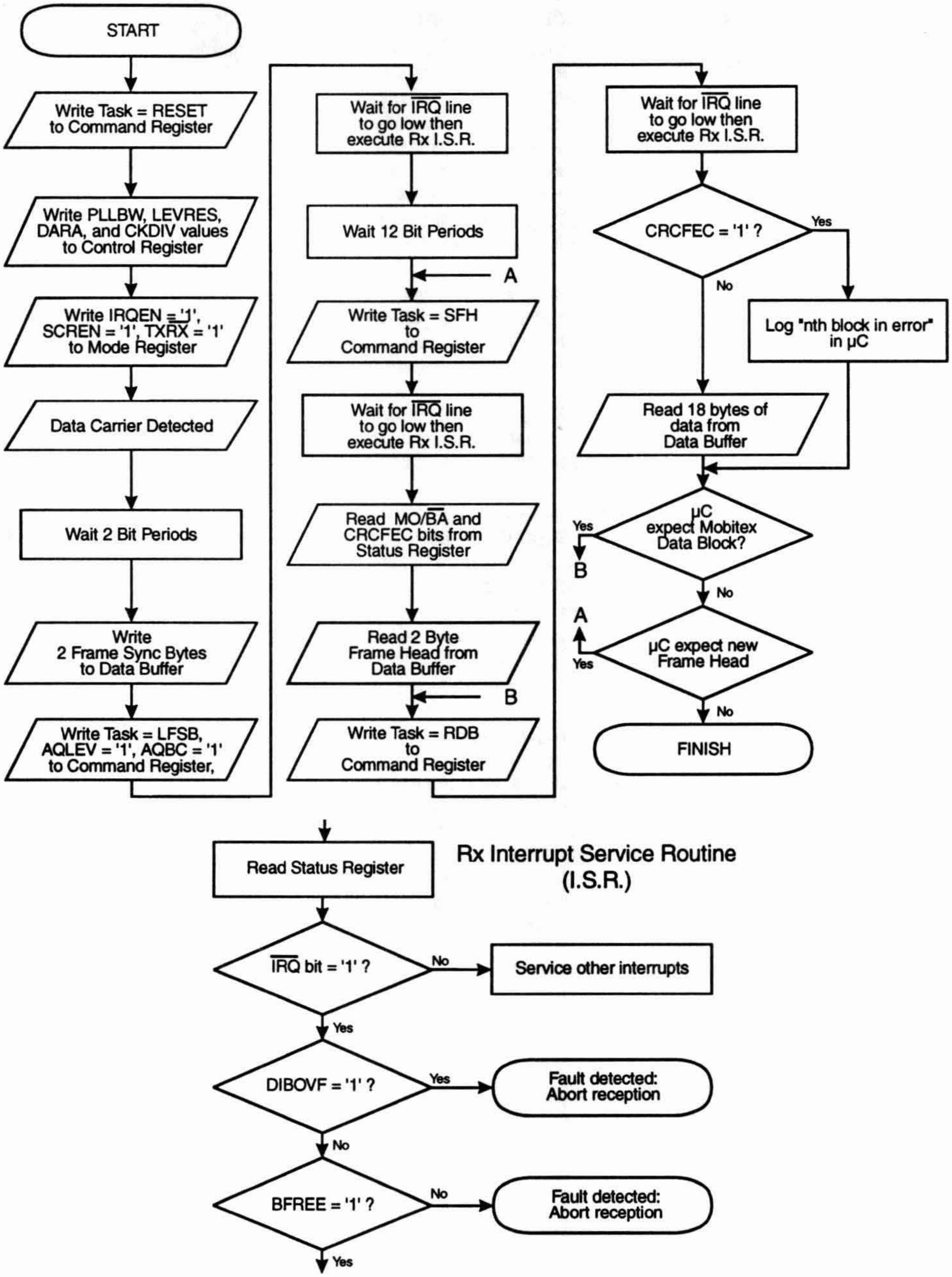

START
Write Task = RESET to Command Register
Write PLLBW, LEVRES, DARA, and CKDIV values to Control Register
Write IRQEN = '1', SCREN = '1', TXRX = '1' to Mode Register
Data Carrier Detected
Wait 2 Bit Periods
Write 2 Frame Sync Bytes to Data Buffer
Write Task = LFSB, AQLEV = '1', AQBC = '1' to Command Register,
Wait for $\overline{IRQ}$ line to go low then execute Rx I.S.R.
Wait 12 Bit Periods
A
Write Task = SFH to Command Register
Wait for $\overline{IRQ}$ line to go low then execute Rx I.S.R.
Read MO/$\overline{BA}$ and CRCFEC bits from Status Register
Read 2 Byte Frame Head from Data Buffer
B
Write Task = RDB to Command Register
Wait for $\overline{IRQ}$ line to go low then execute Rx I.S.R.
CRCFEC = '1' ?
Yes
No
Log "nth block in error" in µC
Read 18 bytes of data from Data Buffer
µC expect Mobitex Data Block?
Yes
B
No
A
µC expect new Frame Head
Yes
No
FINISH
Read Status Register
Rx Interrupt Service Routine (I.S.R.)
$\overline{IRQ}$ bit = '1' ?
No
Service other interrupts
Yes
DIBOVF = '1' ?
Yes
Fault detected: Abort reception
No
BFREE = '1' ?
No
Fault detected: Abort reception
Yes

Figure 15: Receive Process Flow Chart

5.3 Clock Extraction and Level Measurement Systems

The modem needs to make accurate measurements of the received signal amplitude, DC offset and bit timing to achieve reasonable error rates. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time.

However, in most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts. Also, the received baseband signal out of the radio's frequency discriminator will have a DC offset due to small differences between the receiver and transmitter reference oscillators and therefore their 'carrier' frequencies.

To allow for this situation, AQBC and AQLEV (Acquire Bit Clock and Level) commands are provided. When triggered, this causes the modem to follow an automatic sequence designed to perform these measurements as quickly as possible.

The AQLEV sequence always starts with a measurement of the average signal voltage over a period of 1 bit time. The sequence continues by measuring the positive going and negative going peaks of the signal. The attack and decay times used in this 'Lossy Peak Detect' mode are such that a sufficiently accurate measurement can be made within 16 bits of a ' 1100 ...' pattern (i.e. the bit sync sequence) to allow the bit clock extraction circuits to operate.

If SFH or SFS is set within 28 bit times of AQLEV the device will switch to the Residual setting when Frame Sync is found. If an SFH or SFS task is not set then the Residual setting will be active 30 bits after AQLEV was set. The Residual setting is that programmed in the LEVRES bits and is either 'Lossy Peak Detect', 'Peak Detect', 'Peak Averaging' or 'Hold'.

Note: For normal operation the LEVRES bits would only be set to 'hold' for the duration of a fade.

If SFH or SFS is set within 14 bit times of AQBC the device will switch to the Medium setting when Frame Sync is found. If an SFH or SFS task is not set then the Medium setting will be active 16 bits after AQBC was set. The PLLBW will change to the Residual setting 30 bits later.

The complete AQBC and AQLEV sequence, as illustrated in Figure 16, for the situation where the µC can detect the received carrier so that it knows when to issue the AQBC and AQLEV commands.

Note: Due to the delay through the Rx low pass filter, the AQBC and AQLEV sequences should not be started until approximately 2 bit times after the received carrier has been detected at the discriminator output. See Figure 16.

In a system where the host µC is not able to detect the received carrier, the AQBC and AQLEV sequences may be started at any time - possibly when no carrier is being received. However, in this case the clock and level acquisition will take longer since the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a DC offset. In this type of system, the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended - preferably by extending the Bit Sync sequence to 32 or even 48 bits.

Note: The clock extraction circuits work by detecting the timing of edges, i.e. a change from '0' to '1' or '1' to '0'. They will eventually fail if '1' or '0' is transmitted continuously. Similarly, the level measuring circuits require '00' and '11' bit pairs to be received at reasonably frequent intervals.

AQLEV Sequence

SFH or SFS is set up to 28 bits after AQLEV;

Frame Sync is being searched for:

- 1 bit of clamp.
- Lossy Peak detect until Frame Sync is detected.
- Residual setting.

SFH or SFS is not set; Frame Sync is not being searched for:

- 1 bit of clamp.
- 30 bits of Lossy Peak Detect.
- Residual setting.

AQBC Sequence

SFH or SFS is set up to 14 bits after AQBC;

Frame Sync is being searched for:

- 'Wide' setting until Frame Sync detected.
- 30 bits of 'Medium' setting.
- Residual setting.

SFH or SFS is not set; Frame Sync is not being searched for:

- 16 bits of 'Wide' setting.
- 30 bits of 'Medium' setting.
- Residual setting.

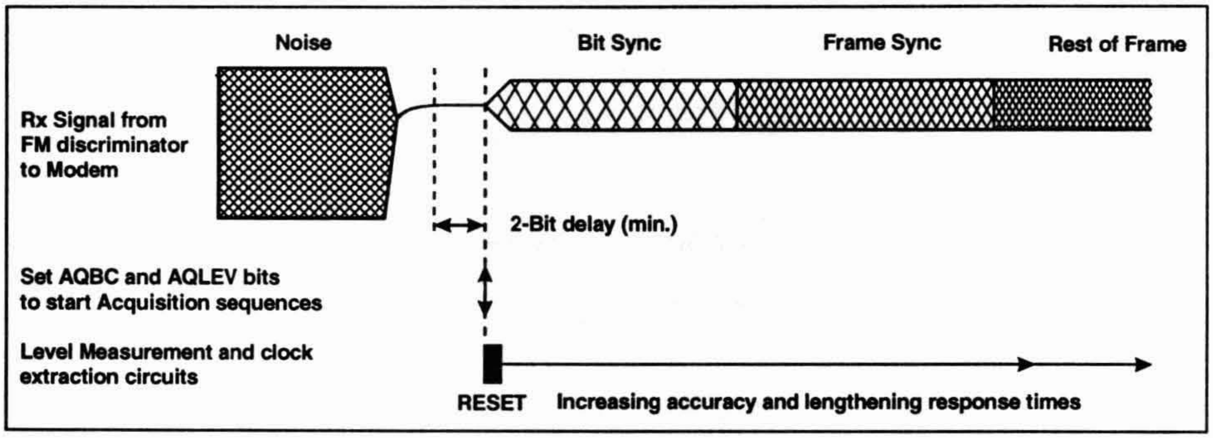

Noise
Bit Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
2-Bit delay (min.)
Set AQBC and AQLEV bits to start Acquisition sequences
Level Measurement and clock extraction circuits
RESET
Increasing accuracy and lengthening response times

Figure 16: Bit Clock and Level Acquisition Example

5.4 AC Coupling

For a practical circuit, when AC coupling from the modem's transmit output to the Frequency Modulator and between the receiver's Frequency Discriminator and the receive input of the modem may be desired. There are, however, two problems:.

1. AC coupling of the signal degrades the Bit Error Rate performance of the modem (at 8kbits/sec, without FEC, for different degrees of AC coupling). See Figure 17
2. Any AC coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As shown in Figure 18, the time for this step to decay to 37% of its original value is 'RC' when:

   RC = 1/(2 x π x the 3dB cut-off frequency of the RC network) and is 8 ms - or 64 bit times at 8kbits/sec for a 20Hz network.

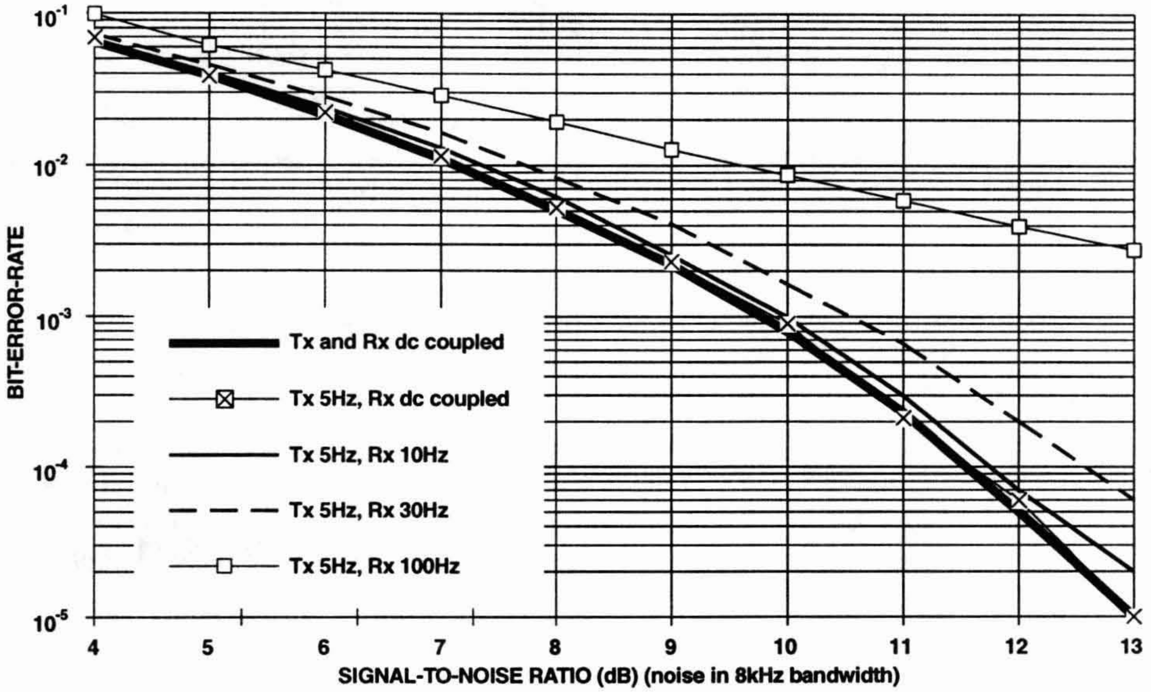
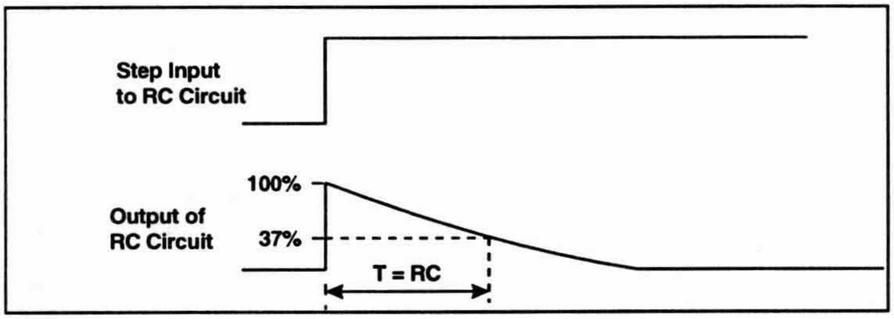


Figure 17: Typical Bit Error Rates (at 8kbits/sec, without FEC, for different degrees of AC decoupling)



Step Input to RC Circuit
Output of RC Circuit
100%
37%
T = RC

Figure 18: Decay Time - AC Coupling

Note: For these reasons the maximum 3dB cut-off frequencies would appear to be approximately 5Hz in the Tx path and 20Hz in the Rx path at 8kbits/sec.

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

RF channel spacing.

Allowable adjacent channel interference.

Bit rate.

Peak carrier deviation (modulation index).

Tx and Rx reference oscillator accuracy's.

Modulator and demodulator linearity.

Receiver IF filter frequency and phase characteristics.

Use of error correction techniques.

Acceptable error rate.

As a guide, 8kbits/sec can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2kHz peak for a repetitive ' 1100... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 1500Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput, by exploiting as much as possible, the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

Linearity, frequency and phase response of the Tx Frequency Modulator.

The bandwidth and phase response of the receiver's IF filters.

Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the received signal eye pattern, using the output of the frequency discriminator, gives a good indication of the overall transmitter/receiver performance.

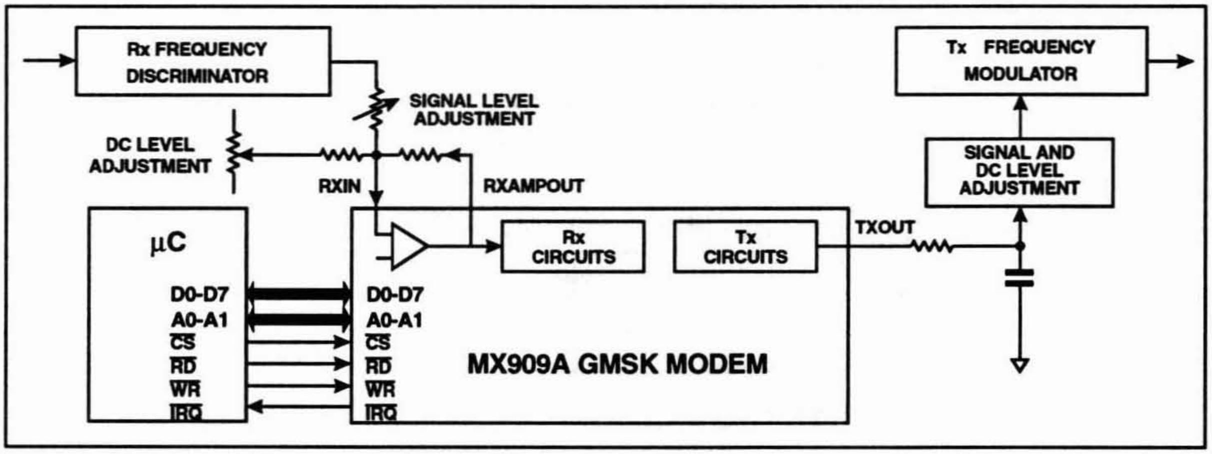

Rx FREQUENCY DISCRIMINATOR
SIGNAL LEVEL ADJUSTMENT
DC LEVEL ADJUSTMENT
RXIN
RXAMPOUT
µC
D0-D7
A0-A1
CS
RD
WR
IRQ
D0-D7
A0-A1
CS
RD
WR
IRQ
Rx CIRCUITS
Tx CIRCUITS
MX909A GMSK MODEM
TXOUT
Tx FREQUENCY MODULATOR
SIGNAL AND DC LEVEL ADJUSTMENT

Figure 19: Typical System Installation

6 Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (VDD - VSS)		3.0	5.5	V
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

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Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.096MHz, Bit Rate = 8k bits/sec, Noise Bandwidth = Bit Rate,

V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (not powersaved) (V_{DD} = 3.3V)	1		2.2	3.3	mA
I_{DD} (powersaved) (V_{DD} = 3.3V)	1		0.4	0.6	mA
I_{DD} (not powersaved)	1		3	4.5	mA
I_{DD} (powersaved)	1		0.9	1.4	mA
AC Parameters					
Tx Output					
TXOUT Impedance (not powersaved)	2		1.0	2.5	kΩ
TXOUT Impedance (powersaved)	2		300		kΩ
Signal Level	3	0.9	1.0	1.1	V_{P-P}
Tx Data Delay	4		4	6	bits
Rx Input					
RXIN Impedance (at 100Hz)		10.0			MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			500		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
Rx Data Delay	6		3.5		bits
Xtal/Clock Input					
'High' Pulse Width	7	40			ns
'Low' Pulse Width	7	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	8, 9	70%			V_{DD}
Input Logic "0" Level	8, 9			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	8, 9	−5.0		5.0	µA
Input Capacitance	8, 9		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	9	90%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	9,10			10%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	10			10	µA

Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance
3. For "1111000011110000..." bit sequence (output level is proportional to V_{DD}).
4. Measured between issuing first task after idle and the center of the first bit at TXOUT see Figure 7)
5. For optimum performance, measured at RXAMPOUT pin, for a "...11110000..." bit sequence
6. Measured between center of last bit of an Rx single byte or Frame Sync at RXIN and an IRQ interrupt to the host µC.
7. Timing for an external input to the CLOCK/XTAL pin.
8. $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{CS}}$, A0 and A1 pins.
9. D0 - D7 pins.
10. $\overline{\text{IRQ}}$ pin.

Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 4.096MHz, V_{DD} = 5.0V @ T_{AMB} = 25°C

µC Parallel Interface Timings ref (Figure 20)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{\text{CS}}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{\text{CS}}$ hold time		0			ns
t_{CSHI}	$\overline{\text{CS}}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ or $\overline{\text{RD}}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{\text{RD}}$ high to $\overline{\text{CS}}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{\text{CS}}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{\text{RD}}$ low	2			145	ns
t_{RL}	$\overline{\text{RD}}$ low time		200			ns
t_{RX}	$\overline{\text{RD}}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{\text{WR}}$ high to $\overline{\text{CS}}$ low time (read)		0			ns
t_{WL}	$\overline{\text{WR}}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

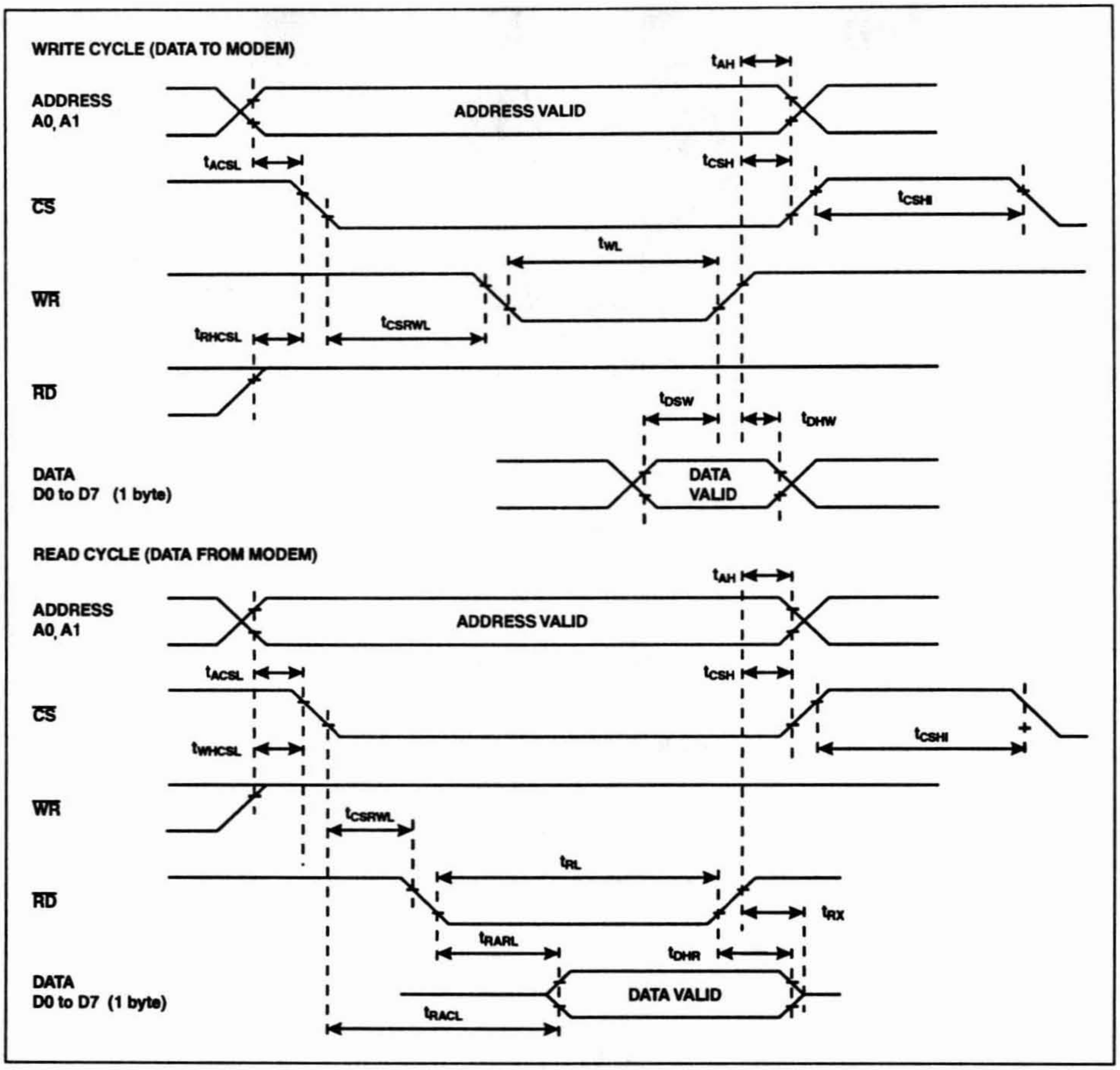
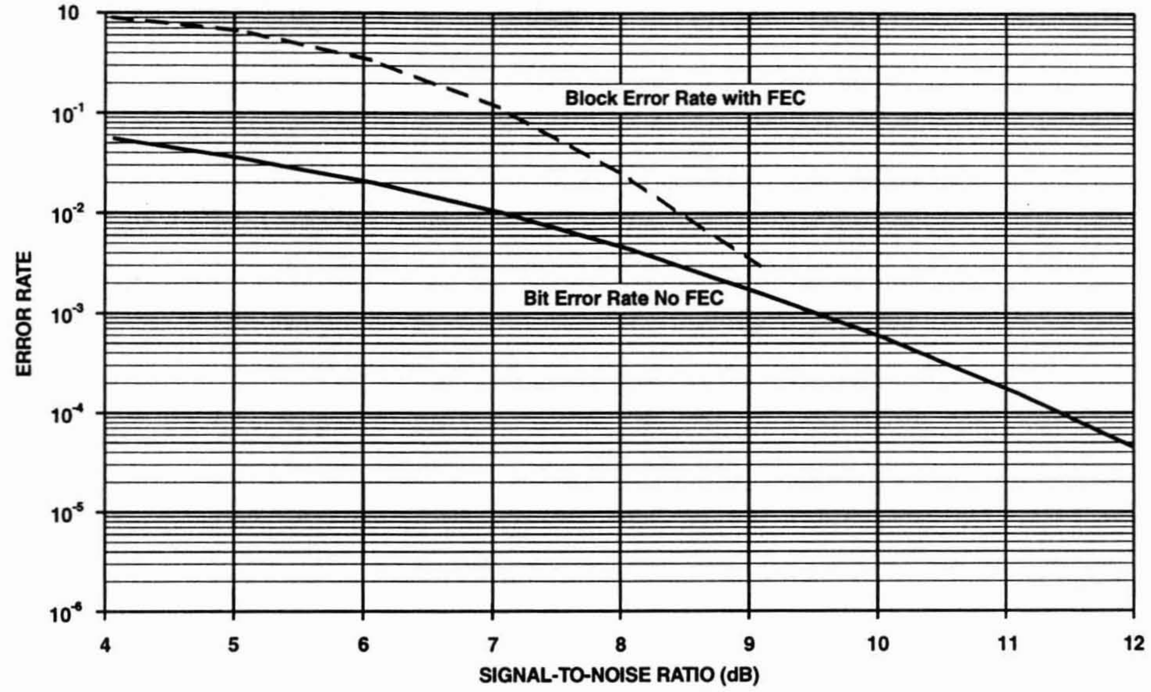

WRITE CYCLE (DATA TO MODEM)
ADDRESS A0, A1
ADDRESS VALID
t_{AH}
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{CSHI}
t_{WL}
$\overline{WR}$
t_{RHCSL}
t_{CSRWL}
$\overline{RD}$
t_{DSW}
t_{DHW}
DATA D0 to D7 (1 byte)
DATA VALID
READ CYCLE (DATA FROM MODEM)
ADDRESS A0, A1
ADDRESS VALID
t_{AH}
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{WHCSL}
t_{CSHI}
$\overline{WR}$
t_{CSRWL}
t_{RL}
$\overline{RD}$
t_{RX}
t_{RARL}
t_{DHR}
DATA D0 to D7 (1 byte)
DATA VALID
t_{RACL}

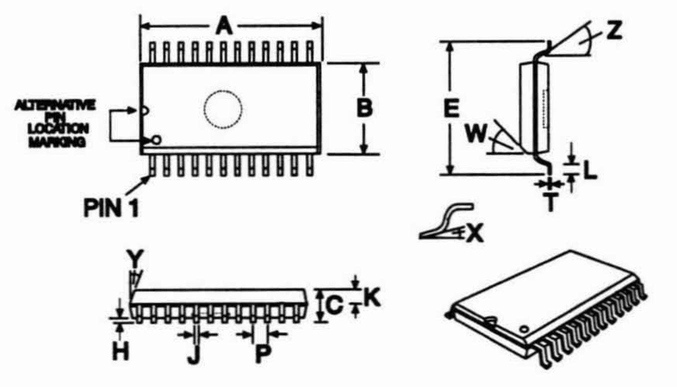
Figure 20: μC Parallel Interface Timing Diagram



NOTE: A block is deemed to be "In Error" if the CRC fails

Figure 21: Typical Bit Error Rate (noise in bit rate bandwidth)

6.2 Packaging

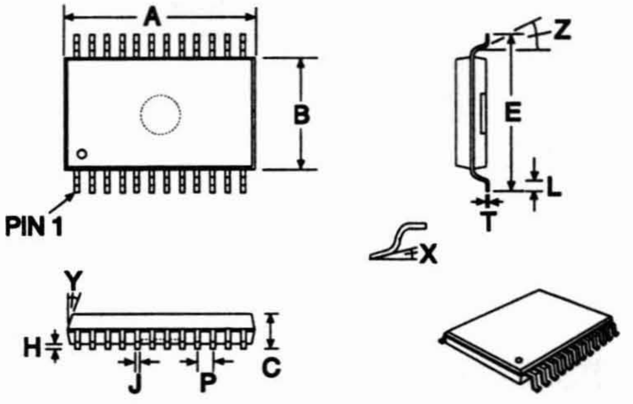


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 22: 24-pin SOIC Mechanical Outline : ***Order as part no. MX909ADW***

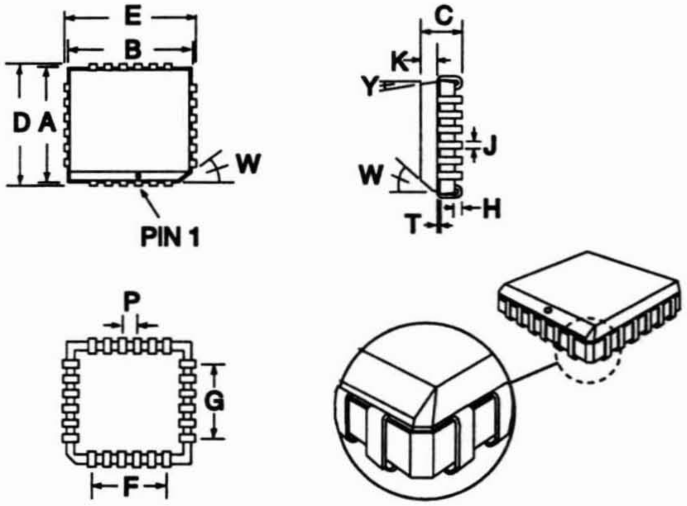


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 23: 24-PIN SSOP Mechanical Outline: ***Order as part no. MX909ADS***

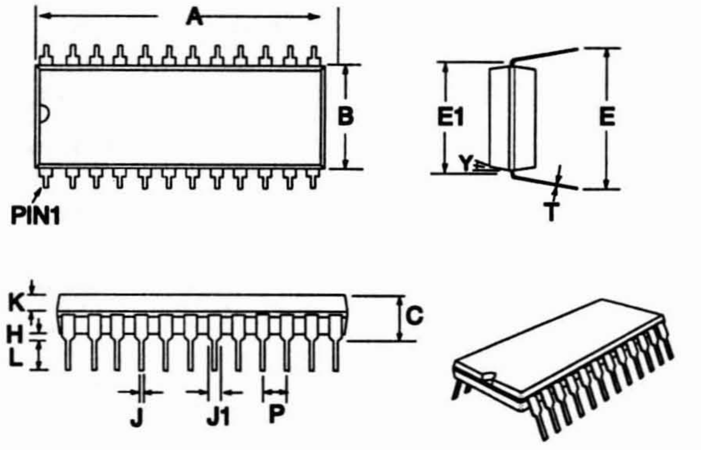


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 24: 24-pin PLCC Mechanical Outline: ***Order as part no. MX909ALH***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 25: 24-pin PDIP Mechanical Outline: ***Order as part no. MX909AP***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX919B 4-Level FSK Modem Data Pump

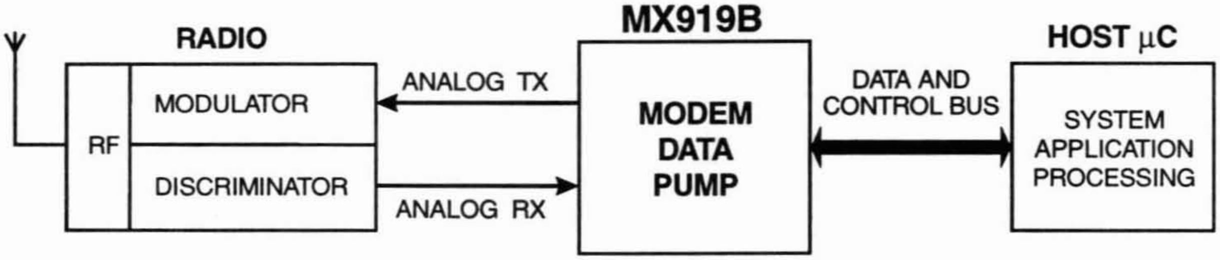
PRELIMINARY INFORMATION

Features

- **4-Level Root Raised Cosine FSK Modulation**
- **Half Duplex, 4800 to 19.2kbps**
- **Increase Channel Bit Rate/Hz**
- **Full Data Packet Framing**
- **Impulse and NRZ Signal Modes**
- **Enhanced Performance in Noisy Conditions**
- **Error Detection and Error Correction**
- **Low Power 3.3V/5.0V Operation**

Applications

- **Wireless Data Terminals**
- **Two Way Paging Systems**
- **Digital Radio Systems**
- **Wide Area Wireless Data Broadcasts**
- **Point to Point Wireless Data Links**



The MX919B is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host µC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over a wireless link.

The MX919B assembles application data received from the host µC, adds forward error correction (FEC) and error detection (CRC) information, and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating the radio transmitter.

In receive mode, the MX919B performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host µC. CRC detected residual uncorrected data errors will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX919B uses data block sizes and FEC/CRC suitable for applications where high speed transfer of data over narrow-band wireless links is required. The device is programmable to operate at standard bit rates from a wide range of Xtal/clock frequencies.

The MX919B may be used with a 3.0V to 5.5V power supply and is available in the following package styles: 24-pin SSOP (MX919BDS), 24-pin SOIC (MX919BDW), 24-pin PLCC (MX919BLH), and 24-pin PDIP (MX919BP).

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1 Block Diagram

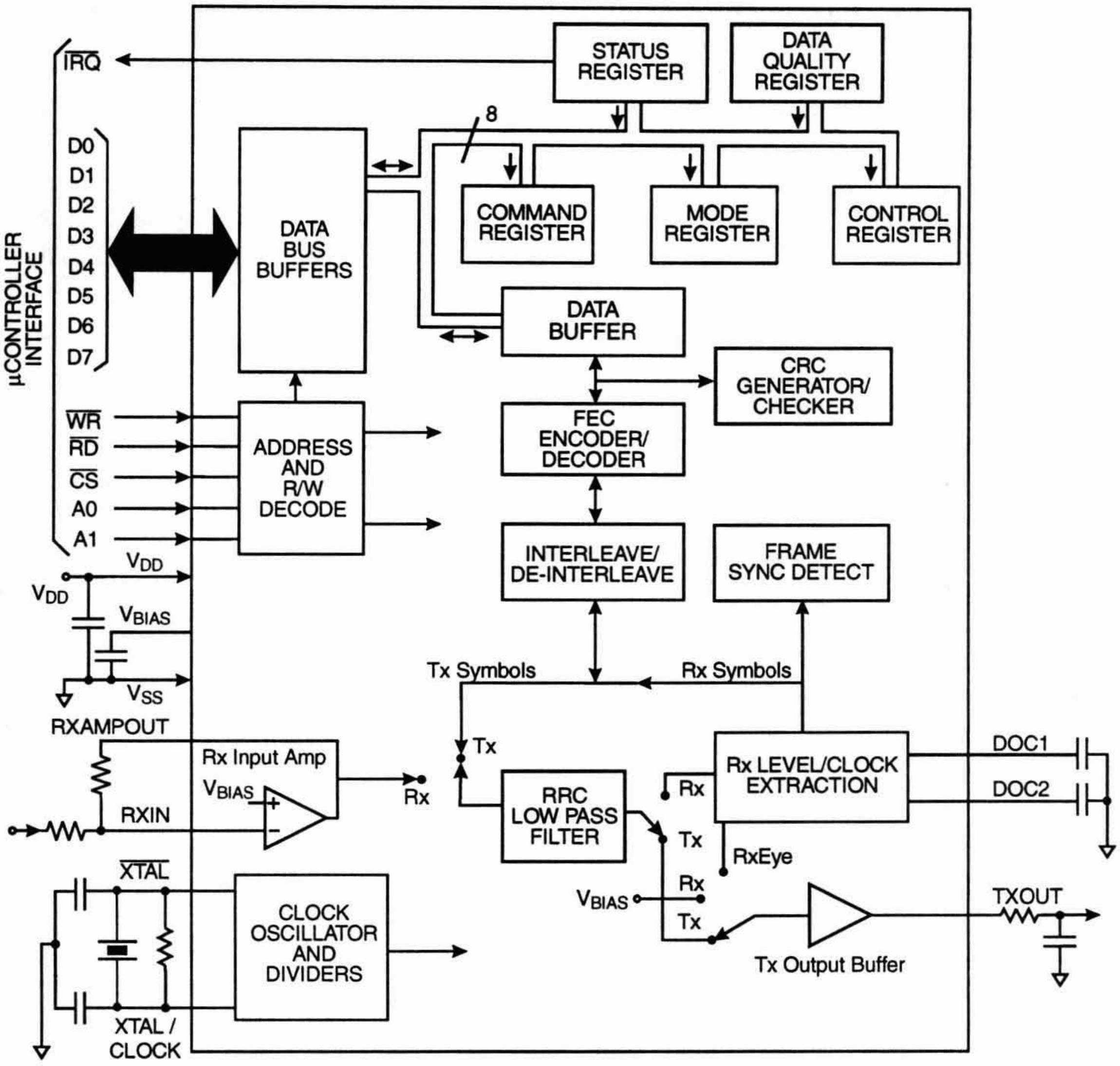
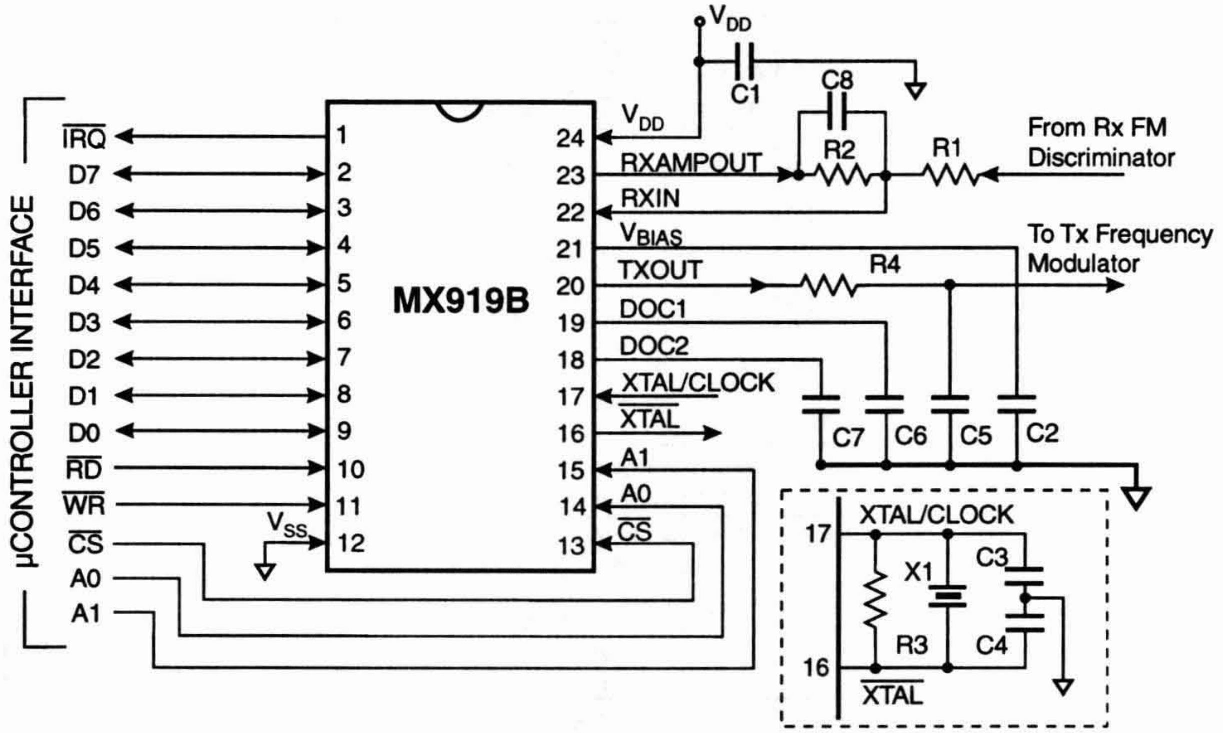

IRQ
D0
D1
D2
D3
D4
D5
D6
D7
µCONTROLLER INTERFACE
WR
RD
CS
A0
A1
VDD
VDD
VBIAS
VSS
RXAMPOUT
RXIN
XTAL
XTAL / CLOCK
STATUS REGISTER
DATA QUALITY REGISTER
8
DATA BUS BUFFERS
COMMAND REGISTER
MODE REGISTER
CONTROL REGISTER
DATA BUFFER
CRC GENERATOR/ CHECKER
FEC ENCODER/ DECODER
ADDRESS AND R/W DECODE
INTERLEAVE/ DE-INTERLEAVE
FRAME SYNC DETECT
Tx Symbols
Rx Symbols
Tx
Rx Input Amp
VBIAS
Rx
RRC LOW PASS FILTER
Rx LEVEL/CLOCK EXTRACTION
Rx
Tx
RxEye
Rx
Tx
VBIAS
Tx Output Buffer
DOC1
DOC2
TXOUT
CLOCK OSCILLATOR AND DIVIDERS

Figure 1: Block Diagram

2 Signal List

Pin No.	Signal	Type	Description
1	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{XTAL}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for an external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry held at V_{DD} /2. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

3 External Components



V_{DD}
C1
C8
R2
R1
From Rx FM Discriminator
$\overline{IRQ}$
D7
D6
D5
D4
D3
D2
D1
D0
$\overline{RD}$
$\overline{WR}$
$\overline{CS}$
A0
A1
µCONTROLLER INTERFACE
V_{SS}
1
2
3
4
5
6
7
8
9
10
11
12
MX919B
24
23
22
21
20
19
18
17
16
15
14
13
V_{DD}
RXAMPOUT
RXIN
V_{BIAS}
TXOUT
DOC1
DOC2
XTAL/CLOCK
$\overline{XTAL}$
A1
A0
$\overline{CS}$
R4
To Tx Frequency Modulator
C7
C6
C5
C2
XTAL/CLOCK
17
X1
C3
R3
C4
16
$\overline{XTAL}$

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±5%
R3		1MΩ	±20%
R4		100kΩ	±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	3		±20%

Component	Notes	Value	Tolerance
C4	3		±20%
C5	4		±5%
C6	5		±20%
C7	5		±20%
C8	4		±5%
X1	2, 3		

Recommended External Component Notes:

1. See Section 4.1.10.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. Crystal frequency tolerances are discussed in Section 4.5.3.4.
4. Values C5 and C8 should be equal to 750,000 / symbol rate, e.g.
5. Values C6 and C7 should be equal to 50,000 / symbol rate, e.g.

Symbol Rate	C5 and C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

Symbol Rate	C6 and C7
2400 symbols/second	0.022µF
4800 symbols/second	0.01µF
9600 symbols/second	4700pF

4 General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$), and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address, and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

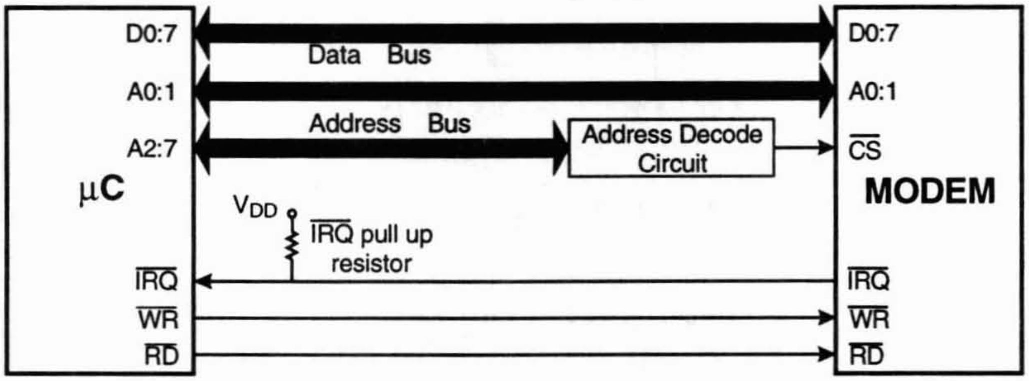


Figure 3: Typical Modem µC connections

4.1.3 Status and Data Quality Registers

Two, 8-bit registers which the µC can read, to determine the status of the modem and received data quality.

4.1.4 Command, Mode, and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

A 12-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in the transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-Interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give 0.2 x V_{DD} volts$_{P\text{-}P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see Section 5.4), otherwise the DC level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} ($V_{DD}/2$).

4.1.11 RRC Low Pass Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$H(f) = 1 \text{ for } 0 \le f < \frac{1-b}{2T}$$

$$H(f) = \sqrt{\frac{1}{2} - \frac{\sin\frac{(\pi Tf - \frac{\pi}{2})}{b}}{2}} \quad \text{for } \frac{1-b}{2T} \le f \le \frac{1+b}{2T}$$

$$H(f) = 0 \text{ for } f > \frac{1+b}{2T}$$

$$\text{Where} \quad b = 0.2, \quad T = \frac{1}{\text{symbol rate}}$$

This frequency response is illustrated in Figure 5 and Figure 6.

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels. The input applied to the RRC Tx filter may be impulses or full-width symbols depending on the setting of the Command Register TXIMP bit. See Section 4.7

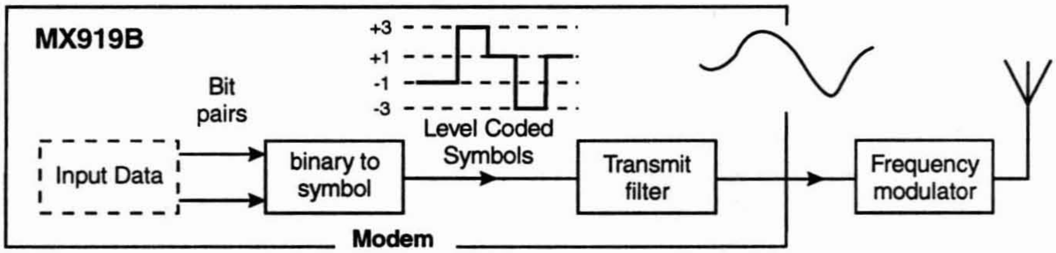


Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in Tx Mode

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols. The equalization characteristics are determined by the setting of the Command Register TXIMP bit.

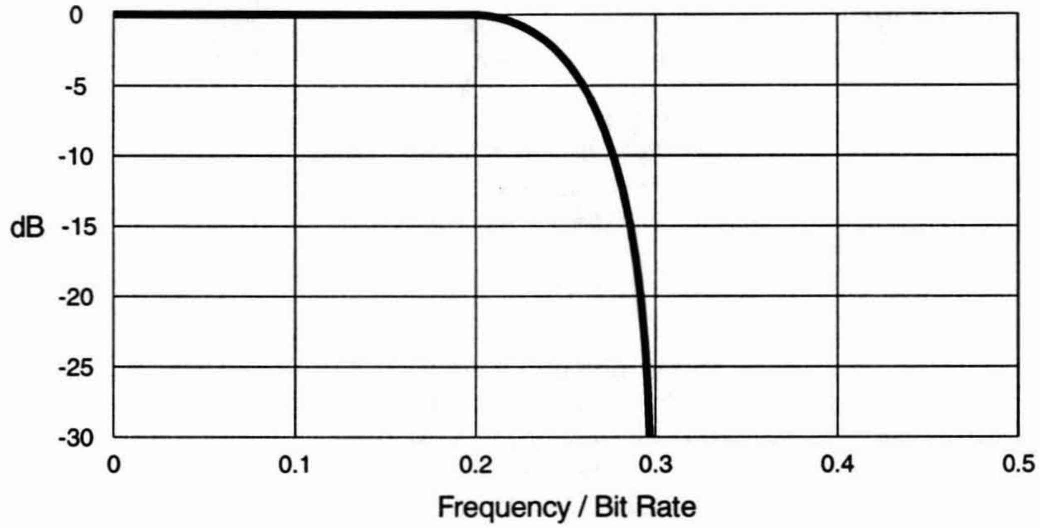


Figure 5: RRC Filter Frequency Response vs. Bit Rate (including the external RC filter R4/C5)

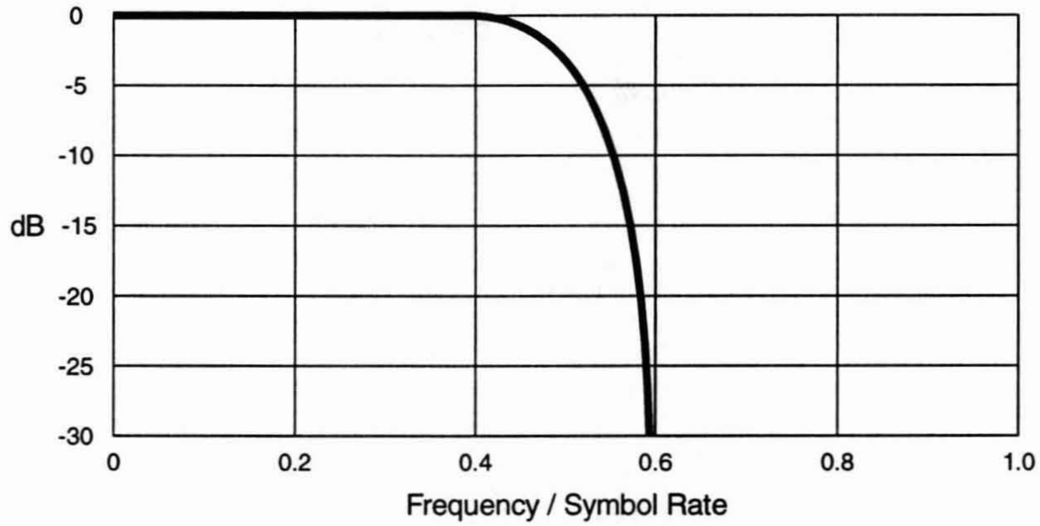


Figure 6: RRC Filter Frequency Response vs. Symbol Rate (including the external RC filter R4/C5)

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}, unless the RXEYE bit of the Control Register is '1', in which case it is connected to the received signal. When changing from Rx to Tx mode, the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any DC level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS}. It is approximately 0.2 x V_{DD} volts$_{P-P}$ for a continuous '+3 +3 -3 -3...' pattern with TXIMP = 0. For typical Tx Eye Diagrams refer to Section 4.7, Figure 17 and Figure 18. For typical Rx Eye Diagrams refer to Section 4.5.4.4, Figure 14.

A capacitor may be placed in series with the input to the frequency modulator if AC coupling is desired. See Section 5.4.

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and DC offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

The capacitors C6 and C7 are driven from a very high impedance source so any measurement of the voltages on the DOC pins must be made via high input impedance (MOS input) voltage followers to avoid disturbance of the level measurement circuits.

Further details of the level and clock extraction functions are given in Section 5.3.

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4, and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4, and R3 should not be installed.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, and Interleaving. Details of the message formats handled by the modem are provided in Section 4.4, Figure 7, and Figure 8.

To reduce the processing load on the associated µC, the MX919B modem has been designed to perform as much of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) searching for and synchronizing onto the Frame Preamble. In normal operation, the modem will only require servicing by the µC once per received or transmitted block.

Therefore, to transmit a block, the controlling µC needs only to load the unformatted 'raw' binary data into the modem's Data Block Buffer, then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding), and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary, perform Forward Error Correction, and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data using the T4S, T24S, and R4S tasks as described in Sections 4.3 and 4.5.2. These tasks are normally used for the transmission of Symbol and Frame Synchronization sequences. These tasks may also be used for the transmission and reception of special test patterns or special data formats. In such a case, care should be taken to ensure that the transmitted TXOUT signal contains enough level and timing information for the receiving modem's level and clock extraction circuits to function correctly.
See Section 5.3.

4.3 Binary to Symbol Translation

Although the over-air signal, and therefore the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct way: (simplest form) - converts between 2 binary bits and a single symbol.

SYMBOL	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

Accordingly, 1 byte = 4 symbols = 8 bits, and one byte translates to four symbols for the T4S and R4S tasks and six bytes translates to twenty-four symbols for the T24S task described in Section 4.5.2.

	MSB							**LSB**
Bits:	7	6	5	4	3	2	1	0
Symbols:	a		b		c		d	
	sent first						sent last	

2. FEC way: (more complicated) - essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, RHB, and RILB described in Section 4.5.2.

4.4 Frame Structure

Figure 7 shows how an over-air message frame may be constructed from a sequence of: a Symbol Sync pattern (preamble), a Frame Sync pattern, and one or more 'Header', 'Intermediate' or 'Last' blocks.

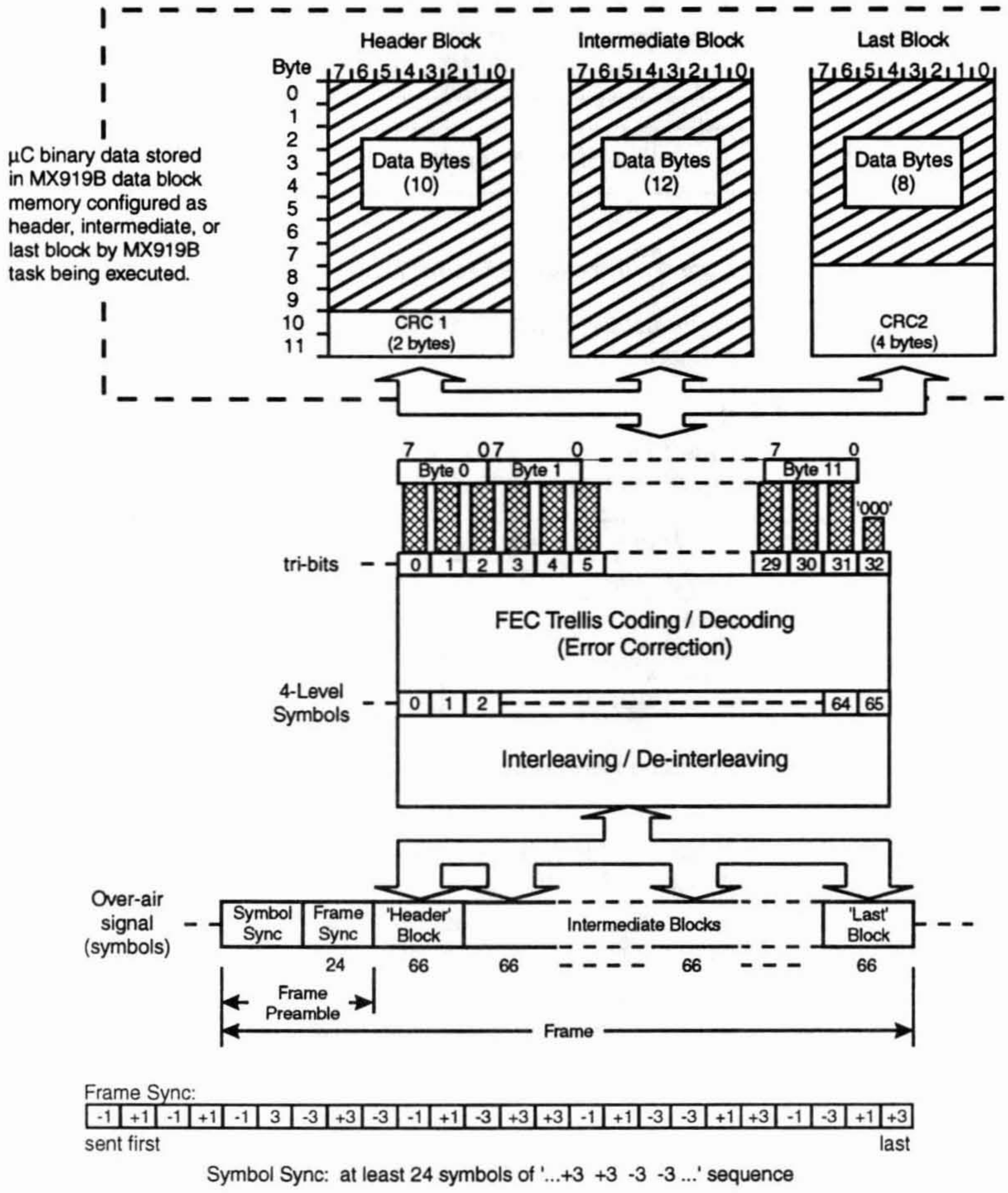

Header Block
Intermediate Block
Last Block
Byte
7 6 5 4 3 2 1 0
0 1 2 3 4 5 6 7 8 9 10 11
µC binary data stored in MX919B data block memory configured as header, intermediate, or last block by MX919B task being executed.
Data Bytes (10)
Data Bytes (12)
Data Bytes (8)
CRC 1 (2 bytes)
CRC2 (4 bytes)
7 0 7 0 7 0
Byte 0
Byte 1
Byte 11
'000'
tri-bits
0 1 2 3 4 5 29 30 31 32
FEC Trellis Coding / Decoding (Error Correction)
4-Level Symbols
0 1 2 64 65
Interleaving / De-interleaving
Over-air signal (symbols)
Symbol Sync
Frame Sync
'Header' Block
Intermediate Blocks
'Last' Block
24 66 66 66 66
Frame Preamble
Frame
Frame Sync:
-1 +1 -1 +1 -1 3 -3 +3 -3 -1 +1 -3 +3 +3 -1 +1 -3 -3 +1 +3 -1 -3 +1 +3
sent first
last
Symbol Sync: at least 24 symbols of '...+3 +3 -3 -3 ...' sequence

Figure 7: Over-Air Signal Format

The 'Header' block is self-contained and includes its own checksum (CRC1). It would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any), and miscellaneous control information. The number of following blocks (if any) is required to allow the Rx device software to expect the Last Block and interpret it as a Last Block rather than an Intermediate Block. There is no other indicator to differentiate a Last Block and an Intermediate Block.

The 'Intermediate' block(s) contain only data, the checksum for all of the data in the 'Intermediate' and 'Last' blocks (CRC2) being contained at the end of the 'Last' block.

This arrangement, while efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In such conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so blocks that are received correctly can be identified as such, and do not need to be re-transmitted. These, and some other possible frame structures, are shown in Figure 8.

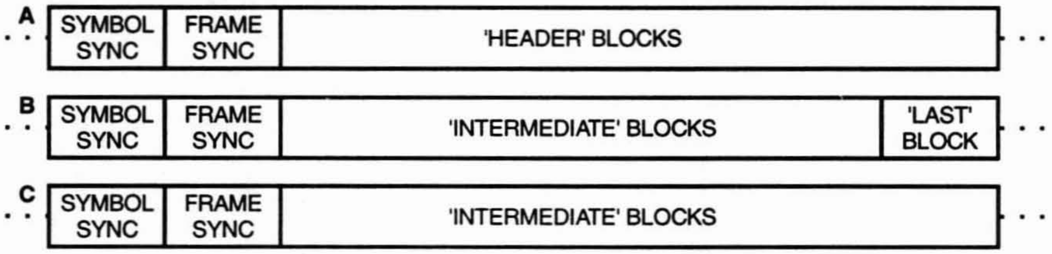


Figure 8: Alternative Frame Structures

The MX919B performs the entire block formatting and de-formatting required to convert data between µC binary form and Over-Air as shown in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4 write only 8-bit registers, shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see Section 6.1.5.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

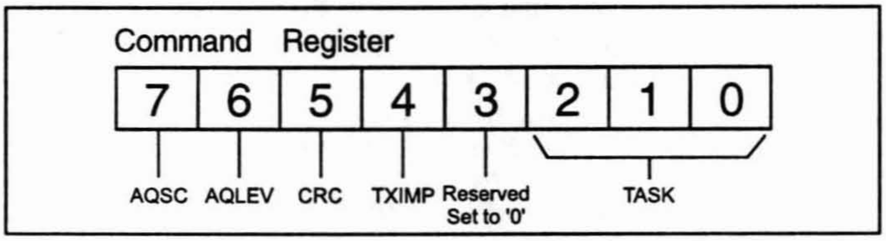
To the µC, the Data Block Buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode, the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific task as indicated by the TASK bits and modified by the AQSC, AQLEV, CRC, and TXIMP bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode, the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode, the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, otherwise these received symbols are ignored.

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQSC bit set to '1'.

The use of the symbol clock acquisition sequence is described in Section 5.3.

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The use of the level measurement acquisition sequence (AQLEV) is described in Section 5.3.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different initial states of the CRC1 and CRC2 checksum generators. When this bit is set to '0', the CRC generators are initialized to 'all ones' as for CCITT X25 CRC calculations. When this bit is set to '1', the CRC generators are initialized to 'all zeros'. Setting this bit to '0' provides compatibility with the MX919, a prior member of the MX919 device family. Other systems may set this bit as required. Note: This bit must be set correctly every time the Command Register is written to.

4.5.2.4 Command Register B4: TXIMP - Tx Level/Impulse Shape

This bit allows the user to choose between two transmit symbol waveform shapes as described in Section 4.7. Note: This bit must be set correctly every time the Command Register is written to.

4.5.2.5 Command Register B3 - Reserved

This bit should always be set to '0'.

4.5.2.6 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE (Buffer Free) bit of the Status Register to '0'.
>
> Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.
>
> Once all of the data has been transferred from the Data Block Buffer, the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write the next task and its associated data to the modem while the modem is still transmitting the data from its previous task.

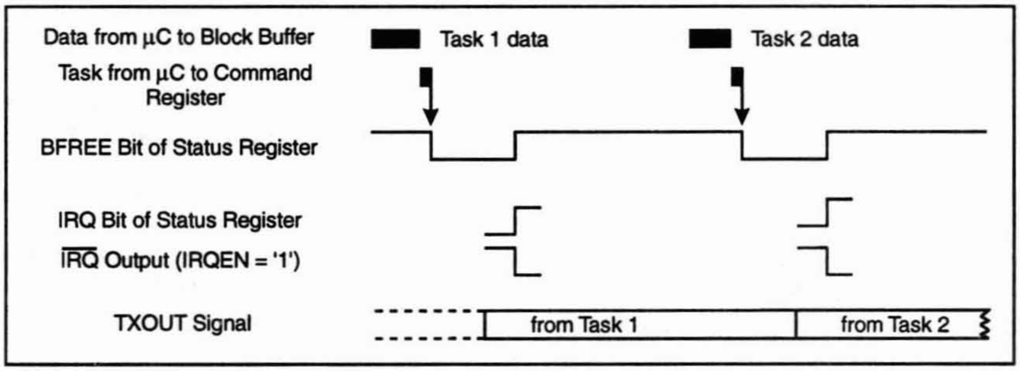

Data from µC to Block Buffer
Task 1 data
Task 2 data
Task from µC to Command Register
BFREE Bit of Status Register
IRQ Bit of Status Register
$\overline{IRQ}$ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE bit of the Status Register to '0'.
>
> Wait until enough received symbols are in the De-interleave Buffer.
>
> Decode them as needed and transfer the resulting binary data to the Data Block Buffer
>
> Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way, the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

Ref. Figure 9 and Figure 10		Task	Typical (bit-times)
t_1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t_2	Time from application of first bit of task to TX Low Pass Filter until BFREE goes to a logic 1	T7H	36
		TQB	24
		TDB	20
		TSB	1
t_3	Time to transmit all bits of task	T7H	56
		TQB	32
		TDB	240
		TSB	8
t_4	Max time allowed from BFREE going to a logic 1 for next task (and data) to be written to the modem	T7H	18
		TQB	6
		TDB	218
		TSB	6
t_5	Time to receive all bits of task	SFH	56
		R3H	24
		RDB	240
		RSB	8
t_6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem	SFH	14
		R3H	18
		RDB	218
		RSB	6
t_7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1'	Any	1

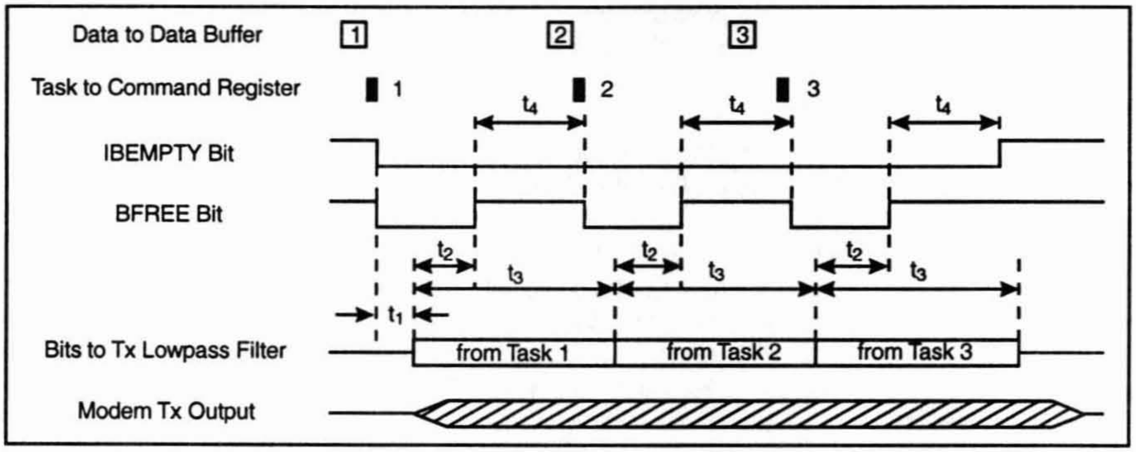

Data to Data Buffer
1
2
3
Task to Command Register
1
2
3
t4
t4
t4
IBEMPTY Bit
BFREE Bit
t2
t3
t2
t3
t2
t3
t1
Bits to Tx Lowpass Filter
from Task 1
from Task 2
from Task 3
Modem Tx Output

Figure 9: Transmit Mode Timing Diagram

4.5.2.10 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µC should be able to tell from the 'Header' block how many blocks are in the frame and when to expect the 'Last' block).

In each case, it will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received, then the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum.

4.5.2.11 SFS: Search for Frame Sync

This task causes the modem to search the received signal for a 24-symbol sequence which matches the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' to indicate to the µC that it should write the next task to the Command Register.

4.5.2.12 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register are then set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by a SFS task.

Note: It is possible to construct message formats, which do not rely on the block formatting of the THB, TIB, and TLB tasks. This can be accomplished by using T4S or T24S tasks to transmit and R4S to receive the user's data. One should be aware, that the receive level and timing measurement circuits need to see a reasonably 'random' distribution of all four possible symbols in the received signal to operate correctly. Accordingly, binary data may benefit from scrambling before transmission if it is not reasonably 'random' to start with.

4.5.2.13 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data needs to be written to the Data Block Buffer to transmit the MX919B Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				**Values written to Data Block Buffer**		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
+3	+3	-3	-3	Byte 5:	11110101	F5

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

4.5.2.14 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.15 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Intermediate' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Last' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.17 T4S: Transmit 4 Symbols

This command is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

4.5.2.18 RESET: Stop any current action

This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note: Due to delays in the transmit filter, it will take several symbol times for any change to appear at the TXOUT pin.

4.5.2.19 Task Timing

The following table and figures describe the duration of tasks and timing sequences for Tx and Rx operation.

		Task	Time (symbol times)
t_1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t_2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1'	T24S THB/TIB/TLB T4S	5 16 0
t_3	Time to transmit all symbols of the task	T24S THB/TIB/TLB T4S	24 66 4
t_4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S THB/TIB/TLB T4S	18 49 3
t_5	Time to receive all symbols of task	SFS SFSH RHB/RILB R4S	24 (minimum) 90 (minimum) 66 4
t_6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS SFSH RHB/RILB R4S	21 21 49 3
t_7	Maximum time from the last bit of the task entering the de interleave circuit to BFREE going to a logic '1' (high)	Any	1

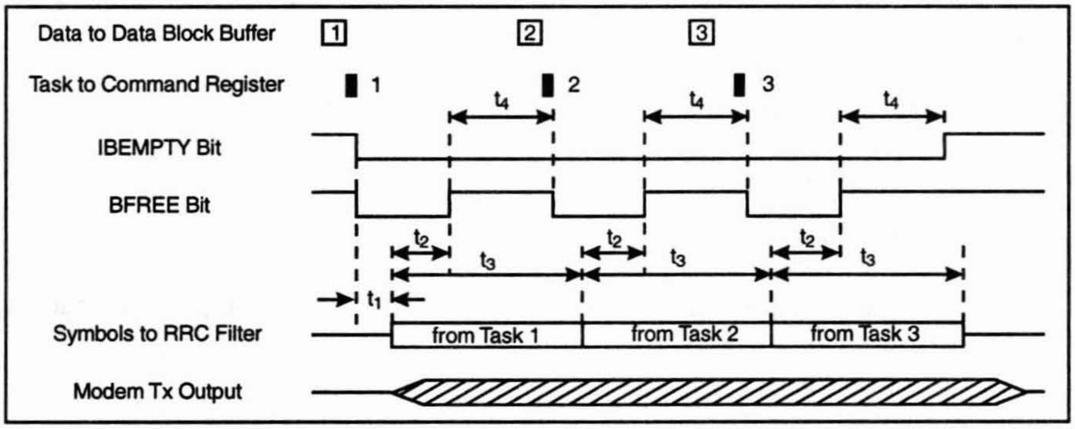

Data to Data Block Buffer
1
2
3
Task to Command Register
1
2
3
t4
t4
t4
IBEMPTY Bit
BFREE Bit
t2
t3
t2
t3
t2
t3
t1
Symbols to RRC Filter
from Task 1
from Task 2
from Task 3
Modem Tx Output

Figure 11: Transmit Task Timing Diagram

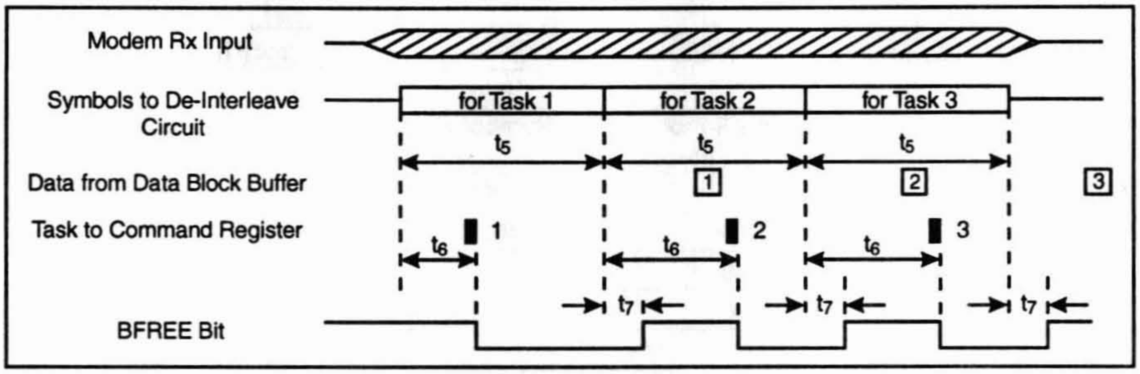

Modem Rx Input
Symbols to De-Interleave Circuit
for Task 1
for Task 2
for Task 3
t5
t5
t5
Data from Data Block Buffer
1
2
3
Task to Command Register
t6
1
t6
2
t6
3
t7
t7
t7
BFREE Bit

Figure 12: Receive Task Timing Diagram

4.5.2.20 RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below:

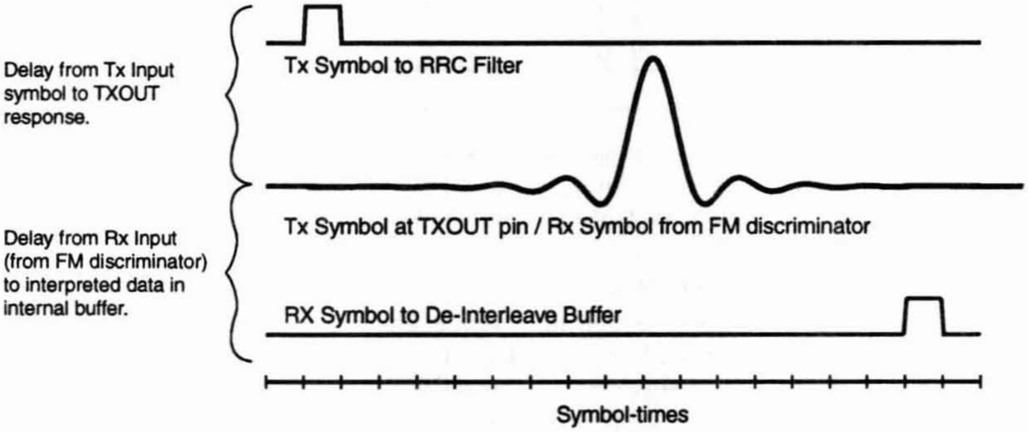
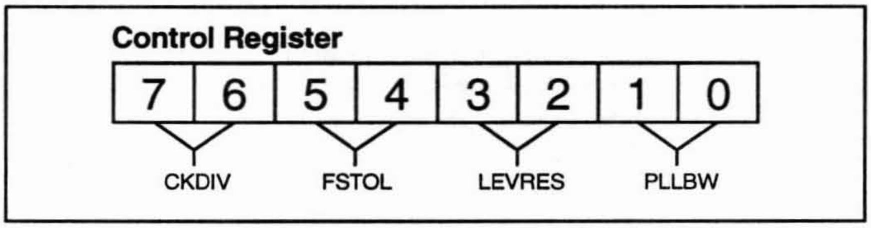

Delay from Tx Input symbol to TXOUT response.
Tx Symbol to RRC Filter
Delay from Rx Input (from FM discriminator) to interpreted data in internal buffer.
Tx Symbol at TXOUT pin / Rx Symbol from FM discriminator
RX Symbol to De-Interleave Buffer
Symbol-times

Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction, signal level measurement circuits, and the Frame Sync pattern recognition tolerance to inexact matches.


Control Register
7
6
5
4
3
2
1
0
CKDIV
FSTOL
LEVRES
PLLBW

4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{\text{XTAL}}$ pin, therefore determining the nominal symbol rate. Because each symbol represents two bits, bit rates are 2x the symbol rates. The table below shows how symbol rates of 2400/4800/9600 symbols/sec (4800/9600/19200bps) may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	**B6**	**Division Ratio: Xtal Frequency/Symbol Rate**	**Symbol Rate (symbols/sec) / Bit Rate (bps)**		
0	0	512	4800/9600	9600/19200	
0	1	1024	2400/4800	4800/9600	9600/19200
1	0	2048		2400/4800	4800/9600
1	1	4096			2400/4800

Note: Device operation is not guaranteed below 2400 symbols/sec (4800bps) or above 9600 symbols/sec (19200bps).

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance to Inexact Matches

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches. A setting of '4 mismatches' is recommended for normal use.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' or 'steady state' operating mode of the Rx signal amplitude and DC offset measuring and tracking circuits. These circuits analyze the Rx signal envelope and charge the DOC1 and DOC2 capacitors to 'store' signal maximum and minimum references that are used in the data reception process. This setting is temporarily overridden during the automatic sequencing triggered by an AQLEV command when level is initially being acquired as described in Section 5.3.

B3	B2	Mode
0	0	Hold
0	1	Level Track
1	0	Lossy Peak Detect
1	1	Slow Peak Detect

In normal use the LEVRES bits should be set to '0 1' (Level Track). The other modes are intended for special purposes, for device testing, or are invoked automatically during an AQLEV sequence.

In 'Slow Peak Detect' modes, the positive and negative excursions of the received signal (after filtering) are measured by peak rectifiers driving the DOC1 and DOC2 capacitors to establish the amplitude of the signal and any DC offset with regards to V_{BIAS}. This mode provides good overall performance, particularly when acquiring level information at the start of a received message, but does not work as well with certain long sequences of repeated data byte values. It is also susceptible to large amplitude noise spikes, which can be caused by deep fades.

The 'Lossy Peak Detect' mode is similar to 'Slow Peak Detect' but the capacitor discharge time constant is much shorter so this mode is not suitable for normal data reception and is only used within part of the automatic AQLEV acquisition sequence.

In 'Level Track' mode the DOC capacitor voltages are slowly adjusted by the MX919B in such a way as to minimize the average errors seen in the received signal. This mode provides the best overall performance, being much more accurate than 'Slow Peak Detect' when receiving large amplitude noise spikes on long sequences of repeated data byte values. It does, however, depend on the measured levels and timing being approximately correct. If either of these is significantly wrong then the correction algorithm used by the 'Level Track' mode can actually drive the voltages on the DOC capacitors away from their optimum levels. For this reason, the automatic AQLEV acquisition sequence (see Section 5.3) forces the level measuring circuits into 'Slow Peak Detect' mode until a Frame Sync pattern has been found.

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Bandwidth Modes

These two bits have no effect in transmit mode. In receive mode, they set the 'normal' or 'steady state' bandwidth of the Rx clock extraction Phase Locked Loop circuit. The PLL circuit synchronizes itself with the Rx Signal to develop a local clock signal used in the data clock recovery process. This setting will be temporarily overridden during the automatic sequencing of an AQSC command when Rx clock extraction circuits are initially being trained as described in Section 5.3.

B1	B0	PLL Mode
0	0	Hold
0	1	Narrow Bandwidth
1	0	Medium Bandwidth
1	1	Wide Bandwidth

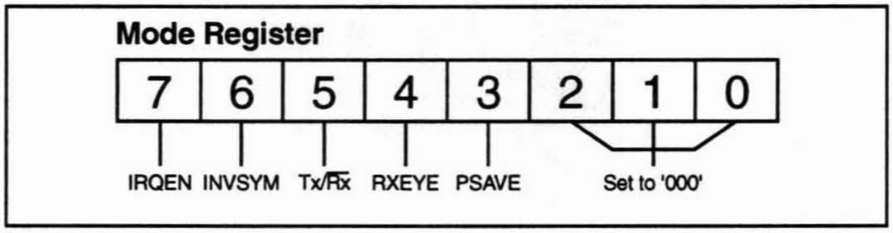
The normal setting for the PLLBW bits should be 'Medium Bandwidth' when the received symbol rate and the frequency of the receiving modem's crystal are both within ±100ppm of nominal, except at the start of a symbol clock acquisition sequence (AQSC) when 'Wide Bandwidth' should be selected as described in Section 5.3

If the received symbol rate and the crystal frequency are both within ±20ppm of nominal then selection of the 'Narrow Bandwidth' setting will provide better performance especially through fades or noise bursts which may otherwise pull the PLL away from its optimum timing. In this case however; it is recommended that the PLLBW bits only be set to 'Narrow Bandwidth' after the modem has been running in 'Medium Bandwidth' mode for about 200 symbol times to ensure accurate lock has first been achieved.

The 'Hold' setting disables the feedback loop of the PLL which continues to run at a rate determined only by the actual crystal frequency and the setting of the Control Register CKDIV bits, not the PLL's operating frequency immediately prior to the 'Hold' setting.

4.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{\text{IRQ}}$ Output Enable

When this bit is set to '1', the $\overline{\text{IRQ}}$ chip output pin is pulled low (V_{SS}) given the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

Note: B6 must be normally set to the same value in Tx and Rx devices for successful operation.

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' places the modem into the Transmit mode, clearing it to '0' puts the modem into the Receive mode.

Note: Changing between receive and transmit modes will cancel any current task.

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'. Setting it to '1' when the modem is in receive mode configures the modem for a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters, and FM demodulator.

This mode is provided because observation of the direct discriminator output of a root raised cosine Tx filtered signal (before Rx equalization) is not very recognizable so it is generally not useful.

The resulting eye diagram (for reasonably random data) should ideally be as shown in the following Figure 14, with 4 distinct and equally spaced level crossing points.

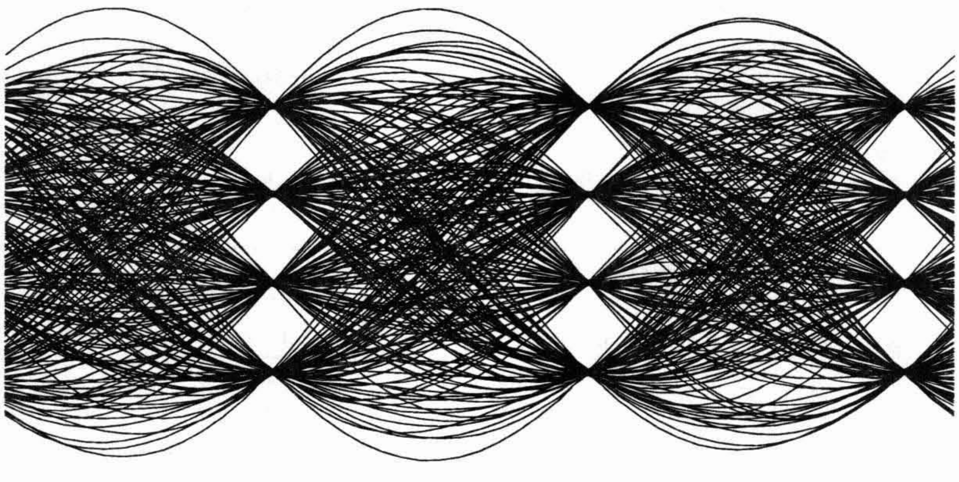


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol and Clock extraction circuits, and the Tx output buffer will be disabled. The TXOUT pin will be connected to V_{BIAS} through a high value internal resistance. The Xtal clock oscillator, Rx input amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

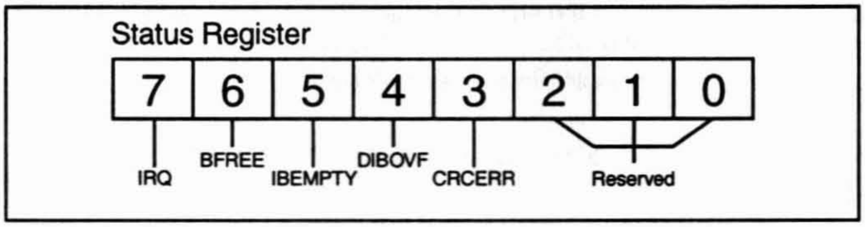
Note: The internal filters, and therefore the TXOUT pin in transmit mode, will take approximately 20 symbol-times to settle after the PSAVE bit has gone from '1' to '0'.

4.5.4.6 Mode Register B2, B1, B0

These bits should be set to '000'.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register $TX/\overline{RX}$ or PSAVE bits

or The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register $TX/\overline{RX}$ or PSAVE bits.

or The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (V_{SS}) when the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' when a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register $TX/\overline{RX}$ or PSAVE bits are changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register $TX/\overline{RX}$ or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level (halfway between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the $TX/\overline{RX}$ or PSAVE bits of the Mode Register.

In transmit mode this bit will be '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode, this bit will be updated at the end of a SFSH, RHB or RILB task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task or by changing the $TX/\overline{RX}$, or PSAVE bits of the Mode Register. In transmit mode this bit is '0'.

4.5.5.6 Status Register B2, B1, B0

These bits are reserved for future use.

4.5.6 Data Quality Register

In receive mode, the MX919B continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal' 4-level FSK baseband signal.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

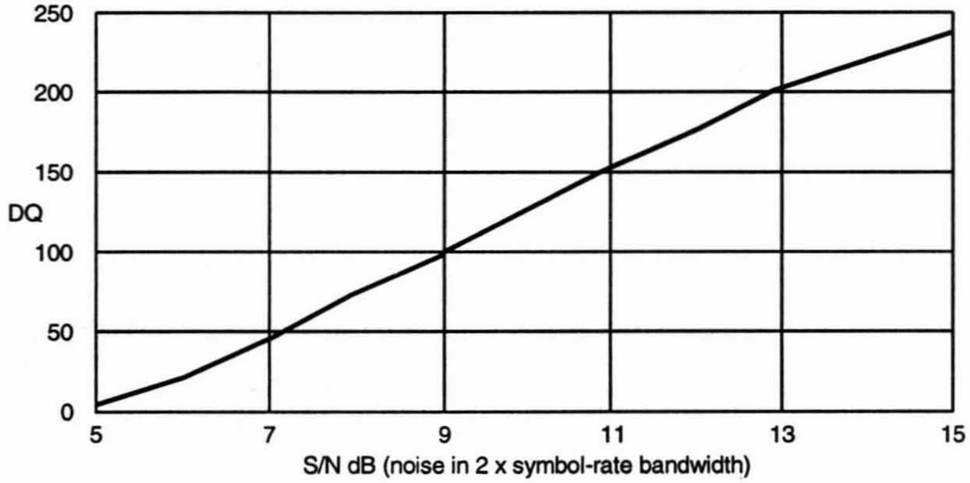


Figure 15: Typical Data Quality Reading vs S/N

The Data Quality readings are only valid when the modem has successfully acquired signal level and timing lock for at least 64 symbol times. It is invalid when an AQSC or AQLEV sequence is being performed or when the LEVRES setting is 'Lossy Peak Detect'. A low reading will be obtained if the PLLBW bits are set to 'Wide' or if the received signal waveform is distorted in any significant way.

Section 5.6 describes how monitoring the Data Quality reading can help improve the overall system performance in some applications.

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block, which provides error detection coverage for the Header Block of a message. It is calculated by the modem from the first 80 bits of the Header Block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^{5} + 1$$

4.6.1.2 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block, which provides error detection coverage for the combined Intermediate Blocks and Last Block of a message. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x^{1} + 1$$

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB, or TLB.

Command Register bit B5 (CRC) allows the user to select between two different forms of the CRC1 and CRC2 checksums. When this bit is set to '0', the CRC generators are initialized to 'all ones' for calculations such as CCITT X25 CRC. When this bit is set to '1', the CRC generators are initialized to 'all zeros'.

4.6.1.3 Forward Error Correction

In transmit mode, the MX919B uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block into a 66-symbol (132 bits) sequence which includes FEC information.

In receive mode, the MX919B decodes the received 66 symbols of a block into 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.1.4 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to provide protection against the effects of noise bursts and short fades.

In receive mode, the MX919B de-interleaves the received symbols prior to decoding.

4.7 Transmitted Symbol Shape

Bit 4 of the Command Register (TXIMP) selects the transmit baseband signal and the receive signal equalization as follows:

If the TXIMP bit is '0', then the transmit baseband signal is generated by feeding full-symbol-time-width 4-level symbols into the RRC lowpass filter. The receive signal equalization is optimized for this type of signal. With this setting, the MX919B is compatible with the MX919A devices, another member of the MX919 device family.

If the TXIMP bit is set to '1,' impulses, rather than full-symbol-time-width symbols are fed into the RRC filter when in TX mode, and the receive signal equalization is suitably adjusted in RX mode.

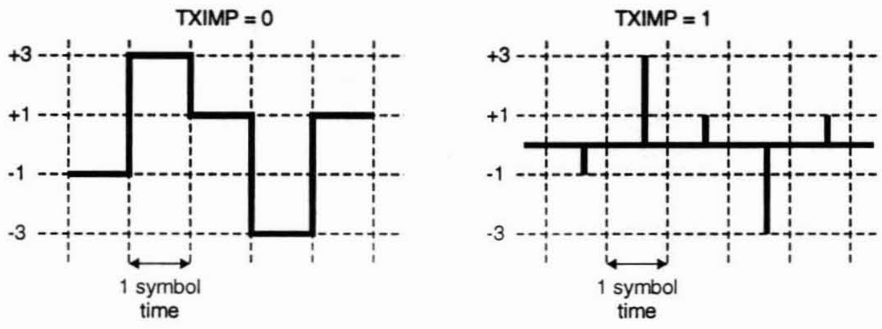


Figure 16: Input Signal to RRC Filter in Tx Mode for TXIMP = 0 and 1

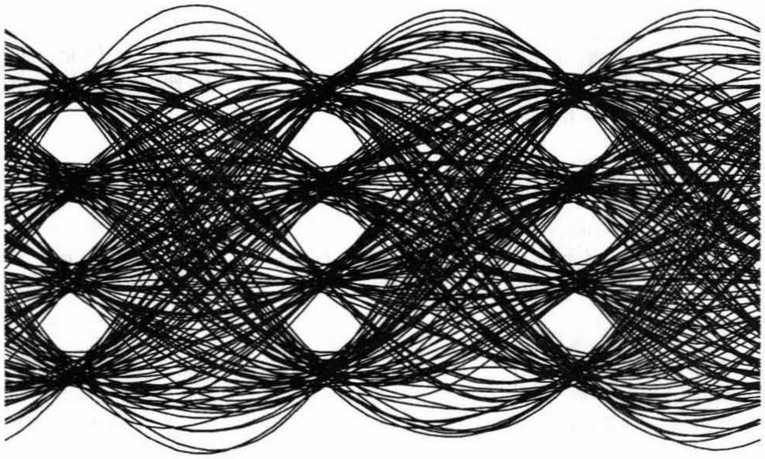


Figure 17: Tx Signal Eye TXIMP = 0

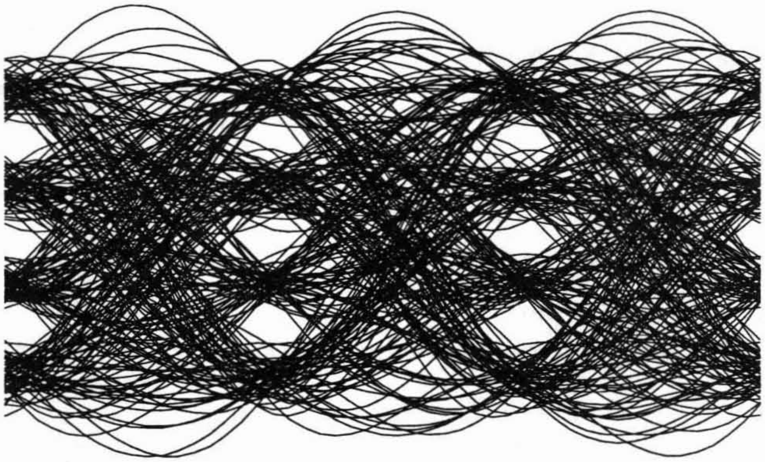


Figure 18: Tx Signal Eye TXIMP = 1

Note: Setting TXIMP to '1' affects the Tx output signal level as shown in Section 6.1.3 and the table below.

	TXIMP = 0	TXIMP = 1
Nominal Voltage difference between continuous '+3' and continuous '-3' symbol outputs.	$0.157V_{DD}$	$0.157V_{DD}$
Nominal V_{P-P} for continuous '+3 +3 -3 -3..." symbol pattern.	$0.20V_{DD}$	$0.22V_{DD}$

5 Application

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, and one each Header, Intermediate and Last blocks are provided below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and TX/$\overline{\text{RX}}$ bits of the Mode Register are '1', the RXEYE and PSAVE bits are '0', and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes (a preamble) to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write 6 byte Frame Sync to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

Figure 19 and Figure 20 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Header block, and any number of Intermediate blocks and one Last Block. It is assumed that the Tx Interrupt Service Routine Figure 20 is called when the MX919B $\overline{\text{IRQ}}$ output line goes low.

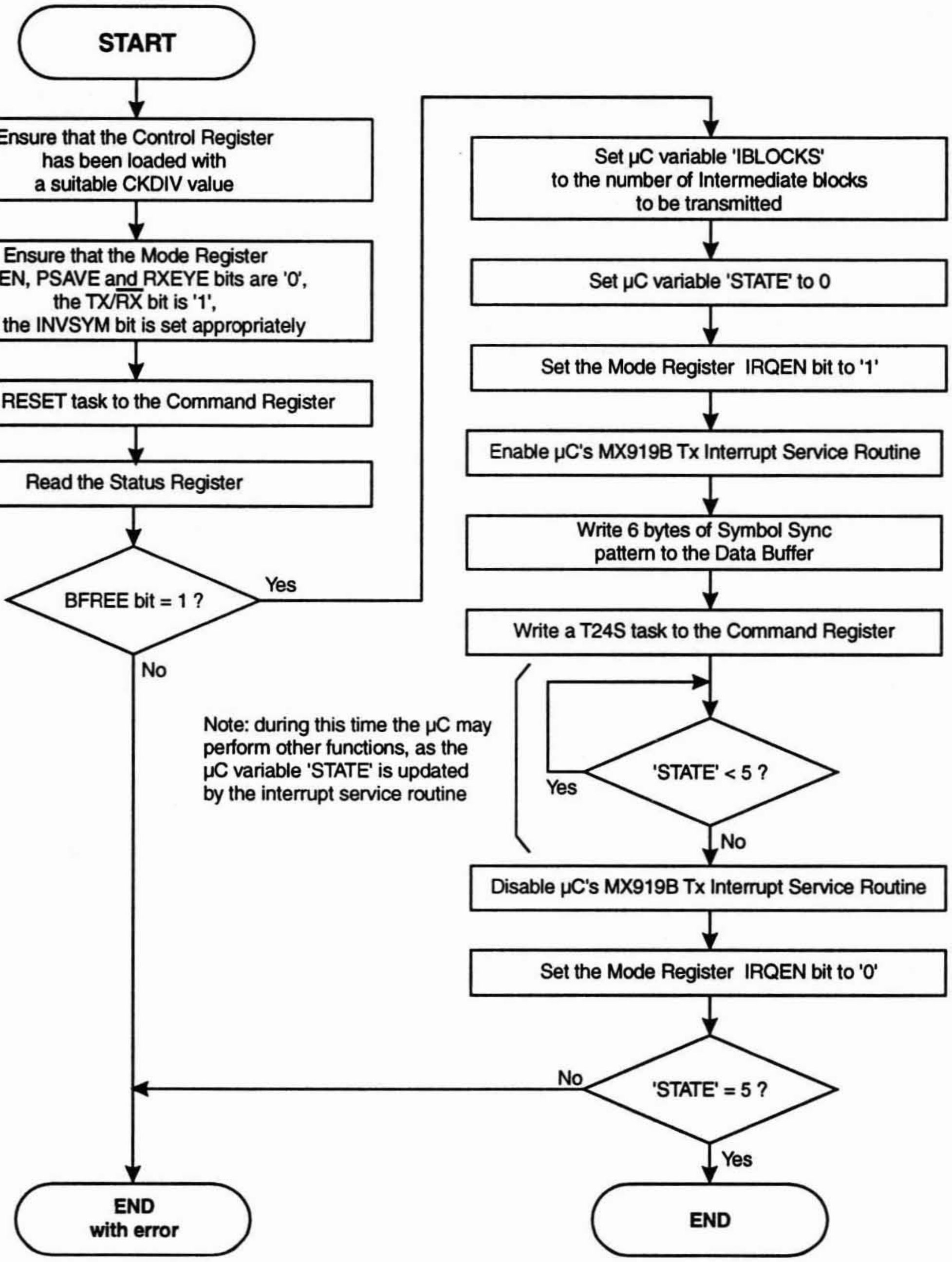
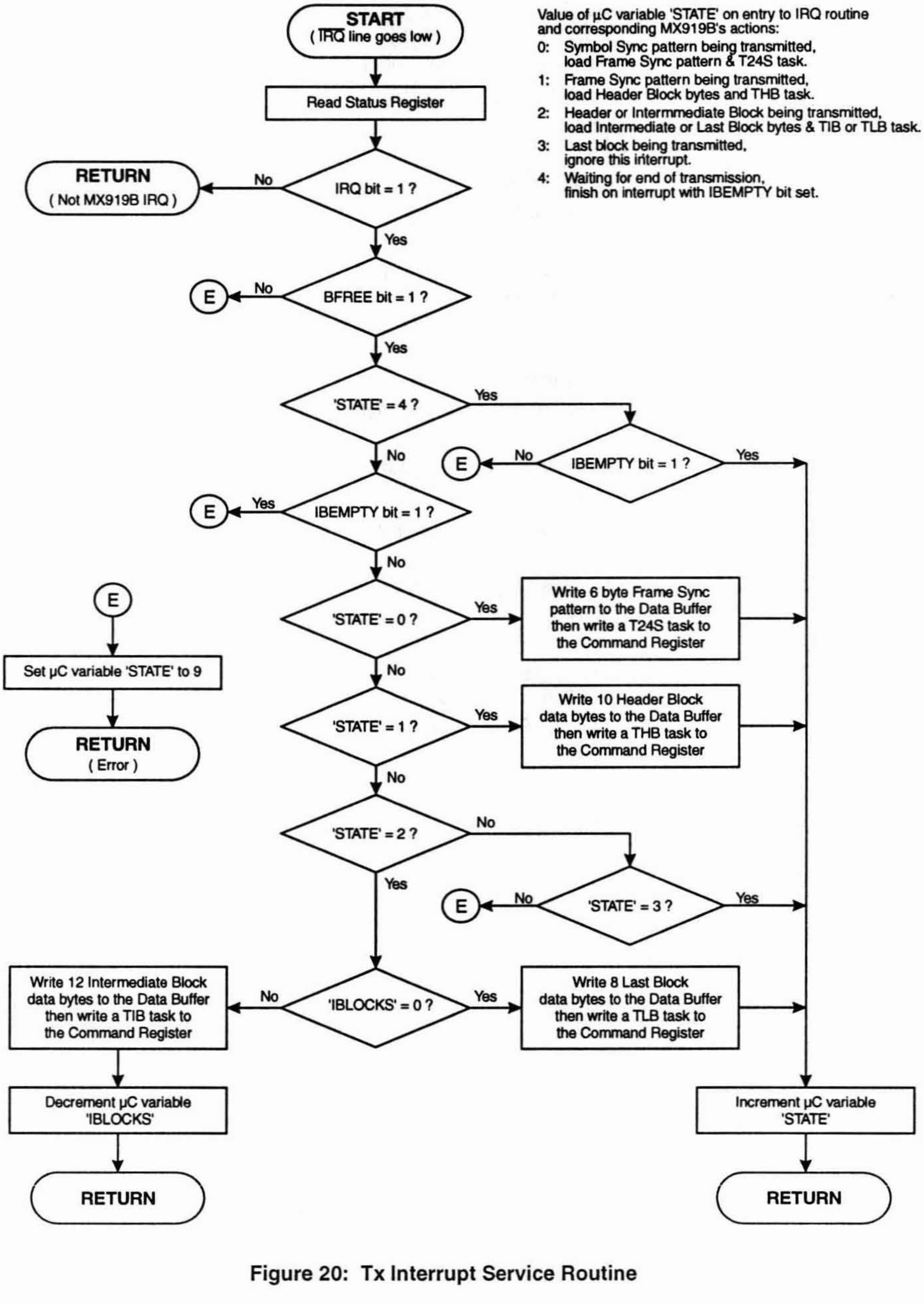

START
Ensure that the Control Register has been loaded with a suitable CKDIV value
Ensure that the Mode Register IRQEN, PSAVE and RXEYE bits are '0', the TX/$\overline{RX}$ bit is '1', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Set µC variable 'IBLOCKS' to the number of Intermediate blocks to be transmitted
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX919B Tx Interrupt Service Routine
Write 6 bytes of Symbol Sync pattern to the Data Buffer
Write a T24S task to the Command Register
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 5 ?
Yes
No
Disable µC's MX919B Tx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 5 ?
No
Yes
END with error
END

Figure 19: Transmit Frame Example Flowchart, Main Program

Notes

1. The RESET command in Figure 19 and the practice of disabling the MX919B's $\overline{\text{IRQ}}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.


START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX919B IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
'STATE' = 4 ?
Yes
IBEMPTY bit = 1 ?
No
E
Yes
No
IBEMPTY bit = 1 ?
Yes
E
No
'STATE' = 0 ?
Yes
Write 6 byte Frame Sync pattern to the Data Buffer then write a T24S task to the Command Register
No
'STATE' = 1 ?
Yes
Write 10 Header Block data bytes to the Data Buffer then write a THB task to the Command Register
No
'STATE' = 2 ?
No
'STATE' = 3 ?
No
E
Yes
Yes
'IBLOCKS' = 0 ?
No
Write 12 Intermediate Block data bytes to the Data Buffer then write a TIB task to the Command Register
Yes
Write 8 Last Block data bytes to the Data Buffer then write a TLB task to the Command Register
Decrement µC variable 'IBLOCKS'
RETURN
Increment µC variable 'STATE'
RETURN
E
Set µC variable 'STATE' to 9
RETURN
(Error)

Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX919B's actions:

0: Symbol Sync pattern being transmitted, load Frame Sync pattern & T24S task.

1: Frame Sync pattern being transmitted, load Header Block bytes and THB task.

2: Header or Intermmediate Block being transmitted, load Intermediate or Last Block bytes & TIB or TLB task.

3: Last block being transmitted, ignore this interrupt.

4: Waiting for end of transmission, finish on interrupt with IBEMPTY bit set.

Figure 20: Tx Interrupt Service Routine

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the TX/$\overline{\text{RX}}$ PSAVE, and RXEYE bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see Section 5.3).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFSH task and with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
7. Write a RILB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Read 12 Intermediate Block bytes from the Data Block Buffer.
10. Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Figure 21 and Figure 22 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Header Block, any number of Intermediate blocks and one Last block. It is assumed that the Rx Interrupt Service Routine Figure 22 is called when the MX919B's $\overline{\text{IRQ}}$ output goes low.

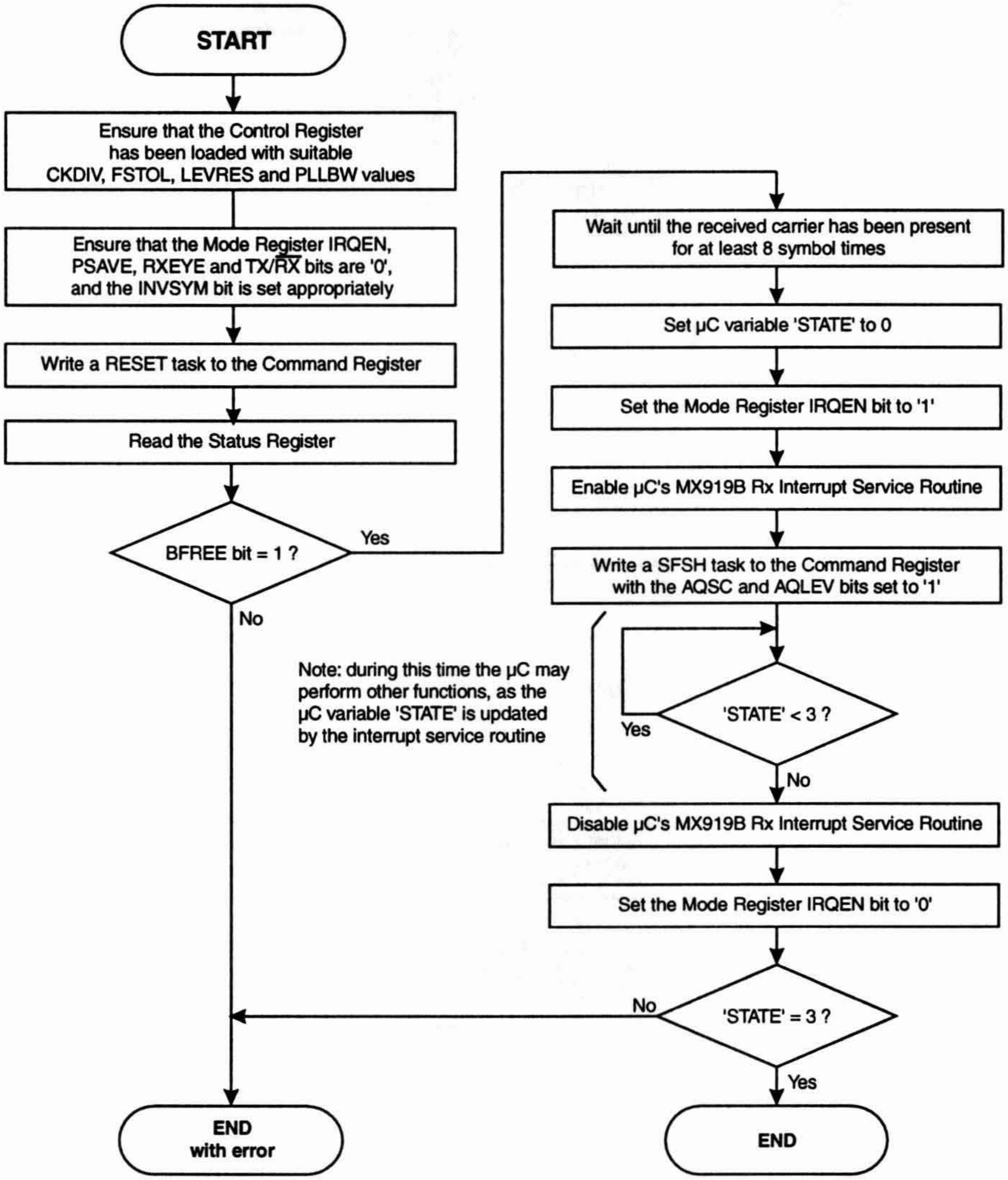
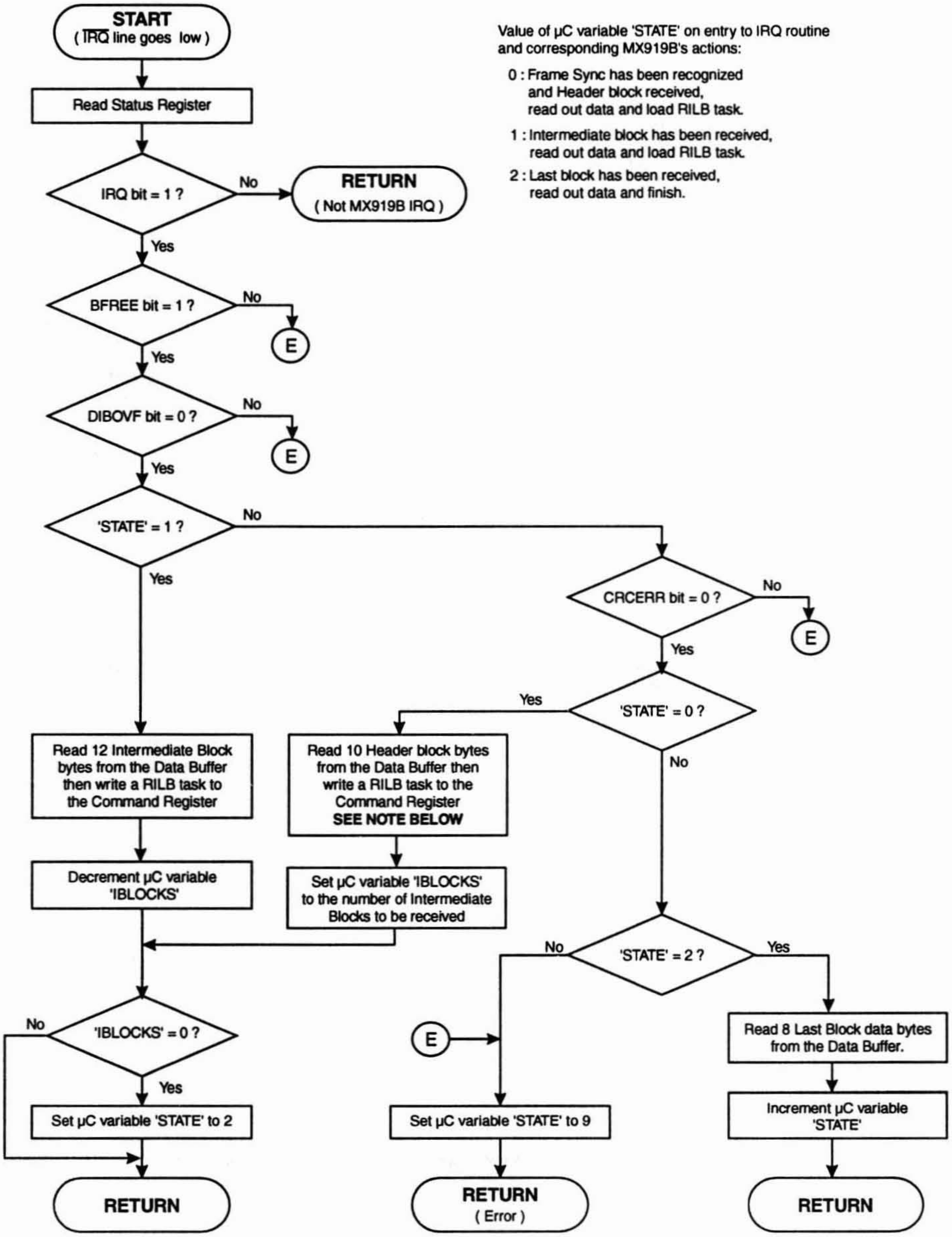

START
Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values
Ensure that the Mode Register IRQEN, PSAVE, RXEYE and TX/$\overline{RX}$ bits are '0', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Wait until the received carrier has been present for at least 8 symbol times
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX919B Rx Interrupt Service Routine
Write a SFSH task to the Command Register with the AQSC and AQLEV bits set to '1'
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 3 ?
Yes
No
Disable µC's MX919B Rx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 3 ?
No
Yes
END with error
END

Figure 21: Receive Frame Example Flowchart, Main Program

Notes

1. The RESET command in Figure 21 and the practice of disabling the MX919B's $\overline{\text{IRQ}}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation.
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.


START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX919B IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
DIBOVF bit = 0 ?
No
E
Yes
'STATE' = 1 ?
No
Yes
CRCERR bit = 0 ?
No
E
Yes
'STATE' = 0 ?
Yes
No
Read 12 Intermediate Block bytes from the Data Buffer then write a RILB task to the Command Register
Read 10 Header block bytes from the Data Buffer then write a RILB task to the Command Register
SEE NOTE BELOW
Decrement µC variable 'IBLOCKS'
Set µC variable 'IBLOCKS' to the number of Intermediate Blocks to be received
'STATE' = 2 ?
No
Yes
'IBLOCKS' = 0 ?
No
Yes
E
Read 8 Last Block data bytes from the Data Buffer.
Set µC variable 'STATE' to 2
Set µC variable 'STATE' to 9
Increment µC variable 'STATE'
RETURN
RETURN
(Error)
RETURN

Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX919B's actions:

0 : Frame Sync has been recognized and Header block received, read out data and load RILB task.

1 : Intermediate block has been received, read out data and load RILB task.

2 : Last block has been received, read out data and finish.

Figure 22: Rx Interrupt Service routine

Note: This routine assumes that the number of Intermediate blocks in the Frame is contained within the Header Block Data.

5.3 Clock Extraction and Level Measurement Systems

5.3.1 Supported Types of Systems

The MX919B is intended for use in systems where:

1. The Symbol Sync pattern is transmitted immediately on start-up of the transmitter, before the first Frame Sync pattern (see Figure 23).
2. A terminal may remain powered up indefinitely, transmitting concatenated Frames with or without intervening Symbol Sync patterns (each Frame having a Frame Sync pattern and symbol timing being maintained from one Frame to the next).
3. A receiving modem may be switched onto a channel before the distant transmitter has started up, or may be switched onto a channel where the transmitting station is already sending concatenated Frames

5.3.2 Clock and Level Acquisition Procedures with RF Carrier Detect

When the receiving modem is enabled or switched onto a channel, it needs to establish the received symbol levels, clock timing, and look for a Frame Sync pattern in the incoming signal. This is best done by the following procedure:

1. Ensure that the Control Register's PLLBW bits are set to 'Wide' and the LEVRES bits to 'Track'.
2. Wait until a received carrier has been present for 8 symbol times. This 8-symbol delay gives time for the received signal to propagate through the modem's RRC filter. An 'RF received 8 symbol times' qualifying function can be included in a radio's carrier detect circuitry to take this into account.
3. Write a SFS or SFSH task to the Command Register with the AQSC and the AQLEV bits set to '1'.
4. When the modem interrupts to signal that it has recognized a Frame Sync pattern (or completed the SFSH task) then change the PLLBW bits to 'Medium'.

Once the receiving modem has achieved level and symbol timing synchronization with a particular channel - as evidenced by recognition of a Frame Sync pattern - then subsequent concatenated Frames can be read by simply issuing SFS or SFSH tasks at appropriate times, keeping the ASQSC and AQLEV bits at zero, and the PLLBW and LEVRES bits at their current 'Medium' and 'Track' settings, respectively.

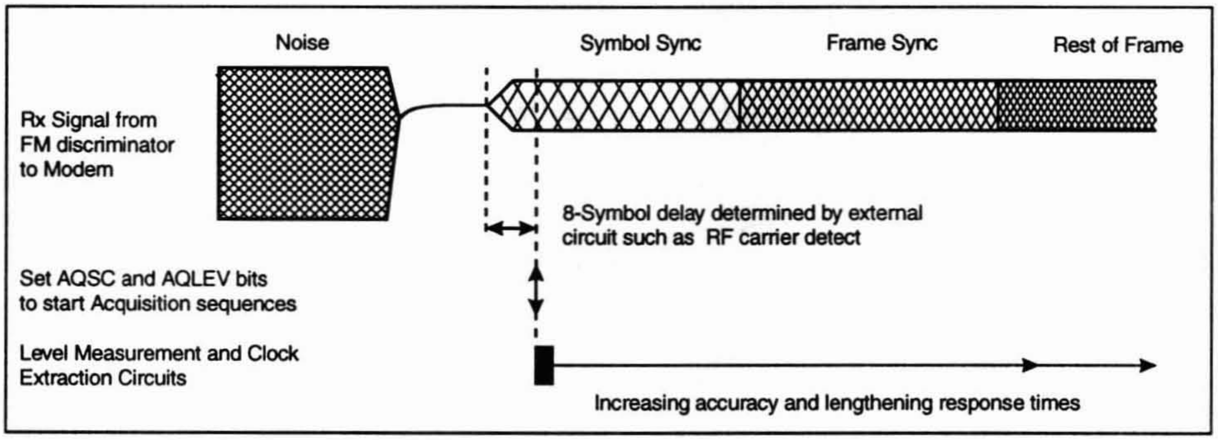

Noise
Symbol Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
8-Symbol delay determined by external circuit such as RF carrier detect
Set AQSC and AQLEV bits to start Acquisition sequences
Level Measurement and Clock Extraction Circuits
Increasing accuracy and lengthening response times

Figure 23: Acquisition Sequence Timing

5.3.3 Clock and Level Acquisition Procedure without RF Carrier Detect

It is also possible to use the modem in a system where there is an indeterminate delay between the RF transmitter turn on time and the transmission moment of the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC, or where the transmitting terminal can send separate unsynchronized Frames. In these cases, each Frame should be preceded by, a Symbol Sync pattern which should be extended to about 100 symbols and the procedure provided in Section 5.3.2. used.

5.3.4 Automatic Acquisition Functions

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude, and DC offset as quickly as possible before switching to accurate - but slower - measurement modes. These acquisition sequences act very quickly if triggered at the start of a received Symbol Sync pattern (as shown in Figure 23), but will still function correctly, although more slowly, if started any time during a normal Frame as when the receiver is switched onto a channel where the transmitter is operating continuously.

The automatic AQLEV Level Measurement acquisition sequence starts with the level measurement circuits being put into 'Clamp' Mode for one symbol time to quickly set the voltages on the DOC pins to approximately correct levels. The level measurement circuits are then automatically set to 'Lossy Peak Detect' mode for 15 symbol times, then 'Slow Peak Detect' until a received Frame Sync pattern is recognized, after which the automatic sequence ends and the level measurement circuit mode reverts to the mode set by the LEVRES bits of the Control Register (normally 'Level Track').

The peak detectors used in both 'Slow' and 'Lossy Peak Detect' modes include additional low pass filtering of the received signal which greatly reduces the effect of pattern noise on the reference voltages held on the external DOC capacitors, but means that pairs of '+3' (and '-3') symbols need to be received to establish the correct levels. Two pairs of '+3' and two pairs of '-3' symbols received after the start of an AQLEV sequence are sufficient to correctly set the levels on the DOC capacitors.

The automatic AQSC Symbol Clock acquisition sequence sets the PLL to 'Extra Wide Bandwidth' mode for 16 symbol times (this mode is not one of those which can be selected by the Control Register PLLBW bits) then changes to 'Wide' bandwidth. After 45 symbol times, the PLL mode will revert to that set by the Control Register PLLBW bits.

5.4 AC Coupling

For a practical circuit, ac coupling between the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem may be desired. There are, however, two issues which deserve consideration:

1. AC coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (9600bps) without FEC for reasonably random data with differing degrees of AC coupling:

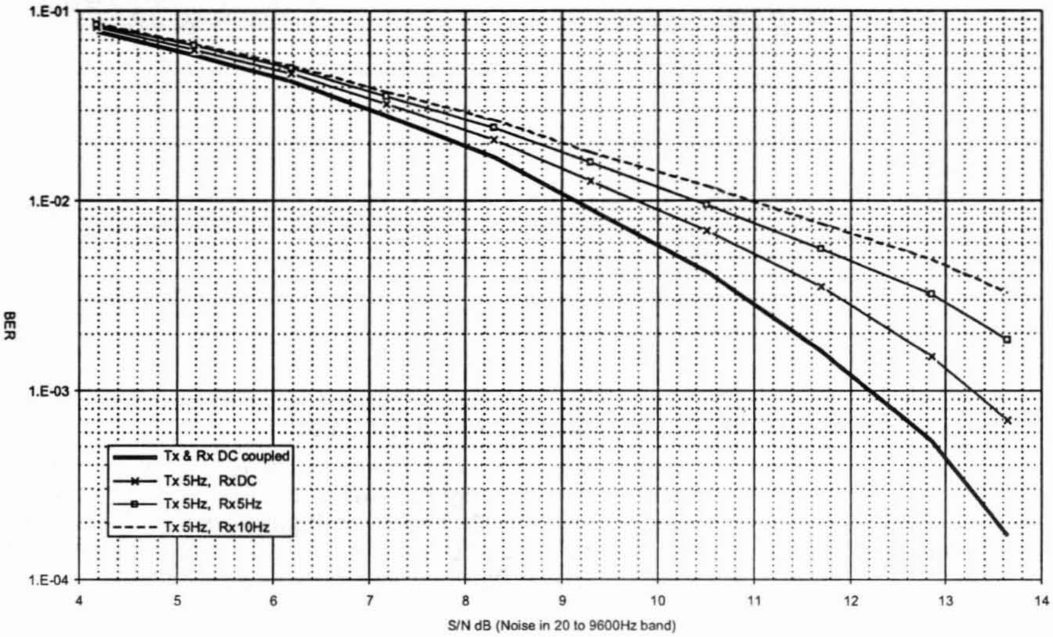


Figure 24: Effect of AC Coupling on BER (without FEC)

2. Any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 25 below, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = \frac{1}{2\pi(\text{3dB cut - off frequency of the RC network})}$$

which is 32ms, or 153 symbol times at 4800 symbols/sec (9600bps) for a 5Hz network.

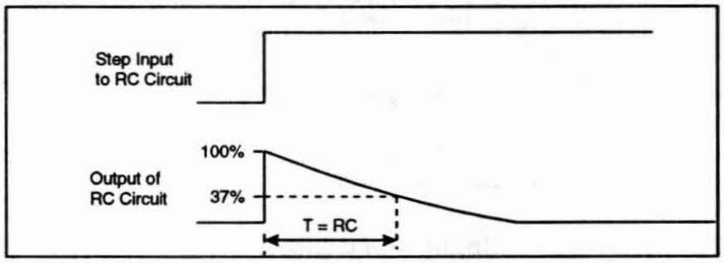


Figure 25: Decay Time - AC Coupling

In general, it is best to DC couple the receiver discriminator to the modem and ensure that any AC coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz for 4800 symbols/sec (9600bps).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracy.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec (9600bps) can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive ' +3 +3 -3 -3 ... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. However; this does place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency, and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec (9600bps) system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the equalized received signal eye diagram, using the Mode Register RXEYE function, provides a good indication of the overall RF transmitter/receiver performance.

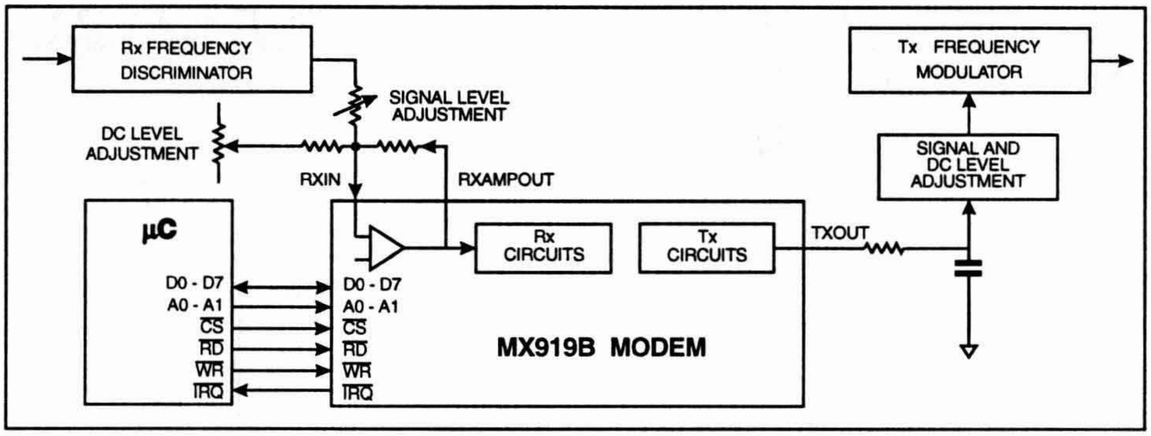

Rx FREQUENCY DISCRIMINATOR
SIGNAL LEVEL ADJUSTMENT
DC LEVEL ADJUSTMENT
RXIN
RXAMPOUT
µC
D0 - D7
A0 - A1
$\overline{\text{CS}}$
$\overline{\text{RD}}$
$\overline{\text{WR}}$
$\overline{\text{IRQ}}$
Rx CIRCUITS
Tx CIRCUITS
MX919B MODEM
TXOUT
Tx FREQUENCY MODULATOR
SIGNAL AND DC LEVEL ADJUSTMENT

Figure 26: Typical Connections between Radio and MX919B

5.6 Received Signal Quality Monitor

In applications where the modem has to monitor a long transmission containing a number of concatenated Frames, it is recommended that the controlling software include a function which regularly checks that the modem is still receiving a good data signal and triggers a re-acquisition and possibly changes to another channel if a problem is encountered. This strategy has been shown to improve the system's overall performance in situation where fading, large noise bursts, severe co-channel interference, or loss of the received signal for long periods are likely to occur.

Such a function can be simply implemented by regularly reading the Data Quality Register, which gives a measure of the overall quality of the received signal, as well as the current effectiveness of the modem's clock extraction and level measurement systems. Experience has shown that if two consecutive DQ readings are both less than 50 then it is worth instructing the MX919B to re-acquire the received signal levels and timing once it has been established that the received carrier level is satisfactory. Re-acquisition should follow the procedure given in Section 5.3.

The intervals between Data Quality readings is not critical, but should be a minimum of 64 symbol times except for the first reading made after triggering the AQSC and AQLEV automatic acquisition sequences, which should be delayed for about 250 symbol times.

A suitable algorithm is shown in Figure 27.

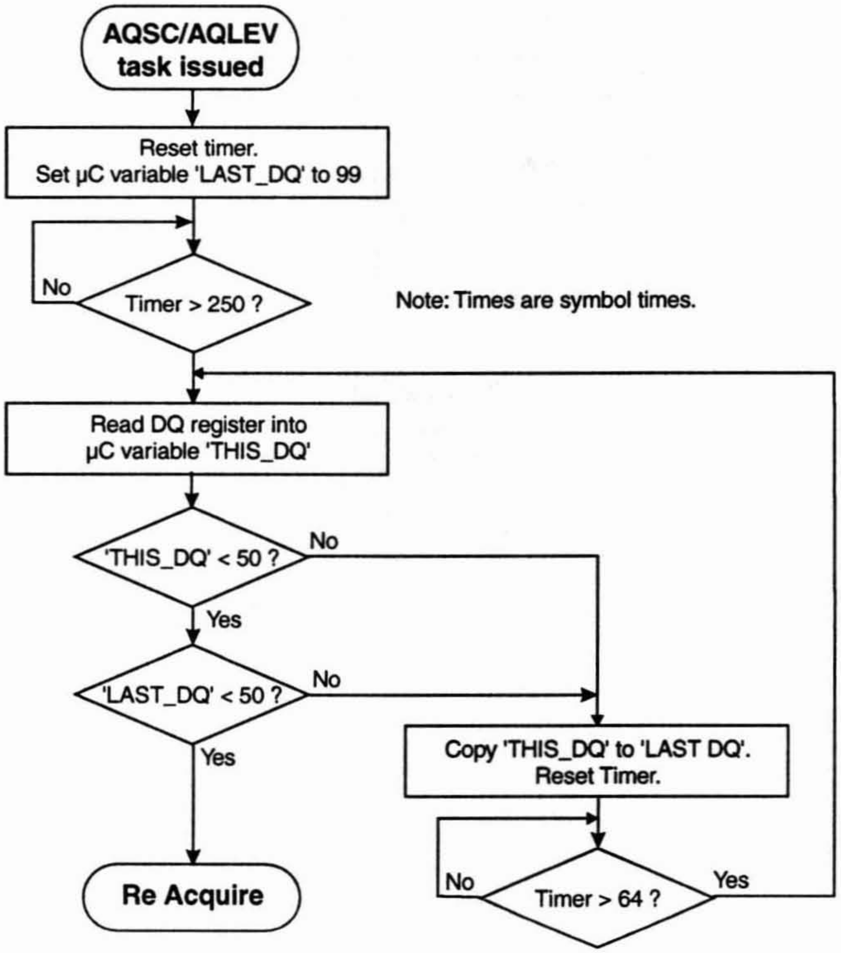

AQSC/AQLEV task issued
Reset timer.
Set µC variable 'LAST_DQ' to 99
No
Timer > 250 ?
Note: Times are symbol times.
Read DQ register into µC variable 'THIS_DQ'
'THIS_DQ' < 50 ?
No
Yes
'LAST_DQ' < 50 ?
No
Yes
Copy 'THIS_DQ' to 'LAST DQ'.
Reset Timer.
Re Acquire
No
Timer > 64 ?
Yes

Figure 27: Received Signal Quality Monitor Flowchart

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Symbol Rate		2400	9600	Symbols/sec
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC Parameters					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level					
TXIMP = 0	3	0.8	1.0	1.2	V_{P-P}
TXIMP = 1	3	0.88	1.1	1.32	V_{P-P}
Output DC Offset with respect to V_{DD} /2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset with respect to V_{DD} /2	5	-0.5		0.5	V
XTAL/CLOCK INPUT					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Inverter Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	−5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

6.1.4 Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance.
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, (Tx output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence, TXIMP = 0 or 1, The optimum level and DC offset values are proportional to V_{DD}.
6. Timing for an external input to the XTAL/CLOCK pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

6.1.5 Timing

µC Parallel Interface Timings (ref. Figure 28)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

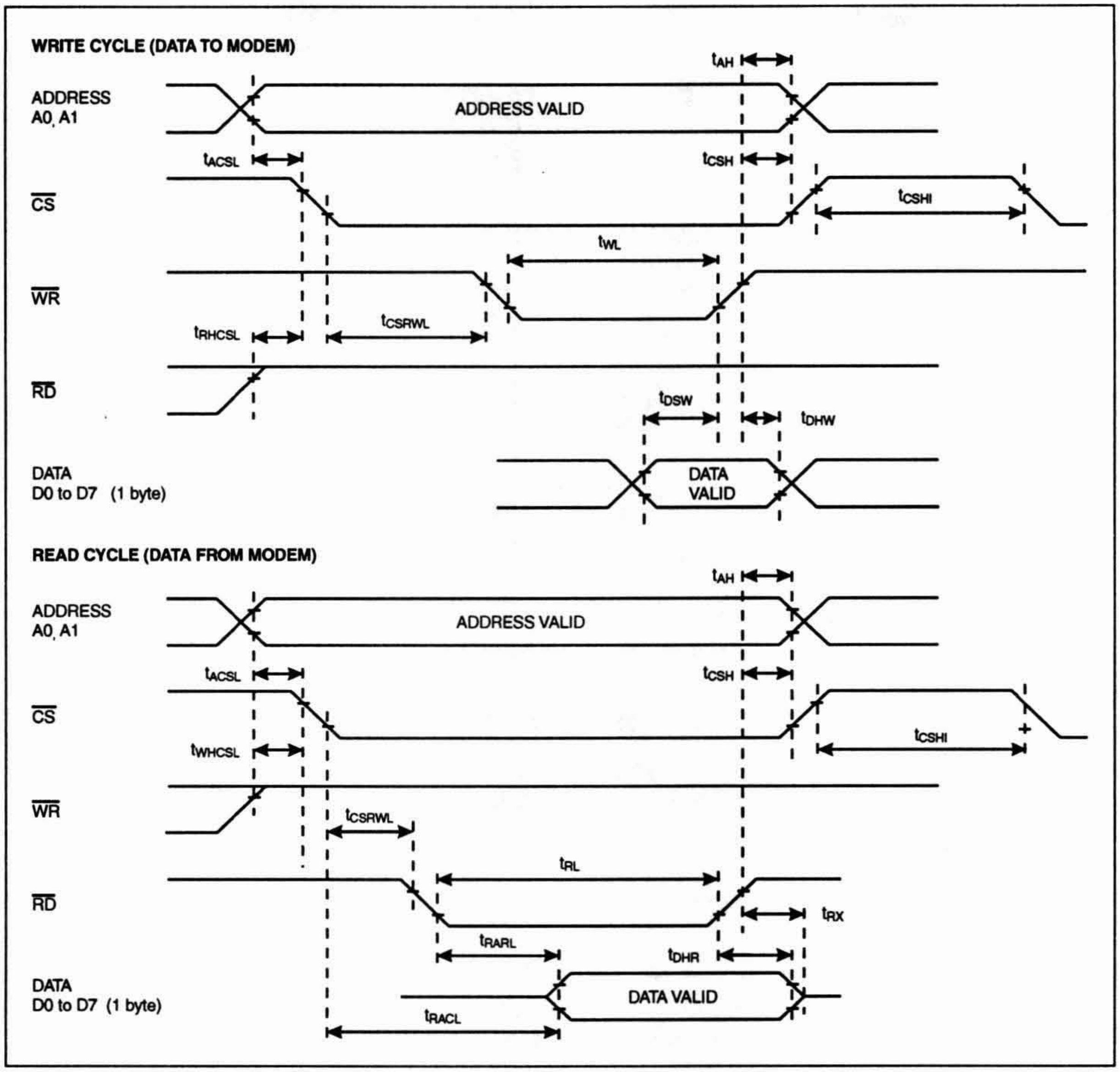

WRITE CYCLE (DATA TO MODEM)
ADDRESS
A0, A1
ADDRESS VALID
t_{AH}
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{CSHI}
t_{WL}
$\overline{WR}$
t_{RHCSL}
t_{CSRWL}
$\overline{RD}$
t_{DSW}
t_{DHW}
DATA
D0 to D7 (1 byte)
DATA VALID
READ CYCLE (DATA FROM MODEM)
ADDRESS
A0, A1
ADDRESS VALID
t_{AH}
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{WHCSL}
t_{CSHI}
$\overline{WR}$
t_{CSRWL}
t_{RL}
$\overline{RD}$
t_{RX}
t_{RARL}
t_{DHR}
DATA
D0 to D7 (1 byte)
DATA VALID
t_{RACL}

Figure 28: µC Parallel Interface Timings

6.1.6 Typical Bit Error Rate

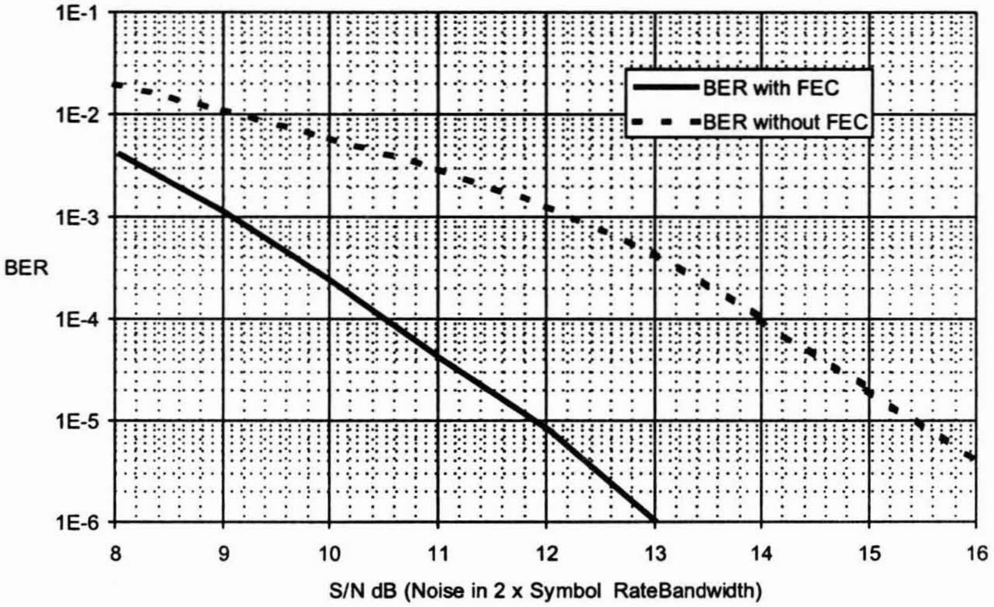


Figure 29: Typical Bit Error Rate With and Without FEC

Measured under nominal working conditions, LEVRES bits set to 'Level Track' or 'Slow Peak Detect' and PLLBW bits set to 'Medium' or 'Narrow' Bandwidth, Command Register TXIMP bit set to '0' or '1' (same for Tx and Rx devices), with pseudo-random data.

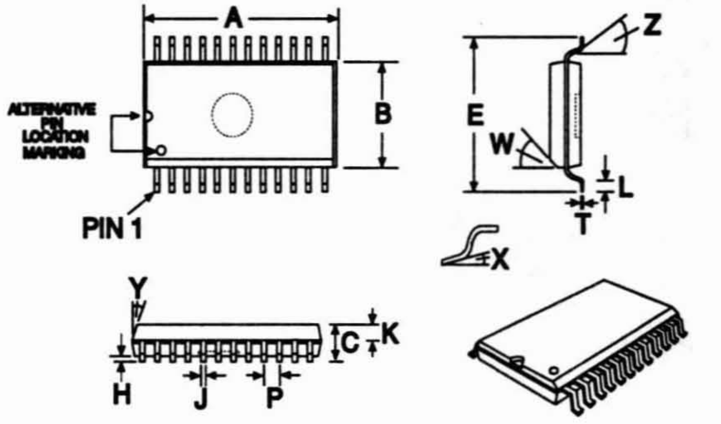
Note: $S/N \text{ calculates as } 20\log_{10}(\frac{\text{Signal Voltage}}{\text{Voltage Noise}})$

Where: Signal Voltage is the measured V_{RMS} of a random 4-level signal.

Noise Voltage is the V_{RMS} of a flat Gaussian noise signal having a bandwidth from a few Hz to twice the symbol rate e.g. to 9600Hz when measuring a 4800 symbol/sec (9600bps) system.

Both signals are measured at the same point in the test circuit.

6.2 Packaging

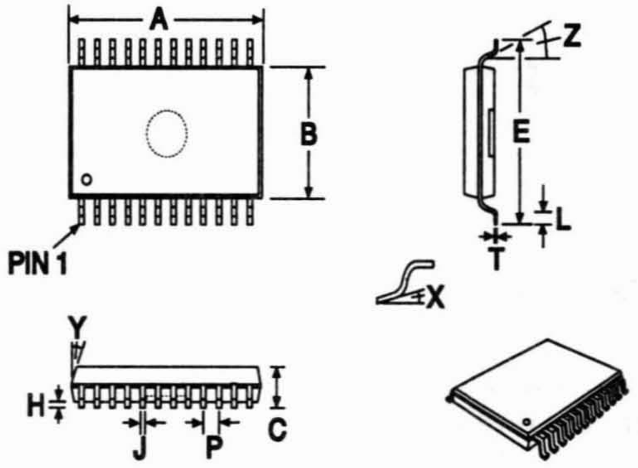


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 30: 24-pin SOIC Mechanical Outline: *Order as part no. MX919BDW*

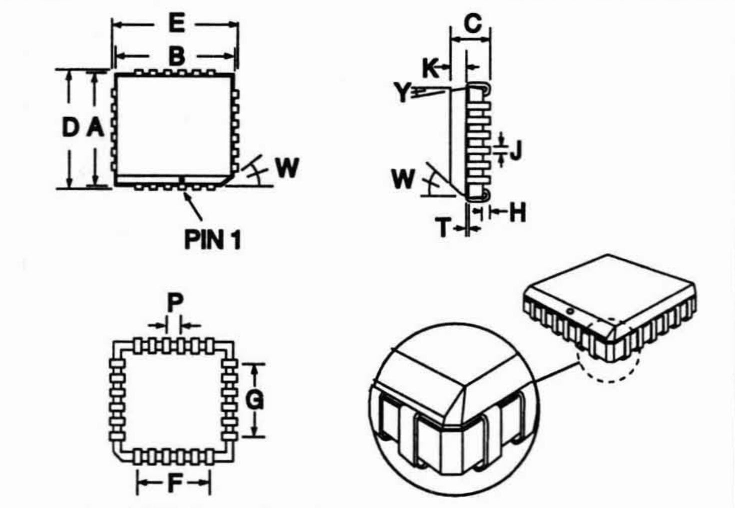


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 31: 24-pin SSOP Mechanical Outline: *Order as part no. MX919BDS*

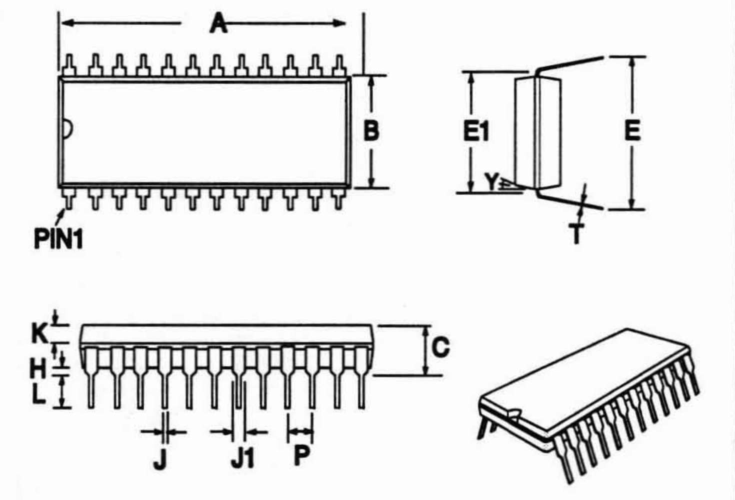


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 32: 24-pin PLCC Mechanical Outline : ***Order as part no. MX919BLH***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 33: 24-pin PDIP Mechanical Outline: ***Order as part no. MX919BP***

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX929B 4-Level FSK Modem Data Pump

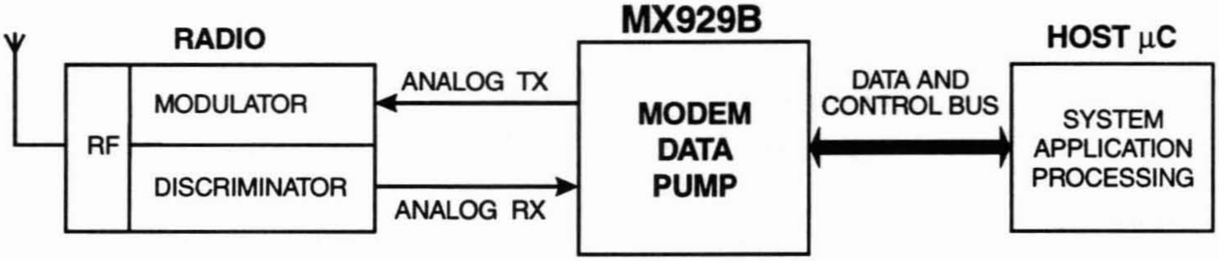
PRELIMINARY INFORMATION

Features

- 4-Level Root Raised Cosine FSK Modulation
- Half Duplex, 4800 to 19.2kbps
- Increase Channel Bit Rate/Hz
- Full Data Packet Framing
- Impulse and NRZ Signal Modes
- Enhanced Performance in Noisy Conditions
- Error Detection and Error Correction
- Low Power 3.3V/5.0V Operation

Applications

- RD-LAP™ Systems
- RCR STD-47 Systems
- Two Way Paging Systems
- Mobile Data Systems
- Wireless Telemetry
- DataTAC™ Terminals
- Portable Wireless Data Equipment



The MX929B is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host µC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over a wireless link.

The MX929B assembles application data received from the host µC, adds forward error correction (FEC) and error detection (CRC) information, and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating the radio transmitter.

In receive mode, the MX929B performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host µC. CRC detected residual uncorrected data errors will be flagged. Readout of the SNR value during receipt of a packet is also provided.

The MX929B uses data block sizes and FEC/CRC Algorithms that are compatible with RD-LAP™ and RCR STD-47 over-air-standards. The device is programmable to operate at standard bit rates from a wide range of Xtal/clock frequencies.

The MX929B may be used with a 3.0V to 5.5V power supply and is available in the following package styles: 24-pin SSOP (MX929BDS), 24-pin SOIC (MX929BDW), and 24-pin PDIP (MX929BP).

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1 Block Diagram

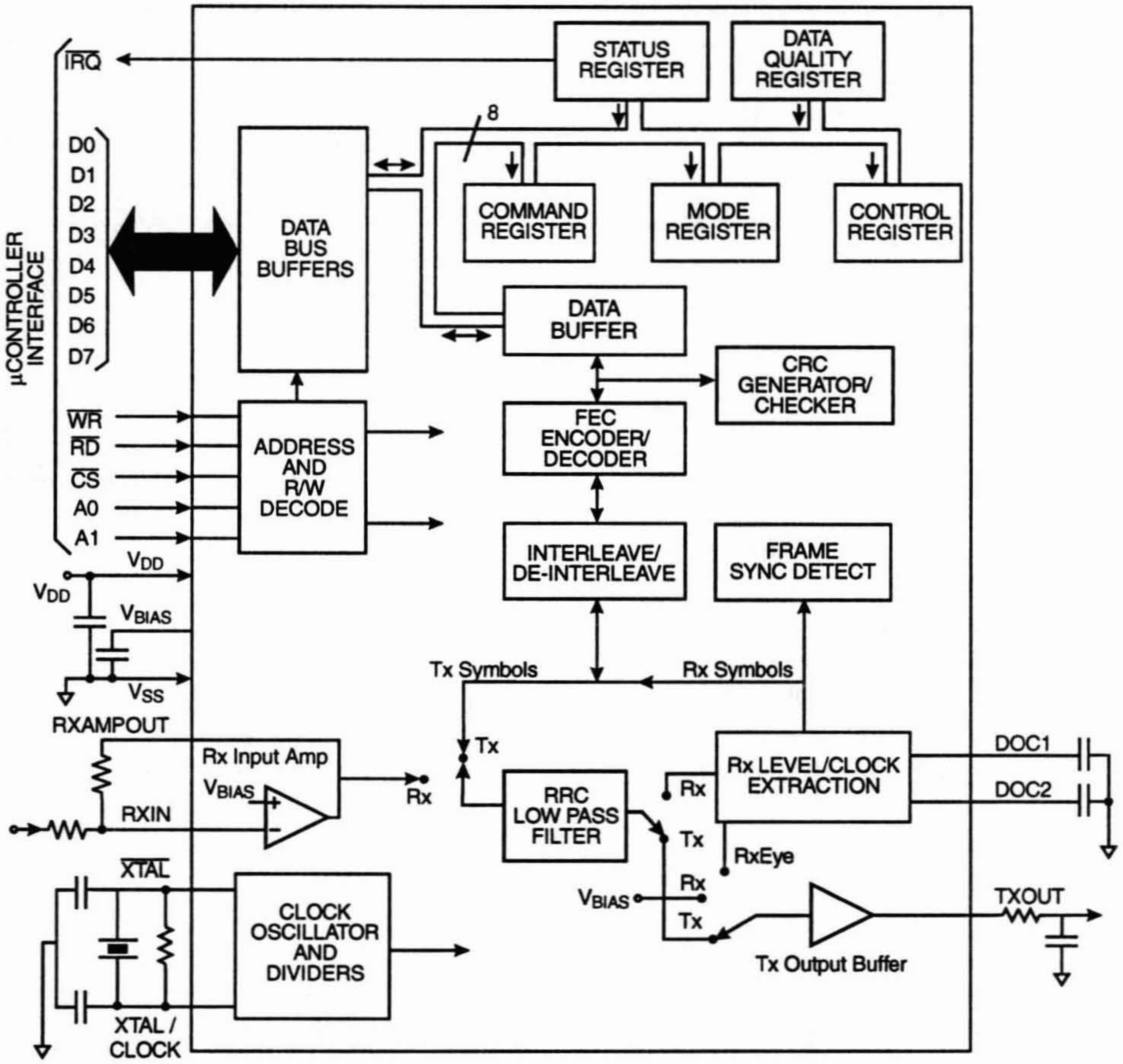
IRQ
STATUS REGISTER
DATA QUALITY REGISTER
8
D0
D1
D2
D3
D4
D5
D6
D7
µCONTROLLER INTERFACE
DATA BUS BUFFERS
COMMAND REGISTER
MODE REGISTER
CONTROL REGISTER
DATA BUFFER
CRC GENERATOR/ CHECKER
FEC ENCODER/ DECODER
WR
RD
CS
A0
A1
ADDRESS AND R/W DECODE
INTERLEAVE/ DE-INTERLEAVE
FRAME SYNC DETECT
VDD
VDD
VBIAS
VSS
Tx Symbols
Rx Symbols
RXAMPOUT
Tx
Rx Input Amp
VBIAS
Rx
RXIN
RRC LOW PASS FILTER
Rx
Tx
Rx LEVEL/CLOCK EXTRACTION
DOC1
DOC2
RxEye
Rx
VBIAS
Tx
Tx Output Buffer
TXOUT
XTAL
CLOCK OSCILLATOR AND DIVIDERS
XTAL / CLOCK

Figure 1: Block Diagram

2 Signal List

Pin No.	Signal	Type	Description
1	$\overline{\text{IRQ}}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{\text{RD}}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{\text{WR}}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply (ground).
13	$\overline{\text{CS}}$	input	Chip Select. An active low logic level input to the modem used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{\text{XTAL}}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for an external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry held at V_{DD} /2. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Note: Internal protection diodes are connected from each signal pin to V_{DD} and V_{SS}.

3 External Components

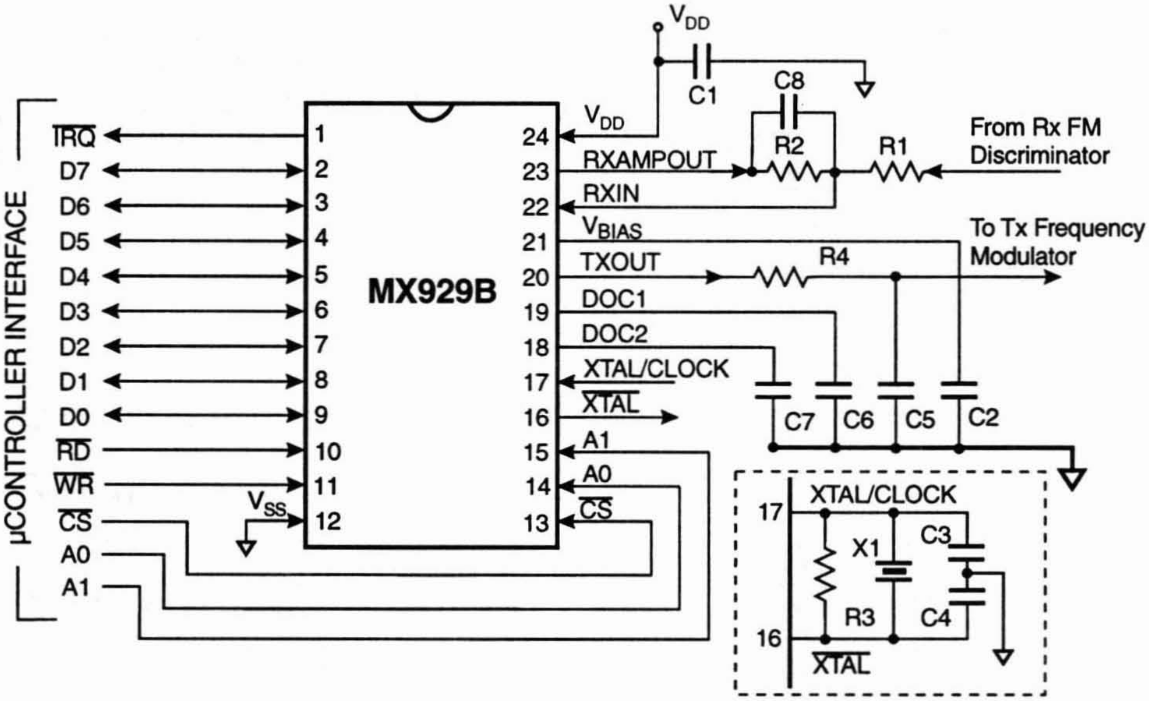
VDD
C1
C8
R2
R1
From Rx FM Discriminator
To Tx Frequency Modulator
R4
MX929B
μCONTROLLER INTERFACE
IRQ
D7
D6
D5
D4
D3
D2
D1
D0
RD
WR
CS
A0
A1
VSS
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VDD
RXAMPOUT
RXIN
VBIAS
TXOUT
DOC1
DOC2
XTAL/CLOCK
XTAL
A1
A0
CS
C7
C6
C5
C2
17
XTAL/CLOCK
X1
C3
R3
C4
16
XTAL

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±5%
R3		1MΩ	±20%
R4		100kΩ	±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	3		±20%

Component	Notes	Value	Tolerance
C4	3		±20%
C5	4		±5%
C6	5		±20%
C7	5		±20%
C8	4		±5%
X1	2		

Recommended External Component Notes:

1. See Section 4.1.10 Rx Input Amp.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. Crystal frequency tolerances are discussed in Section 4.5.3.4Control Register B1, B0: PLLBW - Phase-Locked Loop Bandwidth Modes.
4. Values C5 and C8 should be equal to 750,000 / symbol rate, e.g.

Symbol Rate	C5 and C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

5. Values C6 and C7 should be equal to 50,000 / symbol rate, e.g.

Symbol Rate	C6 and C7
2400 symbols/second	0.022μF
4800 symbols/second	0.01μF
9600 symbols/second	4700pF

4 General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host μC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the μC and the modem's internal registers according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$), and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address, and R/W Decode blocks provide a byte-wide parallel μC interface, which can be memory-mapped, as shown in Figure 3.

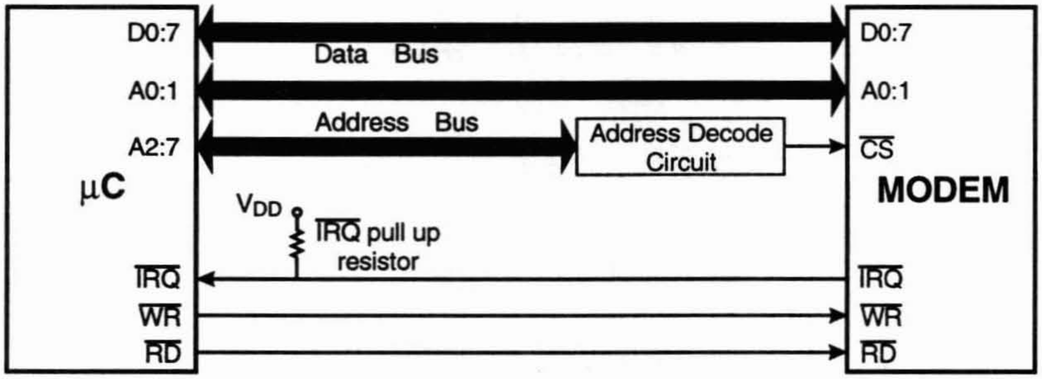

Figure 3: Typical Modem μC connections

4.1.3 Status and Data Quality Registers

Two 8-bit registers which the μC can read to determine the status of the modem and received data quality.

4.1.4 Command, Mode, and Control Registers

The values written by the μC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

A 12-byte buffer used to hold, receive or transmit data to or from the μC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in the transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-Interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give 0.2 x V_{DD} volts$_{P-P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see Section 5.4AC Coupling), otherwise the DC level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} ($V_{DD}/2$).

4.1.11 RRC Low Pass Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$H(f) = 1 \text{ for } 0 \le f < \frac{1-b}{2T}$$

$$H(f) = \sqrt{\frac{1}{2} - \frac{\sin\frac{(\pi Tf - \frac{\pi}{2})}{b}}{2}} \quad \text{for } \frac{1-b}{2T} \le f \le \frac{1+b}{2T}$$

$$H(f) = 0 \text{ for } f > \frac{1+b}{2T}$$

$$\text{Where } \quad b = 0.2, \quad T = \frac{1}{\text{symbol rate}}$$

This frequency response is illustrated in Figure 5 and Figure 6.

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels. The input applied to the RRC Tx filter may be impulses or full-width symbols depending on the setting of the Command Register TXIMP bit. See Section 4.7Transmitted Symbol Shape.

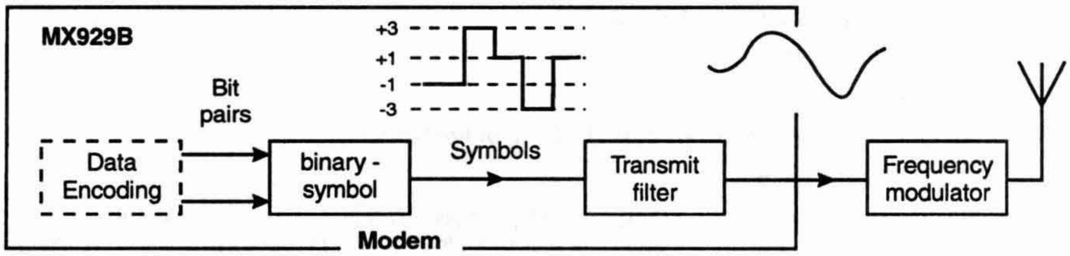

Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in Tx Mode

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols. The equalization characteristics are determined by the setting of the Command Register TXIMP bit.

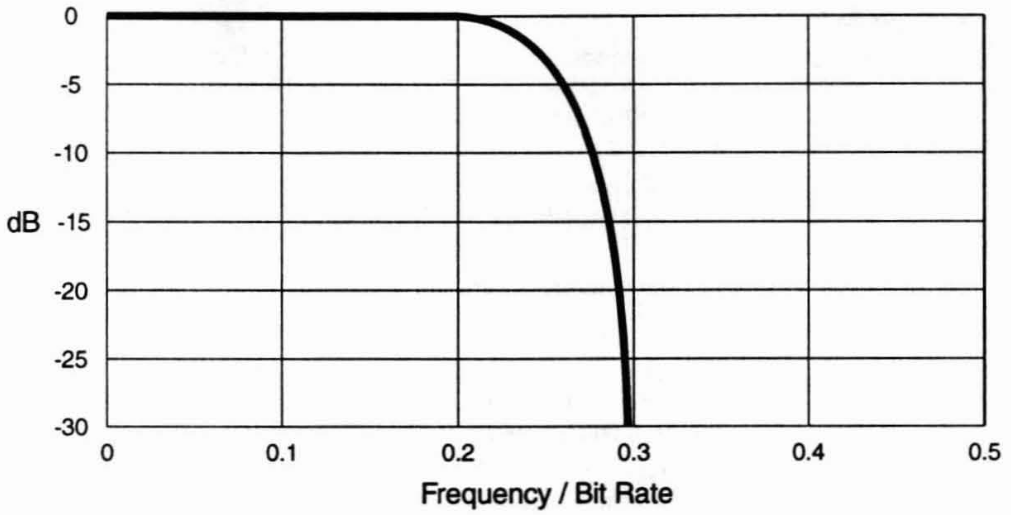

Figure 5: RRC Filter Frequency Response vs. Bit Rate (including the external RC filter R4/C5)

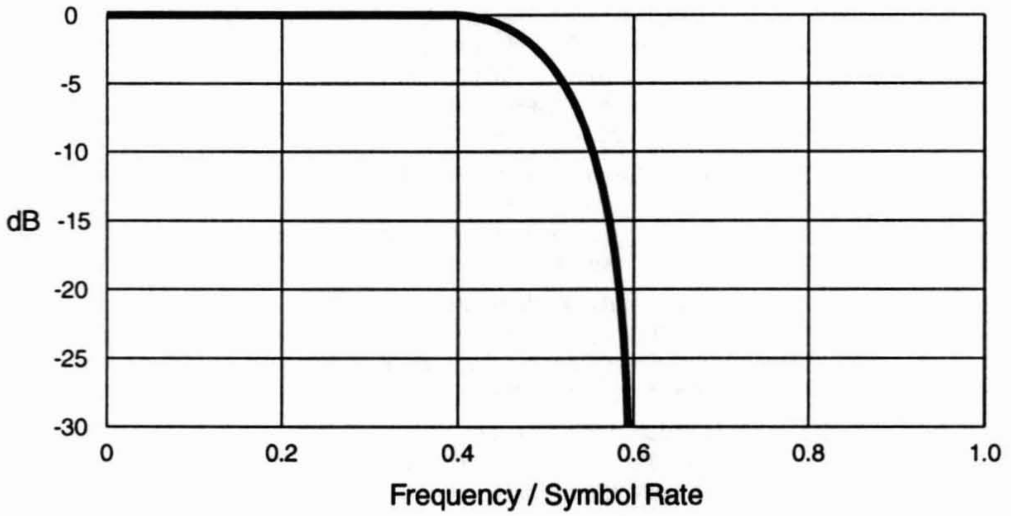

Figure 6: RRC Filter Frequency Response vs. Symbol Rate (including the external RC filter R4/C5)

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}, unless the RXEYE bit of the Control Register is '1', in which case it is connected to the received signal. When changing from Rx to Tx mode, the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any DC level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS}. It is approximately 0.2 x V_{DD} volts$_{P-P}$ for a continuous '+3 +3 -3 -3...' pattern with TXIMP = 0. For typical Tx Eye Diagrams refer to Section 4.7Transmitted Symbol Shape, Figure 17 and Figure 18. For typical Rx Eye Diagrams refer to Section 4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye, Figure 14.

A capacitor may be placed in series with the input to the frequency modulator if AC coupling is desired. See Section 5.4 AC Coupling.

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and DC offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

The capacitors C6 and C7 are driven from a very high impedance source so any measurement of the voltages on the DOC pins must be made via high input impedance (MOS input) voltage followers to avoid disturbance of the level measurement circuits.

Further details of the level and clock extraction functions are given in Section 5.3 Clock Extraction and Level Measurement Systems.

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4, and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4, and R3 should not be installed.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, and Interleaving. Details of the message formats handled by the modem are provided in Section 4.3 Binary to Symbol Translation, Figure 7, and Figure 8.

To reduce the processing load on the associated µC, the MX929B modem has been designed to perform as much of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) searching for and synchronizing onto the Frame Preamble. In normal operation, the modem will only require servicing by the µC once per received or transmitted block.

Therefore, to transmit a block, the controlling µC needs only to load the unformatted 'raw' binary data into the modem's Data Block Buffer, then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding), and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary, perform Forward Error Correction, and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data using the T4S, T24S, and R4S tasks as described in Sections 4.3 Binary to Symbol Translation and 4.5.2 Command Register. These tasks are normally used for the transmission of Symbol and Frame Synchronization sequences. These tasks may also be used for the transmission and reception of special test patterns or special data formats. In such a case, care should be taken to ensure that the transmitted TXOUT signal contains enough level and timing information for the receiving modem's level and clock extraction circuits to function correctly. See Section 5.3Clock Extraction and Level Measurement Systems.

4.3 Binary to Symbol Translation

Although the over-air signal, and therefore the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct way: (simplest form) - converts between two binary bits and a single symbol, such as the 'S' Channel Status symbol.

SYMBOL	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

Accordingly, 1 byte = 4 symbols = 8 bits, and one byte translates to four symbols for the T4S and R4S tasks and six bytes translates to twenty-four symbols for the T24S task described in Section 4.5.2 Command Register.

<table>
<tr><td></td><td colspan="2">MSB</td><td colspan="4"></td><td colspan="2">LSB</td></tr>
<tr><td>Bits:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Symbols:</td><td colspan="2">a</td><td colspan="2">b</td><td colspan="2">c</td><td colspan="2">d</td></tr>
<tr><td></td><td colspan="2">sent first</td><td colspan="4"></td><td colspan="2">sent last</td></tr>
</table>

2. FEC way: (more complicated) - essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, RHB, RILB, and RSID described in
Section 4.5.2 Command Register.

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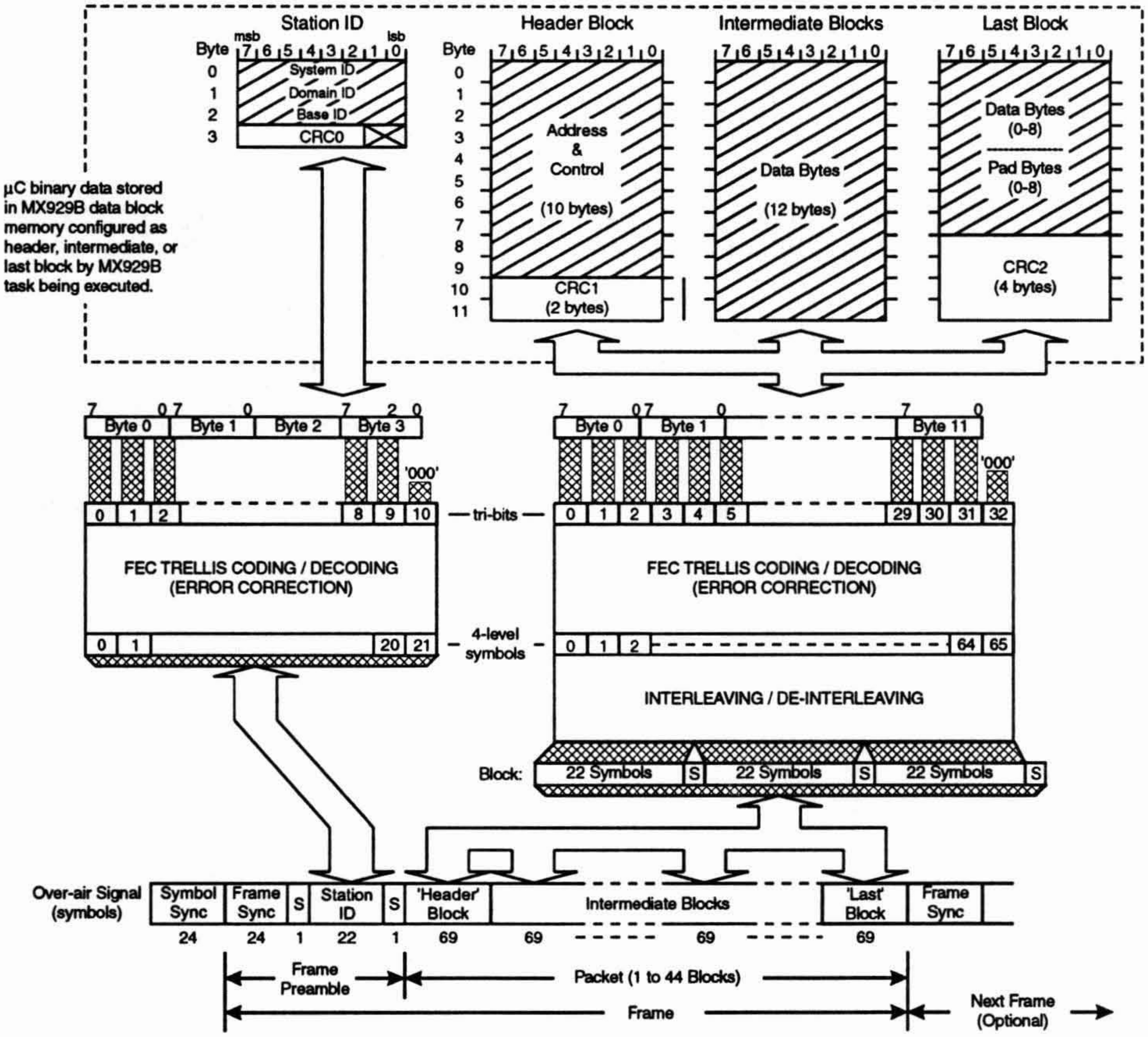
4.4 Frame Structure

The MX929B Frame Structure as used in a RD-LAP™ system is illustrated in Figure 7, and consists of a Frame Preamble (comprising a 24-symbol Frame Synchronization pattern and Station ID block), followed by a 'Header Block', one or more 'Intermediate Blocks', and a 'Last Block'. Channel Status (S) symbols are included at regular intervals. The first Frame of any transmission is preceded by a Symbol Synchronization pattern.



Station ID
msb
lsb
Byte
7 6 5 4 3 2 1 0
0
1
2
3
System ID
Domain ID
Base ID
CRC0
Header Block
Intermediate Blocks
Last Block
Byte
0
1
2
3
4
5
6
7
8
9
10
11
Address & Control (10 bytes)
CRC1 (2 bytes)
Data Bytes (12 bytes)
Data Bytes (0-8)
Pad Bytes (0-8)
CRC2 (4 bytes)
µC binary data stored in MX929B data block memory configured as header, intermediate, or last block by MX929B task being executed.
Byte 0
Byte 1
Byte 2
Byte 3
Byte 11
'000'
tri-bits
0 1 2 8 9 10
0 1 2 3 4 5 29 30 31 32
FEC TRELLIS CODING / DECODING (ERROR CORRECTION)
4-level symbols
0 1 20 21
0 1 2 64 65
INTERLEAVING / DE-INTERLEAVING
Block:
22 Symbols
S
Over-air Signal (symbols)
Symbol Sync
Frame Sync
S
Station ID
'Header' Block
Intermediate Blocks
'Last' Block
Frame Sync
24
24
1
22
1
69
69
69
69
Frame Preamble
Packet (1 to 44 Blocks)
Frame
Next Frame (Optional)

S: Channel Status Symbol: +3 = Busy, +1 = Unknown, -1 = Unknown, -3 = Idle

Frame Sync:	-1	+1	-1	+1	-1	+3	-3	+3	-3	-1	+1	-3	+3	+3	-1	+1	-3	-3	+1	+3	-1	-3	+1	+3
Symbol Sync:	+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	-3	-3	+3	+3

sent first … last

Figure 7: Over-Air Signal Format

The 'Header' block is self-contained and includes its own checksum (CRC1). It would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any), and miscellaneous control information. The number of following blocks (if any) is required to allow the Rx device software to expect the Last Block and interpret it as a Last Block rather than an Intermediate Block. There is no other indicator to differentiate a Last Block and an Intermediate Block.

The 'Intermediate' block(s) contain only data, the checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks.

Proprietary systems that do not use RD-LAP™ format may use the block structures provided by the MX929B to build alternative frame formats more suited to the particular application. Some examples are shown in Figure 7.

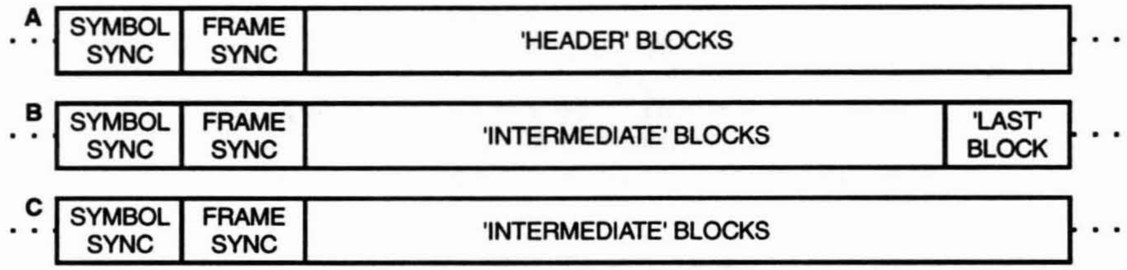


Figure 8: Alternative Frame Structures

The MX929B performs the entire block formatting and de-formatting required to convert data between the µC binary form and the Over-Air form as shown in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4 write only 8-bit registers, shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see Section 6.1.5 Timing.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer used to transfer data (as opposed to command, status, mode, and data quality or control information) between the modem and the host µC.

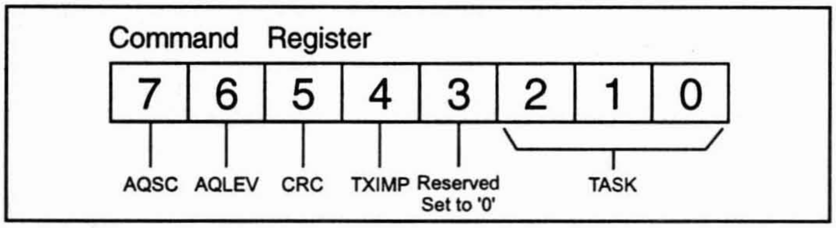
To the µC, the Data Block Buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode, the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific task as indicated by the TASK bits and modified by the AQSC, AQLEV, CRC, and TXIMP bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode, the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode, the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, but otherwise these received symbols are ignored.

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has AQSC = '1'.

The use of the symbol clock acquisition sequence is described in Section 5.3Clock Extraction and Level Measurement Systems.

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has AQLEV = '1'.

The use of the level measurement acquisition sequence (AQLEV) is described in Section 5.3 Clock Extraction and Level Measurement Systems.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different initial states of the CRC0, CRC1 and CRC2 checksum generators. When this bit is set to '1' the CRC generators are initialized to 'all zeros', as required by RD-LAP™ systems. When this bit is set to '0', the CRC generators are initialized to 'all ones' as required by CCITT X25 CRC based systems. It should always be set to '1' for RD-LAP™ compatibility. Other systems may set this bit as required.

4.5.2.4 Command Register B4: TXIMP - Tx Level/Impulse Shape

This bit allows the user to choose between two transmit symbol waveform shapes as described in Section 4.7Transmitted Symbol Shape.

Note: This bit must be set correctly every time the Command Register is written to.

4.5.2.5 Command Register B3 - Reserved

This bit should always be set to '0'.

4.5.2.6 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the μC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The μC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The μC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer, the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{\text{IRQ}}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the μC that it may write new data and the next task to the modem.

This lets the μC write the next task and its associated data to the modem while the modem is still transmitting the data from its previous task.

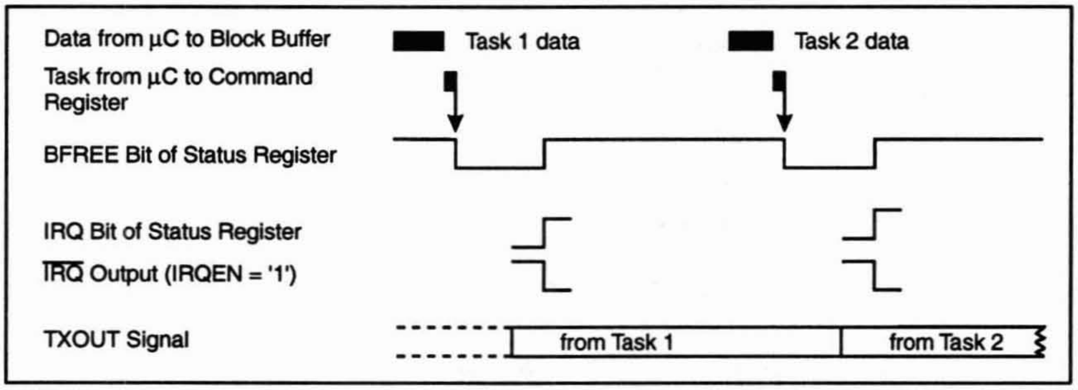

Data from μC to Block Buffer
Task 1 data
Task 2 data
Task from μC to Command Register
BFREE Bit of Status Register
IRQ Bit of Status Register
$\overline{\text{IRQ}}$ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the μC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{\text{IRQ}}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the μC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way, the μC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

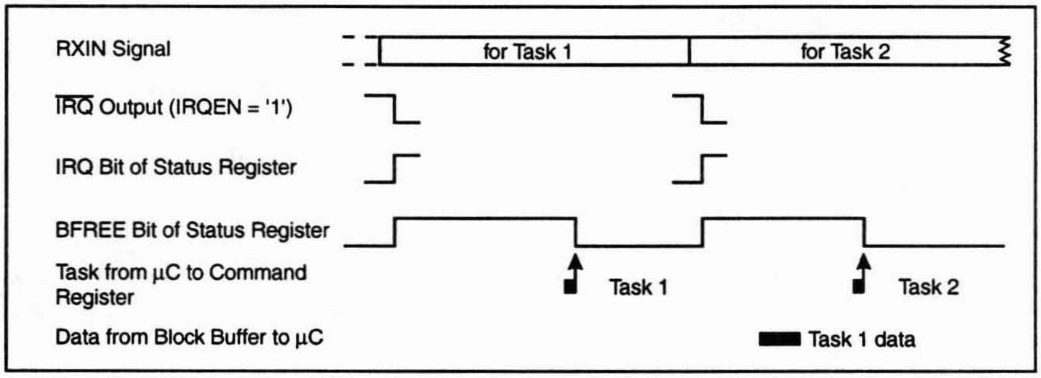

RXIN Signal
for Task 1
for Task 2
IRQ Output (IRQEN = '1')
IRQ Bit of Status Register
BFREE Bit of Status Register
Task from µC to Command Register
Task 1
Task 2
Data from Block Buffer to µC
Task 1 data

Figure 10: Receive Task Overlapping

Detailed timings for the various tasks are provide in Figure 11 and Figure 12.

MX929B Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFP	Search for Frame Preamble	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	RSID	Read Station ID	TSID	Transmit Station ID
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.5.2.7 NULL: No effect

This is provided so an AQSC or AQLEV command can be initiated without loading a new task.

4.5.2.8 SFP: Search for Frame Preamble

This task causes the modem to search the received signal for a valid 24-symbol Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID Block which has a correct CRC0 checksum.

The task continues until a valid Frame Preamble has been found.

The search consists of four stages:

> First the modem will attempt to match the incoming symbols against the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Control Register.
>
> Once a match has been found, the modem will read in the following 'S' symbol, place it in the SVAL bits of the Status Register then set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1').
>
> The modem will then read the next 22 symbols as station ID data. They will be decoded and the CRC0 checked. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.
>
> If the received CRC0 is correct, the following 'S' symbol will be read into the SVAL bits of the Status Register and the SRDY, BFREE, and IRQ bits set to '1', the CRCERR bit cleared to '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

Upon detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the three Station ID bytes from the Data Block Buffer and then write the next task to the modem's Command Register.

4.5.2.9 RHB: Read Header Block

This task causes the modem to read the next 69 symbols as a 'Header' Block. It will strip out the 'S' symbols then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer and, when the task is complete, setting the BFREE and IRQ bits of the Status Register to '1'to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

As each of the three 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

4.5.2.10 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block. (The µC can tell from the 'Header' block how many blocks are in the frame and therefore when to expect the 'Last' block).

In each case, it will strip out the three 'S' symbols, de-interleave, and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received, then the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register. For a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum.

As each of the three 'S' symbols of the block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

4.5.2.11 SFS: Search for Frame Sync

This task, which is intended for special test and channel monitoring purposes, performs the first two parts only of a SFP task. It causes the modem to search the received signal for a 24-symbol sequence, which matches the required Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ, and SRDY bits of the Status Register to '1' and update the SVAL bits. The µC may then write the next task to the Command Register.

4.5.2.12 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register are then set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by a SFS task.

Note: It is possible to construct message formats, which do not rely on the block formatting of the THB, TIB, and TLB tasks. This can be accomplished by using T4S or T24S tasks to transmit and R4S to receive the user's data. One should be aware, that the receive level and timing measurement circuits need to see a reasonably 'random' distribution of all four possible symbols in the received signal to operate correctly. Accordingly, binary data may benefit from scrambling before transmission if it is not reasonably 'random' to start with.

4.5.2.13 RSID: Read Station ID

This task causes the modem to read in and decode the following 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of a SFP task except that it will not restart if the received CRC0 is incorrect. It would normally follow a SFS task.

The three decoded bytes will be placed into the Data Block Buffer, and the CRCERR bit of the Status Register set to '1' if the received CRC0 is incorrect, otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY, and IRQ bits set to '1' to indicate that the µC may read the three received bytes from the Data Block buffer and write the next task to the modem's Command Register.

4.5.2.14 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC, interleaving, or adding any 'S' symbols.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data needs to be written to the Data Block Buffer to transmit the MX929B Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
-3	-3	+3	+3	Byte 5:	01011111	5F

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

4.5.2.15 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Header' Block, inserting 'S' symbols at 22 symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Intermediate' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.17 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Last' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.18 T4S: Transmit 4 Symbols

This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

4.5.2.19 TSID: Transmit Station ID

This task takes three ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.20 RESET: Stop any current action

This task takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used after V_{DD} is applied first to set the modem into a known state.

Note: Due to delays in the RRC filter, it will take several symbol times for any change caused by RESET to appear at the TXOUT pin.

4.5.2.21 Task Timing

The following table and figures describe the duration of tasks and timing sequences for Tx and Rx operation.

		Task	**Time (symbol times)**
t_1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t_2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1'	T24S TSID THB/TIB/TLB T4S	5 6 16 0
t_3	Time to transmit all symbols of the task	T24S/TSID THB/TIB/TLB T4S	24 69 4
t_4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S TSID THB/TIB/TLB T4S	18 17 52 3
t_5	Time to receive all symbols of task	SFS SFP RSID RHB/RILB R4S	25 (minimum) 48 (minimum) 23 69 4
t_6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS SFP RSID RHB/RILB R4S	21 21 15 51 3
t_7	Maximum time from the last bit of the task entering the de interleave circuit to BFREE going to a logic '1' (high)	Any	1

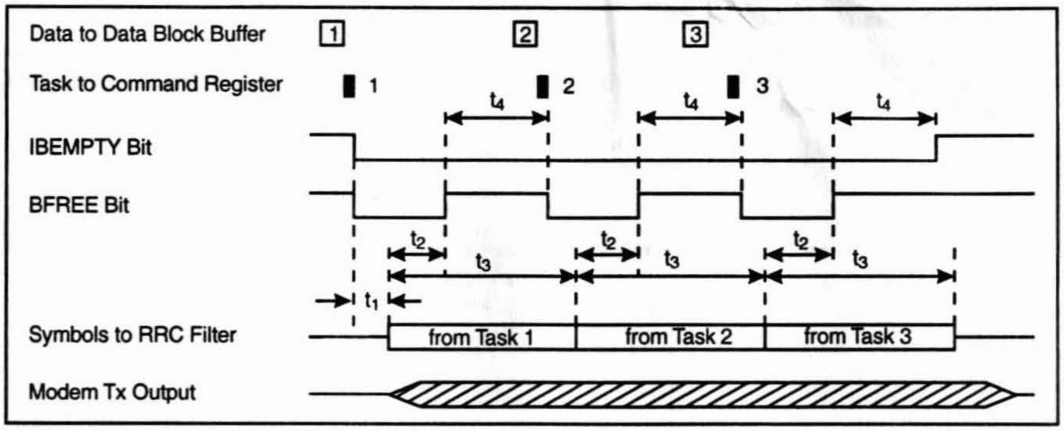

Data to Data Block Buffer
1
2
3
Task to Command Register
1
2
3
t_4
t_4
t_4
IBEMPTY Bit
BFREE Bit
t_2
t_2
t_2
t_3
t_3
t_3
t_1
Symbols to RRC Filter
from Task 1
from Task 2
from Task 3
Modem Tx Output

Figure 11: Transmit Task Timing Diagram

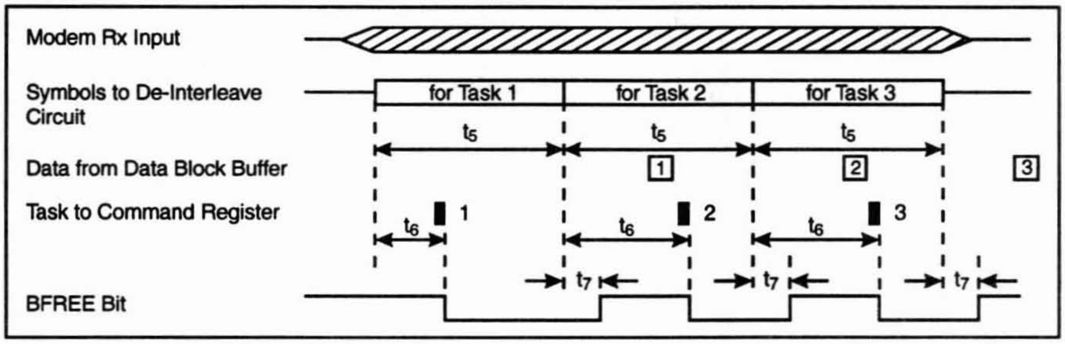

Modem Rx Input
Symbols to De-Interleave Circuit
for Task 1
for Task 2
for Task 3
t_5
t_5
t_5
Data from Data Block Buffer
1
2
3
Task to Command Register
t_6
1
t_6
2
t_6
3
t_7
t_7
t_7
BFREE Bit

Figure 12: Receive Task Timing Diagram

4.5.2.22 RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below:

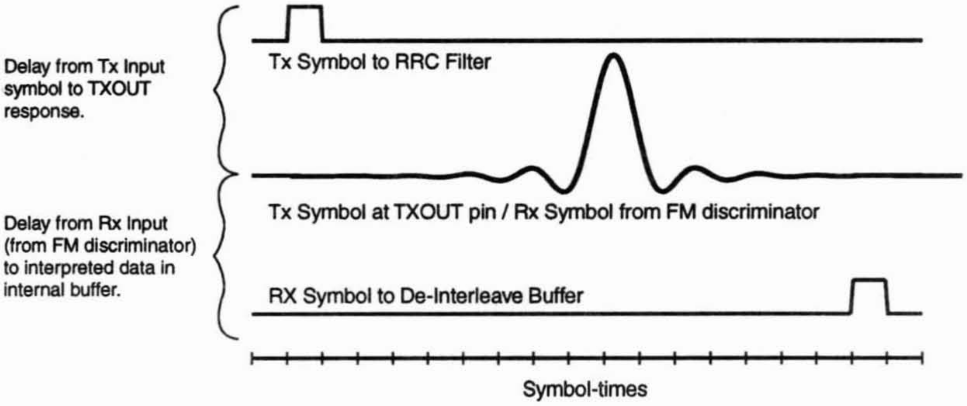
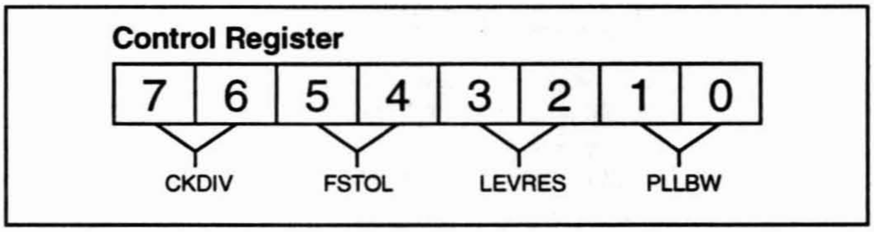

Delay from Tx Input symbol to TXOUT response.
Delay from Rx Input (from FM discriminator) to interpreted data in internal buffer.
Tx Symbol to RRC Filter
Tx Symbol at TXOUT pin / Rx Symbol from FM discriminator
RX Symbol to De-Interleave Buffer
Symbol-times

Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction, signal level measurement circuits, and the Frame Sync pattern recognition tolerance to inexact matches.



4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{\text{XTAL}}$ pin, therefore determining the nominal symbol rate. Because each symbol represents two bits, bit rates are 2x the symbol rates. The table below shows how symbol rates of 2400/4800/9600 symbols/sec (4800/9600/19200bps) may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	**B6**	**Division Ratio: Xtal Frequency/Symbol Rate**	**Symbol Rate (symbols/sec) / Bit Rate (bps)**		
0	0	512	4800/9600	9600/19200	
0	1	1024	2400/4800	4800/9600	9600/19200
1	0	2048		2400/4800	4800/9600
1	1	4096			2400/4800

Note: Device operation is not guaranteed below 2400 symbols/sec (4800bps) or above 9600 symbols/sec (19200bps).

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance to Inexact Matches

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches allowed during a search for the Frame Sync pattern:

B5	**B4**	**Mismatches allowed**
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches. A setting of '4 mismatches' is recommended for normal use.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' or 'steady state' operating mode of the Rx signal amplitude and DC offset measuring and tracking circuits. These circuits analyze the Rx signal envelope and charge the DOC1 and DOC2 capacitors to 'store' signal maximum and minimum references that are used in the data reception process. This setting is temporarily overridden during the automatic sequencing triggered by an AQLEV command when level is initially being acquired as described in Section 5.3 Clock Extraction and Level Measurement Systems.

B3	B2	Mode
0	0	Hold
0	1	Level Track
1	0	Lossy Peak Detect
1	1	Slow Peak Detect

In normal use the LEVRES bits should be set to '0 1' (Level Track). The other modes are intended for special purposes, for device testing, or are invoked automatically during an AQLEV sequence.

In 'Slow Peak Detect' modes, the positive and negative excursions of the received signal (after filtering) are measured by peak rectifiers driving the DOC1 and DOC2 capacitors to establish the amplitude of the signal and any DC offset with regards to V_{BIAS}. This mode provides good overall performance, particularly when acquiring level information at the start of a received message, but does not work as well with certain long sequences of repeated data byte values. It is also susceptible to large amplitude noise spikes, which can be caused by deep fades.

The 'Lossy Peak Detect' mode is similar to 'Slow Peak Detect' but the capacitor discharge time constant is much shorter so this mode is not suitable for normal data reception and is only used within part of the automatic AQLEV acquisition sequence.

In 'Level Track' mode the DOC capacitor voltages are slowly adjusted by the MX929B in such a way as to minimize the average errors seen in the received signal. This mode provides the best overall performance, being much more accurate than 'Slow Peak Detect' when receiving large amplitude noise spikes on long sequences of repeated data byte values. It does, however, depend on the measured levels and timing being approximately correct. If either of these is significantly wrong then the correction algorithm used by the 'Level Track' mode can actually drive the voltages on the DOC capacitors away from their optimum levels. For this reason, the automatic AQLEV acquisition sequence (see Section 5.3Clock Extraction and Level Measurement Systems) forces the level measuring circuits into 'Slow Peak Detect' mode until a Frame Sync pattern has been found.

In 'HOLD' mode the DOC Capacitors are isolated from the charging and discharging circuits, allowing their voltages to remain constant.

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Bandwidth Modes

These two bits have no effect in transmit mode. In receive mode, they set the 'normal' or 'steady state' bandwidth of the Rx clock extraction Phase Locked Loop circuit. The PLL circuit synchronizes itself with the Rx Signal to develop a local clock signal used in the data clock recovery process. This setting will be temporarily overridden during the automatic sequencing of an AQSC command when Rx clock extraction circuits are initially being trained as described in Section 5.3Clock Extraction and Level Measurement Systems.

B1	B0	PLL Mode
0	0	Hold
0	1	Narrow Bandwidth
1	0	Medium Bandwidth
1	1	Wide Bandwidth

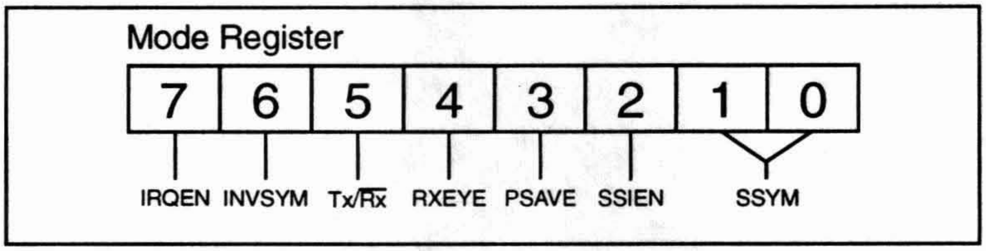
The normal setting for the PLLBW bits should be 'Medium Bandwidth' when the received symbol rate and the frequency of the receiving modem's crystal are both within ±100ppm of nominal, except at the start of a symbol clock acquisition sequence (AQSC) when 'Wide Bandwidth' should be selected as described in Section 5.3Clock Extraction and Level Measurement Systems.

If the received symbol rate and the crystal frequency are both within ±20ppm of nominal then selection of the 'Narrow Bandwidth' setting will provide better performance especially through fades or noise bursts which may otherwise pull the PLL away from its optimum timing. In this case however; it is recommended that the PLLBW bits only be set to 'Narrow Bandwidth' after the modem has been running in 'Medium Bandwidth' mode for about 200 symbol times to ensure accurate lock has first been achieved.

The 'Hold' setting disables the feedback loop of the PLL which continues to run at a rate determined only by the actual crystal frequency and the setting of the Control Register CKDIV bits, not the PLL's operating frequency immediately prior to the 'Hold' setting.

4.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (V_{SS}) given the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

Note: B6 must be normally set to the same value in Tx and Rx devices for successful communication between them.

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' places the modem into the Transmit mode, clearing it to '0' puts the modem into the Receive mode.

Note: Changing between receive and transmit modes will cancel any current task.

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'. Setting it to '1' when the modem is in receive mode configures the modem for a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters, and FM demodulator.

This mode is provided because observation of the direct discriminator output of a root raised cosine Tx filtered signal (before Rx equalization) is not very recognizable so it is generally not useful.

The resulting eye diagram (for reasonably random data) should ideally be as shown Figure 14, with 4 distinct and equally spaced level crossing points.

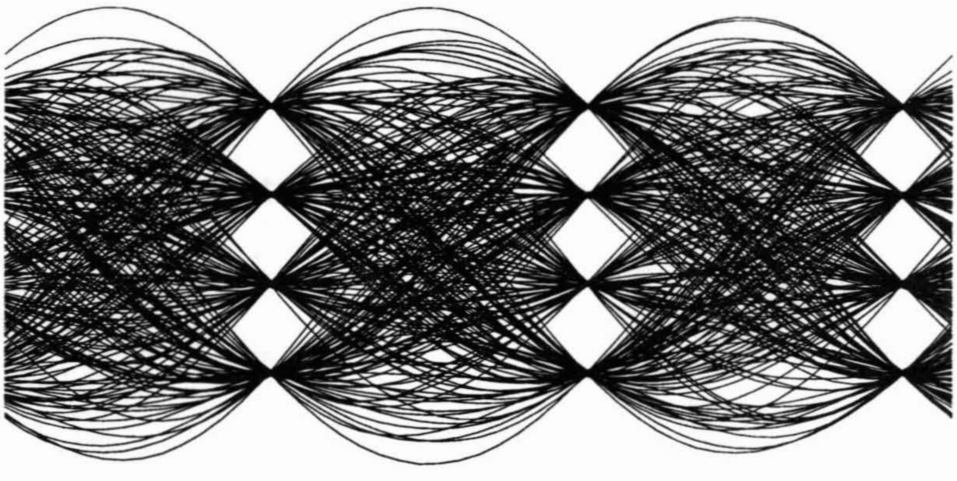


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol and Clock extraction circuits, and the Tx output buffer will be disabled. The TXOUT pin will be connected to V_{BIAS} through a high value internal resistance. The Xtal clock oscillator, Rx input amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

Note: The internal filters, and therefore the TXOUT pin in transmit mode, will take approximately 20 symbol-times to settle after the PSAVE bit has gone from '1' to '0'.

4.5.4.6 Mode Register B2: SSIEN - 'S' Symbol IRQ Enable

In receive mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will also be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.)

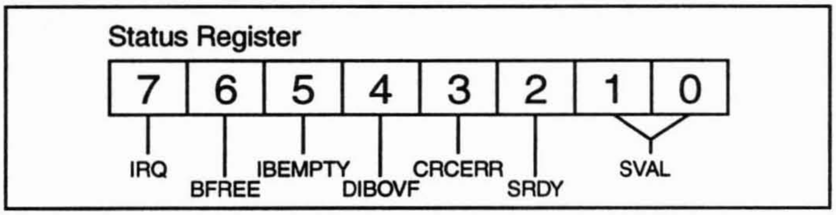
In transmit mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a 'S' symbol has been transmitted. (The SRDY bit of the Status Register will also be set to '1' at the same time.)

4.5.4.7 Mode Register B1, B0: SSYM - 'S' Symbol To Be Transmitted

In transmit mode, these two bits define the next 'S' symbol to be transmitted. These bits have no effect in receive mode.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register $TX/\overline{RX}$ or PSAVE bits

or The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register $TX/\overline{RX}$ or PSAVE bits.

or The Status Register DIBOVF bit going from '0' to '1'.

or The Status Register SRDY bit being set to '1' (due to a 'S' symbol being received or transmitted) if the Mode Register SSIEN bit is '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (V_{SS}) when the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' when a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register $TX/\overline{RX}$ or PSAVE bits are changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register $TX/\overline{RX}$ or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level (halfway between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB, RSID, or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the $TX/\overline{RX}$ or PSAVE bits of the Mode Register.

In transmit mode this bit is '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode, this bit will be updated at the end of a SFP, RHB, RILB, or RSID task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task or by changing the $TX/\overline{RX}$, or PSAVE bits of the Mode Register. In transmit mode this bit is '0'.

4.5.5.6 Status Register B2: 'S' Symbol Ready

In receive mode, this bit is set to '1' whenever an 'S' symbol has been received. The µC may then read the value of the symbol from the SVAL field of the Status Register. In transmit mode, this bit is set to '1' whenever an 'S' symbol has been transmitted.

The bit is cleared to '0' immediately after a read of the Status Register, by a RESET task or by changing the $TX/\overline{RX}$ or PSAVE bits of the Mode Register.

4.5.5.7 Status Register B1, B0: SVAL - Received 'S' Symbol Value

In receive mode, these two bits reflect the value of the latest received 'S' symbol. In transmit mode, these two bits will be '0'.

4.5.6 Data Quality Register

In receive mode, the MX929B continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal' 4-level FSK baseband signal.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

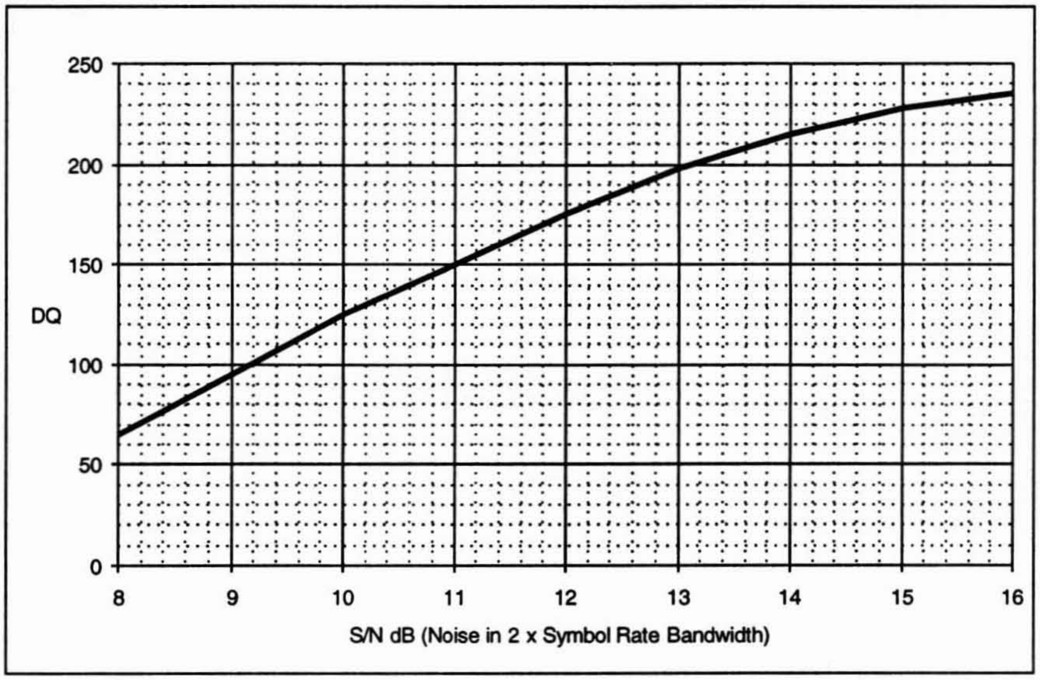


Figure 15: Typical Data Quality Reading vs S/N

The Data Quality readings are only valid when the modem has successfully acquired signal level and timing lock for at least 64 symbol times. It is invalid when an AQSC or AQLEV sequence is being performed or when the LEVRES setting is 'Lossy Peak Detect'. A low reading will be obtained if the PLLBW bits are set to 'Wide' or if the received signal waveform is distorted in any significant way.

Section 5.6Received Signal Quality Monitor describes how monitoring the Data Quality reading can help improve the overall system performance in some applications.

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC0

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0, 1, and 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23 such that the MSB bit (7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of x^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the modulo-2 division.

$$\frac{x^6 M(x)}{(x^6 + x^4 + x^3 + 1)}$$

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x).

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the MSB of CRC0

4.6.1.2 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block, which provides error detection coverage for the Header Block of a message. It is calculated by the modem from the first 80 bits of the Header Block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

4.6.1.3 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block, which provides error detection coverage for the combined Intermediate Blocks and Last Block of a message. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB, or TLB.

Command Register bit B5 (CRC) allows the user to select between two different forms of the CRC0, CRC1 and CRC2 checksums. When this bit is set to '1' the CRC generators are initialized to 'all zeros', as required by RD-LAP™ systems. When this bit is set to '0', the CRC generators are initialized to 'all ones' for calculations such as CCITT X25 based systems. It should always be set to '1' for RD-LAP™ compatibility, other systems may set this bit as required.

4.6.1.4 Forward Error Correction

In transmit mode, the MX929B uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate', 'Last' Block, into a 66 symbol (132 bits) sequence which includes FEC information. Station ID Blocks (30 bits) are translated into a 22 symbol (44 bit) sequence which includes FEC information.

In receive mode, the MX929B decodes the received 22 or 66 symbols of a block into 30 or 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.1.5 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission (and before the 'S' symbols are added) to provide protection against the effects of noise bursts and short fades. The 22 symbols of a 'Station ID' Block are not interleaved.

In receive mode, the MX929B strips out the 'S' symbols and then de-interleaves the received symbols. FEC and decoding follow.

4.7 Transmitted Symbol Shape

Bit 4 of the Command Register (TXIMP) selects the transmit baseband signal and the receive signal equalization as follows:

If the TXIMP bit is '0', then the transmit baseband signal is generated by feeding full-symbol-time-width 4-level symbols into the RRC lowpass filter and the receive signal equalization is optimized for this type of signal. With this setting, the MX929B is compatible with the MX929A device, another member of the MX929 device family.

If the TXIMP bit is set to '1,' impulses, rather than full-symbol-time-width symbols are fed into the RRC filter when in TX mode and the receive signal equalization is suitably adjusted in RX mode.

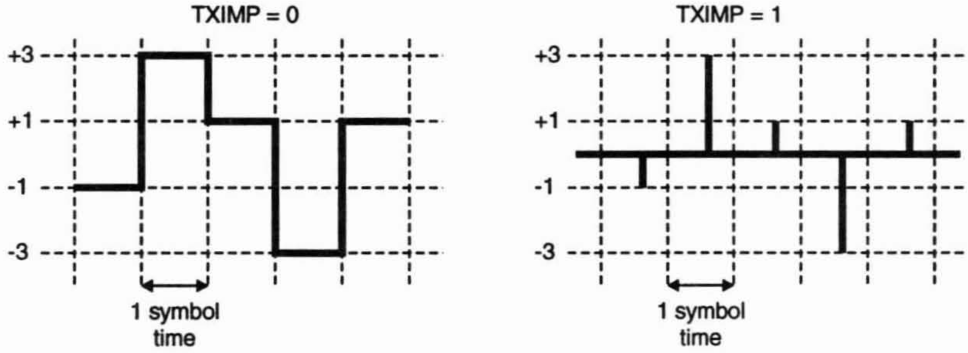


Figure 16: Input Signal to RRC Filter in Tx Mode for TXIMP = 0 and 1

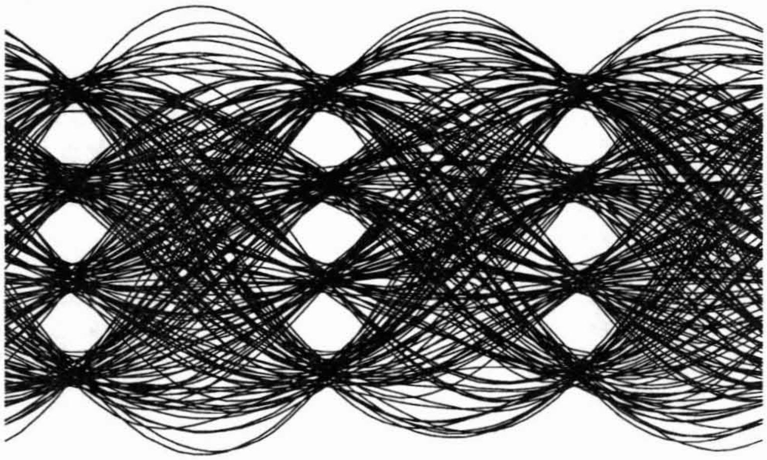


Figure 17: Tx Signal Eye TXIMP = 0

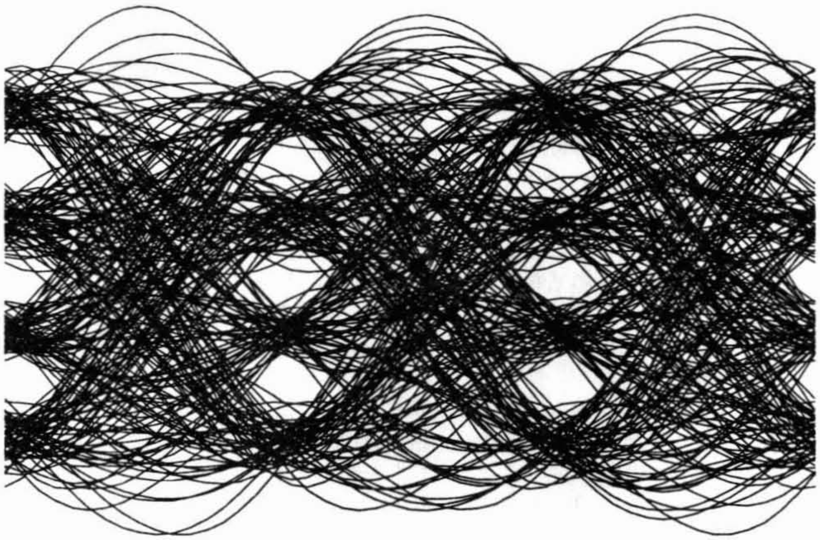


Figure 18: Tx Signal Eye TXIMP = 1

Note: Setting TXIMP to '1' affects the Tx output signal level as shown in Section 6.1 Electrical Performance and the table below.

	TXIMP = 0	**TXIMP = 1**
Nominal Voltage difference between continuous '+3' and continuous '-3' symbol outputs.	$0.157V_{DD}$	$0.157V_{DD}$
Nominal V_{P-P} for continuous '+3 +3 -3 -3..." symbol pattern.	$0.20V_{DD}$	$0.22V_{DD}$

5 Application

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, and one each Header, Intermediate and Last blocks are provided below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and $TX/\overline{RX}$ bits of the Mode Register are '1', the RXEYE, PSAVE, and SSIEN bits are '0', and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes (a preamble) to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write the 6 byte Frame Sync to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 3 Station ID bytes to the Data Block Buffer and a TSID task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
13. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
14. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Notes:

1. The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.
2. The SSYM bits of the Mode Register may be altered at any time to change the transmitted 'S' symbols. If a timing reference is required, then setting the Mode Register SSIEN bit to '1' will cause a µC interrupt after every 'S' symbol transmitted, in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.
3. Figure 19 and Figure 20 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header block, and any number of Intermediate blocks and one Last Block. It is assumed that the Tx Interrupt Service Routine Figure 20 is called every time the MX929B $\overline{IRQ}$ output line goes low.

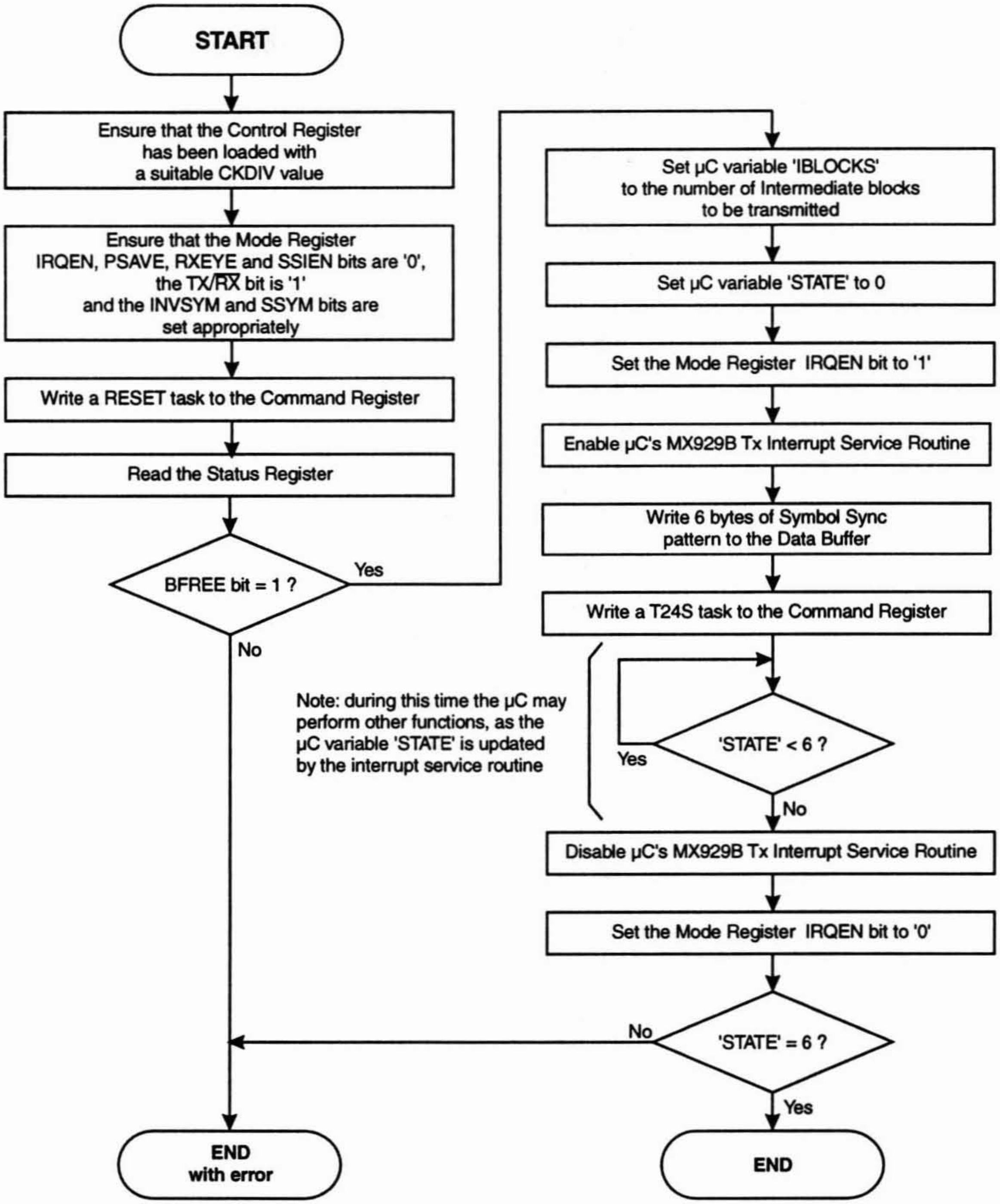
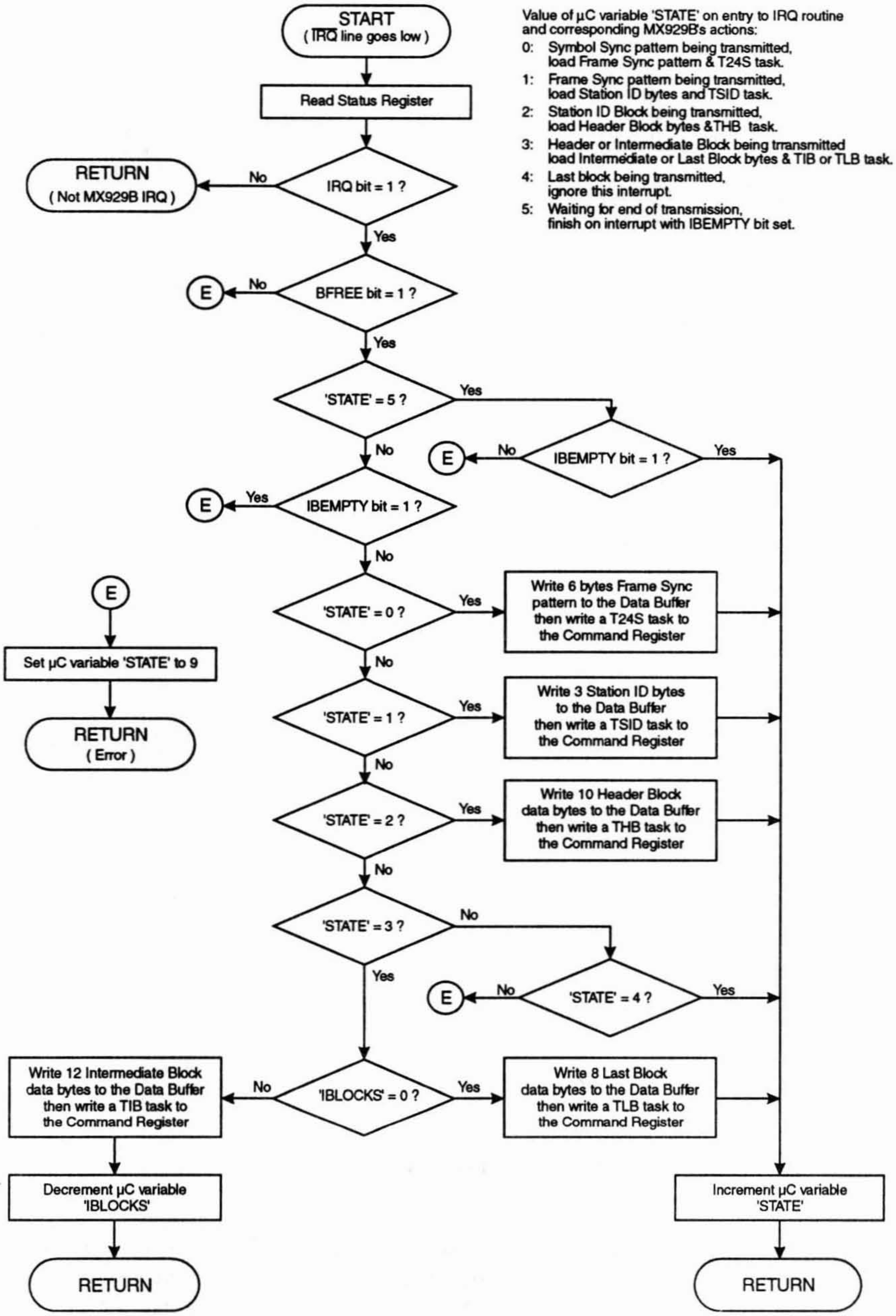

START
Ensure that the Control Register has been loaded with a suitable CKDIV value
Ensure that the Mode Register IRQEN, PSAVE, RXEYE and SSIEN bits are '0', the TX/RX bit is '1' and the INVSYM and SSYM bits are set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Set µC variable 'IBLOCKS' to the number of Intermediate blocks to be transmitted
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX929B Tx Interrupt Service Routine
Write 6 bytes of Symbol Sync pattern to the Data Buffer
Write a T24S task to the Command Register
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 6 ?
Yes
No
Disable µC's MX929B Tx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 6 ?
No
Yes
END with error
END

Figure 19: Transmit Frame Example Flowchart, Main Program

Notes:

1. The RESET command in Figure 19 and the practice of disabling the MX929B's $\overline{\text{IRQ}}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.


START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX929B IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
'STATE' = 5 ?
Yes
IBEMPTY bit = 1 ?
No
E
Yes
No
IBEMPTY bit = 1 ?
Yes
E
No
E
Set μC variable 'STATE' to 9
RETURN
(Error)
'STATE' = 0 ?
Yes
Write 6 bytes Frame Sync pattern to the Data Buffer then write a T24S task to the Command Register
No
'STATE' = 1 ?
Yes
Write 3 Station ID bytes to the Data Buffer then write a TSID task to the Command Register
No
'STATE' = 2 ?
Yes
Write 10 Header Block data bytes to the Data Buffer then write a THB task to the Command Register
No
'STATE' = 3 ?
No
'STATE' = 4 ?
No
E
Yes
Yes
'IBLOCKS' = 0 ?
No
Write 12 Intermediate Block data bytes to the Data Buffer then write a TIB task to the Command Register
Yes
Write 8 Last Block data bytes to the Data Buffer then write a TLB task to the Command Register
Decrement μC variable 'IBLOCKS'
RETURN
Increment μC variable 'STATE'
RETURN

Value of μC variable 'STATE' on entry to IRQ routine and corresponding MX929B's actions:

0: Symbol Sync pattern being transmitted, load Frame Sync pattern & T24S task.
1: Frame Sync pattern being transmitted, load Station ID bytes and TSID task.
2: Station ID Block being transmitted, load Header Block bytes &THB task.
3: Header or Intermediate Block being trransmitted load Intermediate or Last Block bytes & TIB or TLB task.
4: Last block being transmitted, ignore this interrupt.
5: Waiting for end of transmission, finish on interrupt with IBEMPTY bit set.

Figure 20: Tx Interrupt Service Routine

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences, Station ID Block, and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the $TX/\overline{RX}$, RXEYE, PSAVE, and SSIEN bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see Section 5.3 Clock Extraction and Level Measurement Systems).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFP task and with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Read 3 Station ID bytes from the Data Block Buffer.
7. Write a RHB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
10. Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Read 12 Intermediate Block bytes from the Data Block Buffer.
13. Write a RILB task to the Command Register.
14. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
15. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from the Data Buffer.

Note:

1. The value of the latest 'S' symbol received will be contained in the SVAL bits each time the Status Register is read. If desired, the Mode Register SSIEN bit may be set to '1', which will cause a µC interrupt after every 'S' symbol received, in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1' and those caused by SRDY bit being set to '1'.
2. Figure 21 and Figure 22 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header Block, any number of Intermediate blocks and one Last block. It is assumed that the Rx Interrupt Service Routine Figure 22 is called every time the MX929B's $\overline{IRQ}$ output goes low.

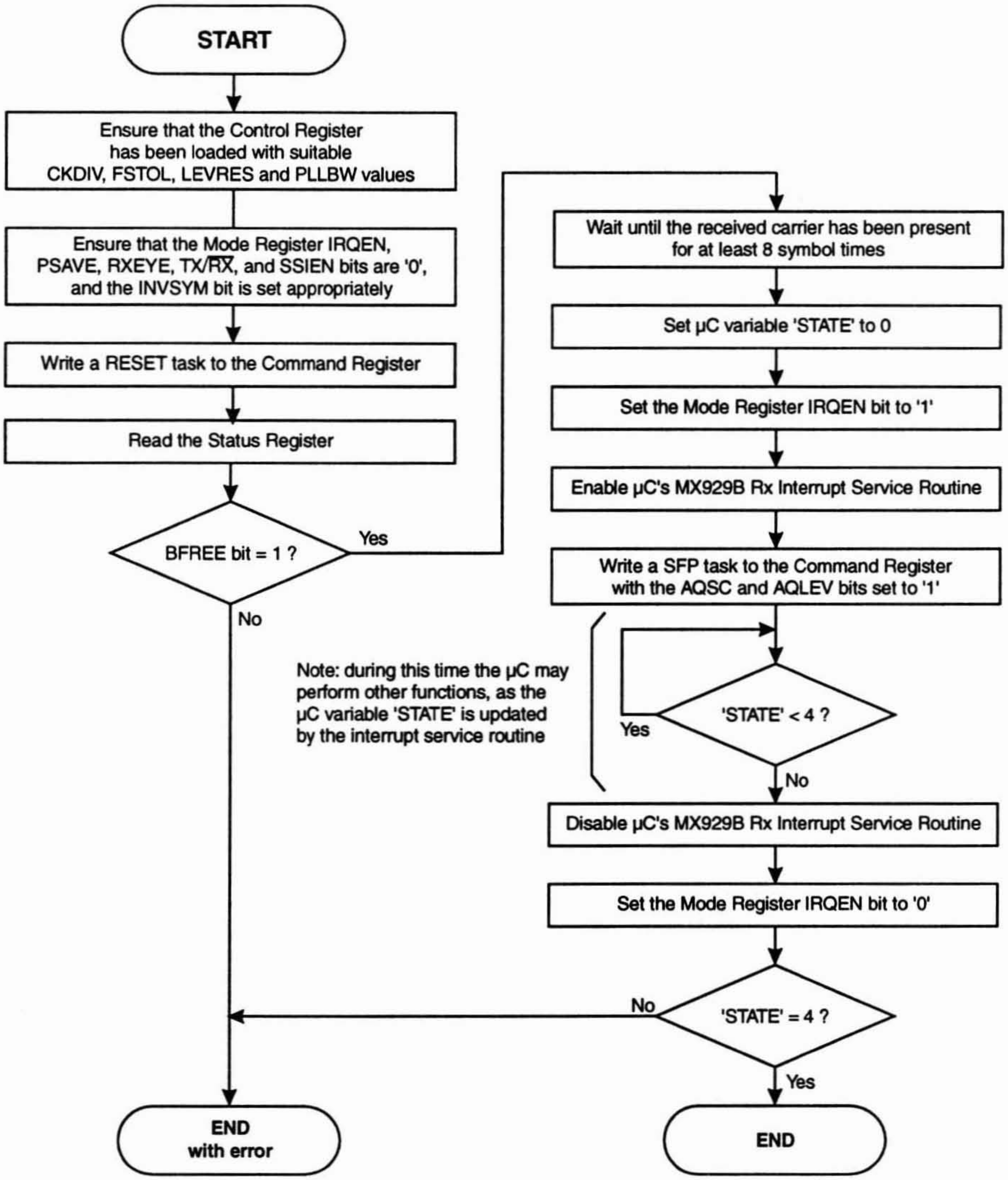
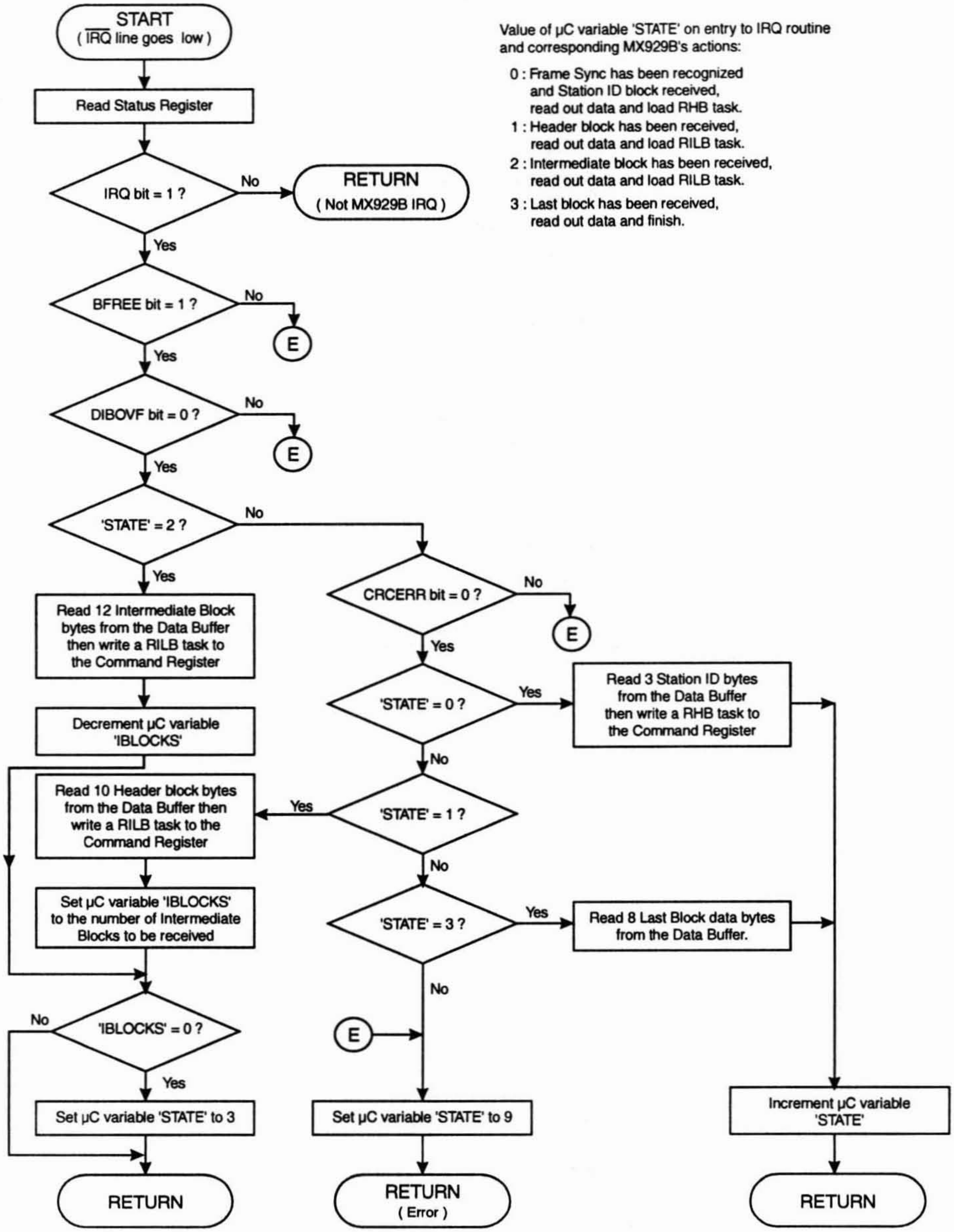

START
Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values
Ensure that the Mode Register IRQEN, PSAVE, RXEYE, TX/$\overline{RX}$, and SSIEN bits are '0', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Wait until the received carrier has been present for at least 8 symbol times
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX929B Rx Interrupt Service Routine
Write a SFP task to the Command Register with the AQSC and AQLEV bits set to '1'
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 4 ?
Yes
No
Disable µC's MX929B Rx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 4 ?
No
Yes
END with error
END

Figure 21: Receive Frame Example Flowchart, Main Program

Notes

1. The RESET command in Figure 21 and the practice of disabling the MX929B's $\overline{IRQ}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation.
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.


START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX929B IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
DIBOVF bit = 0 ?
No
E
Yes
'STATE' = 2 ?
No
Yes
Read 12 Intermediate Block bytes from the Data Buffer then write a RILB task to the Command Register
CRCERR bit = 0 ?
No
E
Yes
'STATE' = 0 ?
Yes
Read 3 Station ID bytes from the Data Buffer then write a RHB task to the Command Register
Decrement µC variable 'IBLOCKS'
No
Read 10 Header block bytes from the Data Buffer then write a RILB task to the Command Register
Yes
'STATE' = 1 ?
No
Set µC variable 'IBLOCKS' to the number of Intermediate Blocks to be received
'STATE' = 3 ?
Yes
Read 8 Last Block data bytes from the Data Buffer.
No
No
'IBLOCKS' = 0 ?
E
Yes
Set µC variable 'STATE' to 3
Set µC variable 'STATE' to 9
Increment µC variable 'STATE'
RETURN
RETURN
(Error)
RETURN

Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX929B's actions:

0 : Frame Sync has been recognized and Station ID block received, read out data and load RHB task.
1 : Header block has been received, read out data and load RILB task.
2 : Intermediate block has been received, read out data and load RILB task.
3 : Last block has been received, read out data and finish.

Figure 22: Rx Interrupt Service routine

Note: This routine assumes that the number of Intermediate blocks in the Frame is contained within the Header Block Data.

5.3 Clock Extraction and Level Measurement Systems

5.3.1 Supported Types of Systems

The MX929B is intended for use in systems where:

1. The Symbol Sync pattern is transmitted immediately on start-up of the transmitter, before the first Frame Sync pattern (see Figure 23).
2. A Base Station may remain powered up indefinitely, transmitting concatenated Frames with or without intervening Symbol Sync patterns (each Frame starting with the Frame Sync pattern and symbol timing being maintained from one Frame to the next).
3. A receiving modem may be switched onto a channel before the distant transmitter has started up or may be switched onto a channel where the transmitting station is already sending concatenated Frames.

5.3.2 Clock and Level Acquisition Procedures with RF Carrier Detect

When the receiving modem is enabled or switched onto a channel, it needs to establish the received symbol levels, clock timing, and look for a Frame Sync pattern in the incoming signal. This is best done by the following procedure:

1. Ensure that the Control Register's PLLBW bits are set to 'Wide' and the LEVRES bits to 'Level Track'.
2. Wait until a received carrier has been present for 8 symbol times. This 8-symbol delay gives time for the received signal to propagate through the modem's RRC filter. An 'RF received 8 symbol times' qualifying function can be included in a radio's carrier detect circuitry to take this into account.
3. Write a SFS or SFP task to the Command Register with the AQSC and the AQLEV bits set to '1'.
4. When the modem interrupts to signal that it has recognized a Frame Sync pattern (or completed the SFP task) then change the PLLBW bits to 'Medium'.

Once the receiving modem has achieved level and symbol timing synchronization with a particular channel - as evidenced by recognition of a Frame Sync pattern - then subsequent concatenated Frames can be read by simply issuing SFS or SFP tasks at appropriate times, keeping the ASQSC and AQLEV bits at zero, and the PLLBW and LEVRES bits at their current 'Medium' and 'Level Track' settings, respectively.

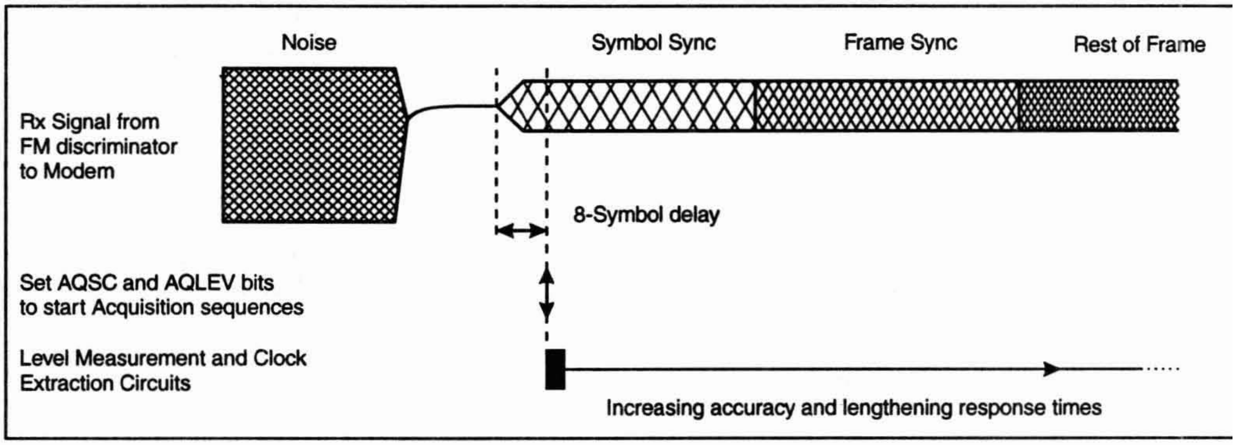

Noise
Symbol Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
8-Symbol delay
Set AQSC and AQLEV bits to start Acquisition sequences
Level Measurement and Clock Extraction Circuits
Increasing accuracy and lengthening response times

Figure 23: Acquisition Sequence Timing

5.3.3 Clock and Level Acquisition Procedure without RF Carrier Detect

It is also possible to use the modem in a non-standard system where there is an indeterminate delay between the RF transmitter turn on time and the transmission moment of the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC, or where the transmitting terminal can send separate unsynchronized Frames. In these cases, each Frame should be preceded by a Symbol Sync pattern which should be extended to about 100 symbols and the procedure provided in Section 5.3.2 Clock and Level Acquisition Procedures with RF Carrier Detect used.

5.3.4 Automatic Acquisition Functions

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude, and DC offset as quickly as possible before switching to accurate - but slower - measurement modes. These acquisition sequences act very quickly if triggered at the start of a received Symbol Sync pattern (as shown in Figure 23), but will still function correctly, although more slowly, if started any time during a normal Frame as when the receiver is switched onto a channel where the transmitter is operating continuously.

The automatic AQLEV Level Measurement acquisition sequence starts with the level measurement circuits being put into 'Clamp' Mode for one symbol time to quickly set the voltages on the DOC pins to approximately correct levels. The level measurement circuits are then automatically set to 'Lossy Peak Detect' mode for 15 symbol times, then 'Slow Peak Detect' until a received Frame Sync pattern is recognized, after which the automatic sequence ends and the level measurement circuit mode reverts to the mode set by the LEVRES bits of the Control Register (normally 'Level Track').

The peak detectors used in both 'Slow' and 'Lossy Peak Detect' modes include additional low pass filtering of the received signal. This greatly reduces the effect of pattern noise on the reference voltages held on the external DOC capacitors but means that pairs of '+3' (and '-3') symbols need to be received to establish the correct levels. Two pairs of '+3' and two pairs of '-3' symbols received after the start of an AQLEV sequence are sufficient to correctly set the levels on the DOC capacitors.

The automatic AQSC Symbol Clock acquisition sequence sets the PLL to 'Extra Wide Bandwidth' mode for 16 symbol times (this mode is not one of those which can be selected by the Control Register PLLBW bits) then changes to 'Wide' bandwidth. After 45 symbol times, the PLL mode will revert to that set by the Control Register PLLBW bits.

5.4 AC Coupling

For a practical circuit, ac coupling between the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem may be desired. There are, however, two issues which deserve consideration:

1. AC coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (9600bps) without FEC for reasonably random data with differing degrees of AC coupling:

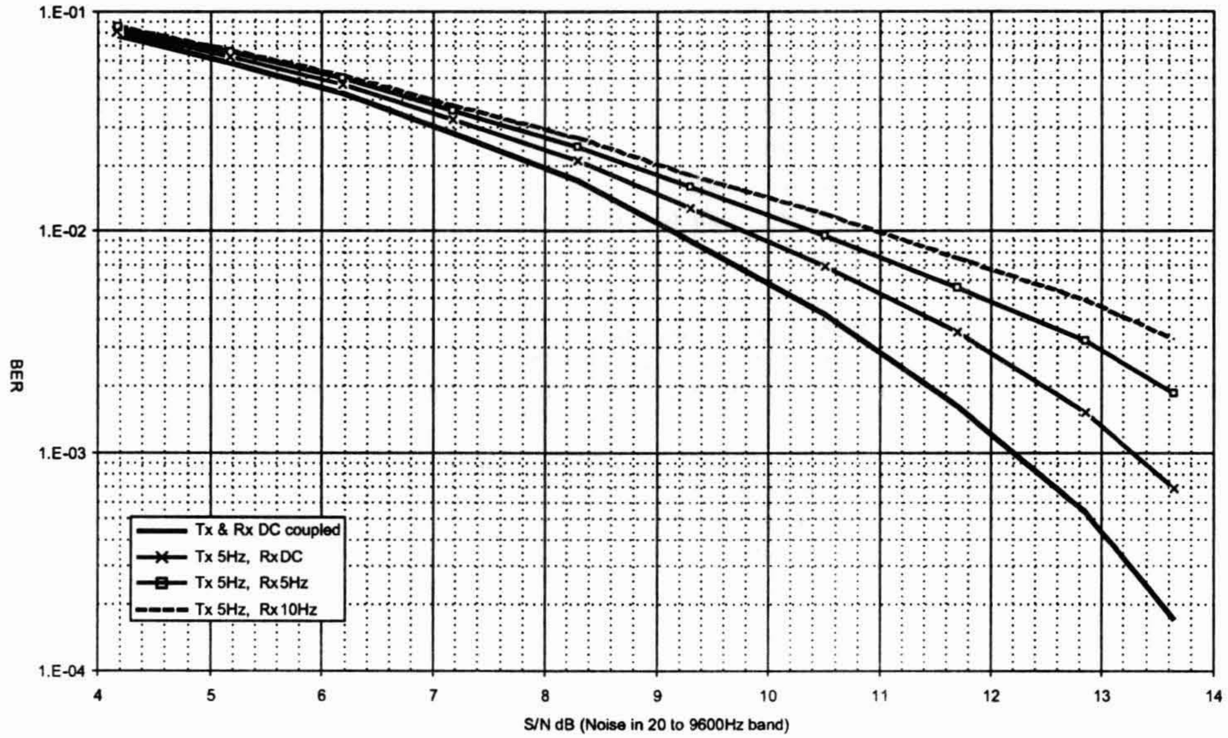


Figure 24: Effect of AC Coupling on BER (without FEC)

2. Any AC coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 25 below, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = \frac{1}{2\pi(\text{3dB cut-off frequency of the RC network})}$$

which is 32ms, or 153 symbol times at 4800 symbols/sec (9600bps) for a 5Hz network.

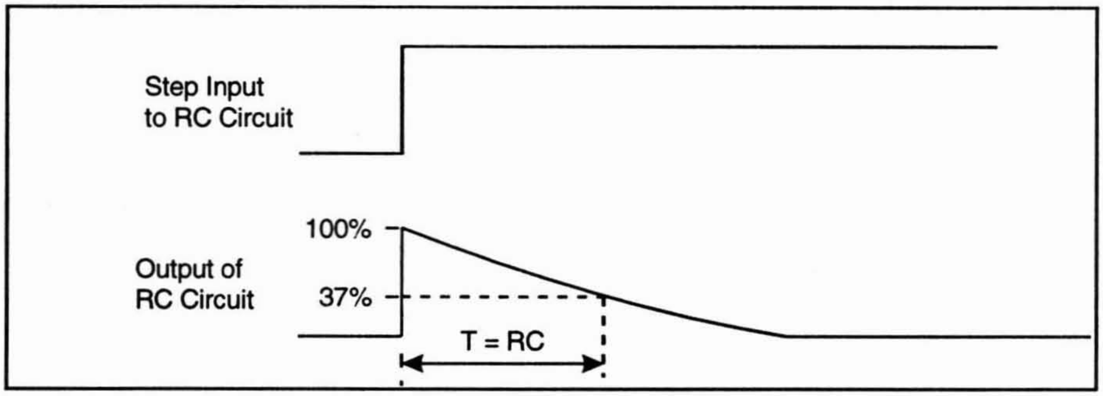


Figure 25: Decay Time - AC Coupling

In general, it is best to DC couple the receiver discriminator to the modem and ensure that any AC coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz for 4800 symbols/sec (9600bps).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracy.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec (9600bps) can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive ' +3 +3 -3 -3 ... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. However, this does place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency, and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec (9600bps) system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the equalized received signal eye diagram, using the Mode Register RXEYE function, provides a good indication of the overall RF transmitter/receiver performance.

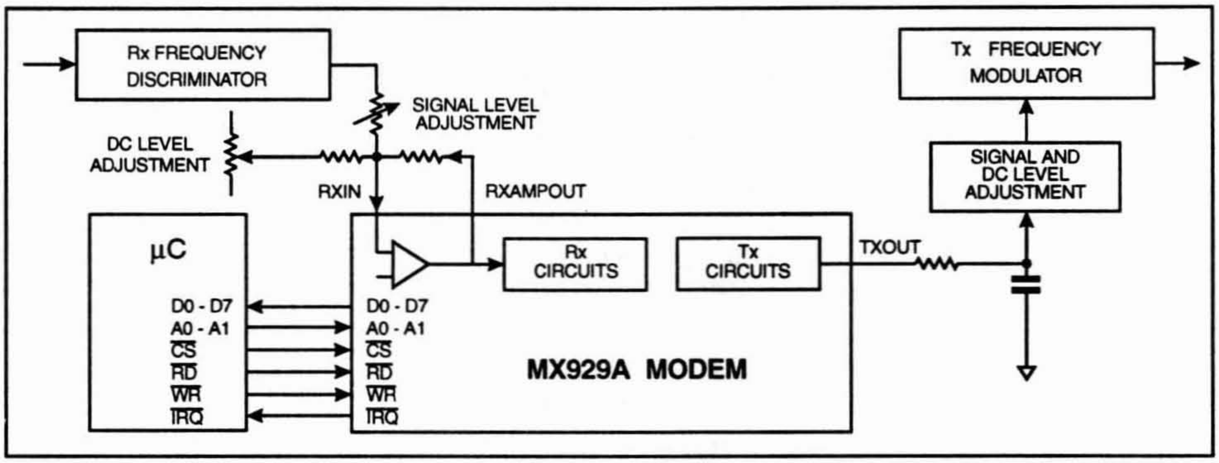

Rx FREQUENCY DISCRIMINATOR
SIGNAL LEVEL ADJUSTMENT
DC LEVEL ADJUSTMENT
RXIN
RXAMPOUT
µC
D0 - D7
A0 - A1
$\overline{CS}$
$\overline{RD}$
$\overline{WR}$
$\overline{IRQ}$
D0 - D7
A0 - A1
$\overline{CS}$
$\overline{RD}$
$\overline{WR}$
$\overline{IRQ}$
Rx CIRCUITS
Tx CIRCUITS
MX929A MODEM
TXOUT
Tx FREQUENCY MODULATOR
SIGNAL AND DC LEVEL ADJUSTMENT

Figure 26: Typical Connections between Radio and MX929B

5.6 Received Signal Quality Monitor

In applications where the modem has to monitor a long transmission containing a number of concatenated Frames, it is recommended that the controlling software include a function which regularly checks that the modem is still receiving a good data signal and triggers a re-acquisition and possibly changes to another channel if a problem is encountered. This strategy has been shown to improve the system's overall performance in situations where fading, large noise bursts, severe co-channel interference, or loss of the received signal for long periods are likely to occur.

Such a function can be simply implemented by regularly reading the Data Quality Register, which gives a measure of the overall quality of the received signal, as well as the current effectiveness of the modem's clock extraction and level measurement systems. Experience has shown that if two consecutive DQ readings are both less than 50 then it is worth instructing the MX929B to re-acquire the received signal levels and timing once it has been established that the received carrier level is satisfactory. Re-acquisition should follow the procedure given in Section 5.3 Clock Extraction and Level Measurement Systems.

The interval between Data Quality readings is not critical, but should be a minimum of 64 symbol times except for the first reading made after triggering the AQSC and AQLEV automatic acquisition sequences, which should be delayed for about 250 symbol times.

A suitable algorithm is shown in Figure 27.

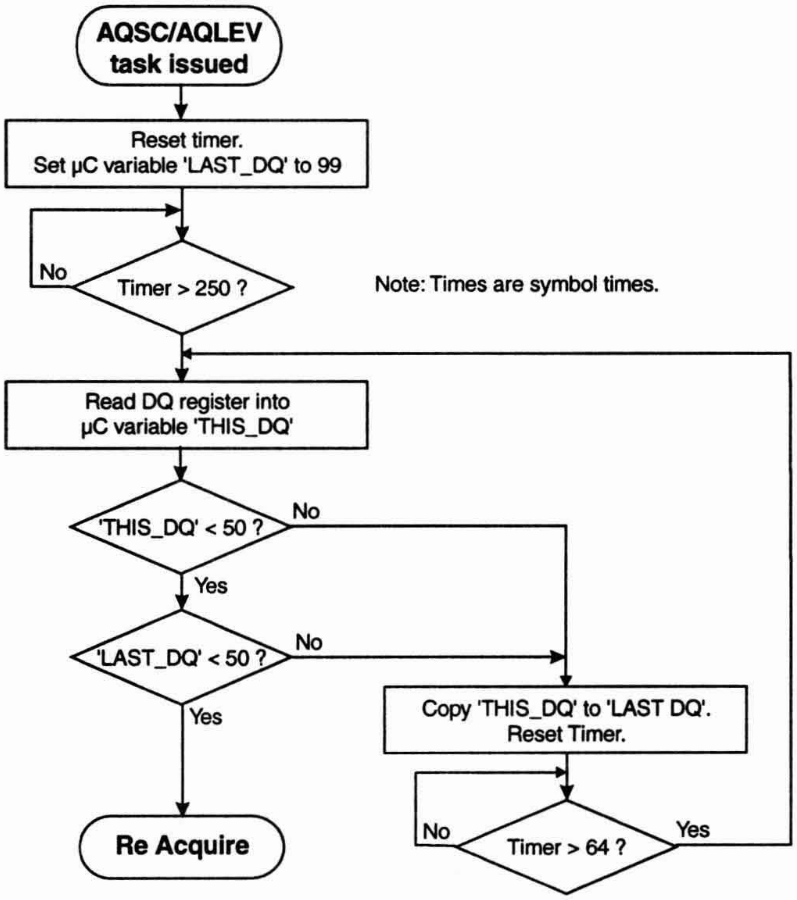

AQSC/AQLEV task issued
Reset timer. Set µC variable 'LAST_DQ' to 99
No
Timer > 250 ?
Note: Times are symbol times.
Read DQ register into µC variable 'THIS_DQ'
'THIS_DQ' < 50 ?
No
Yes
'LAST_DQ' < 50 ?
No
Yes
Copy 'THIS_DQ' to 'LAST DQ'. Reset Timer.
No
Timer > 64 ?
Yes
Re Acquire

Figure 27: Received Signal Quality Monitor Flowchart

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW and P Packages	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Symbol Rate		2400	9600	Symbols/sec
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz, Symbol Rate = 4800 symbols/sec (9600bps),
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 3.3V to 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC Parameters					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level					
TXIMP = 0	3	0.8	1.0	1.2	V_{P-P}
TXIMP = 1	3	0.88	1.1	1.32	V_{P-P}
Output DC Offset with respect to V_{DD} /2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset with respect to V_{DD} /2	5	-0.5		0.5	V
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Inverter Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	−5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10.0	µA

6.1.4 Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance.
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence. (Tx output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence, TXIMP = 0 or 1. The optimum level and DC offset values are proportional to V_{DD}.
6. Timing for an external input to the XTAL/Clock pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

6.1.5 Timing

µC Parallel Interface Timings (ref. Figure 28)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6.0			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90.0			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

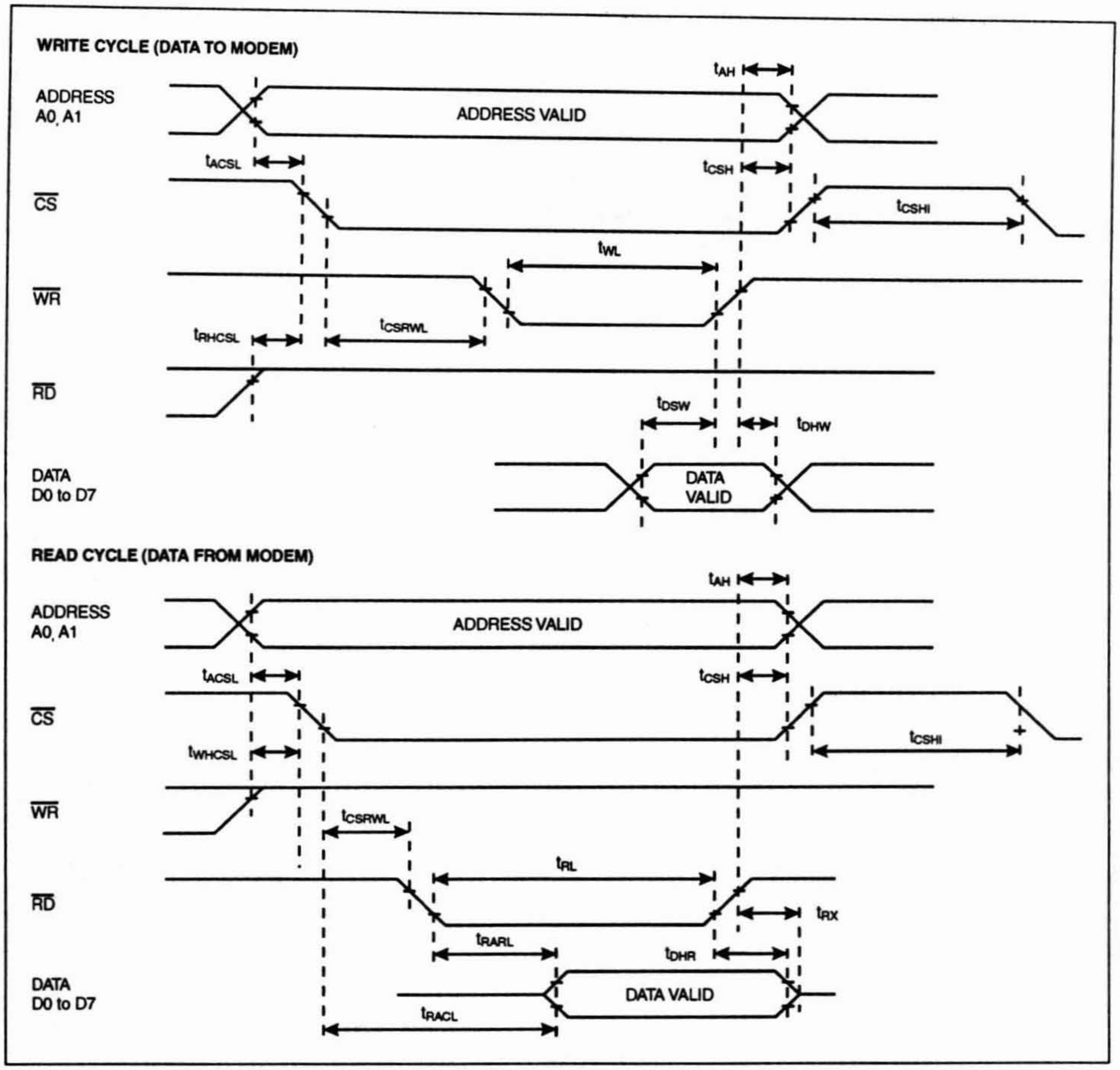

WRITE CYCLE (DATA TO MODEM)
t_{AH}
ADDRESS A0, A1
ADDRESS VALID
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{CSHI}
t_{WL}
$\overline{WR}$
t_{RHCSL}
t_{CSRWL}
$\overline{RD}$
t_{DSW}
t_{DHW}
DATA D0 to D7
DATA VALID
READ CYCLE (DATA FROM MODEM)
t_{AH}
ADDRESS A0, A1
ADDRESS VALID
t_{ACSL}
t_{CSH}
$\overline{CS}$
t_{WHCSL}
t_{CSHI}
$\overline{WR}$
t_{CSRWL}
t_{RL}
$\overline{RD}$
t_{RX}
t_{RARL}
t_{DHR}
DATA D0 to D7
DATA VALID
t_{RACL}

Figure 28: µC Parallel Interface Timings

6.1.6 Typical Bit Error Rate

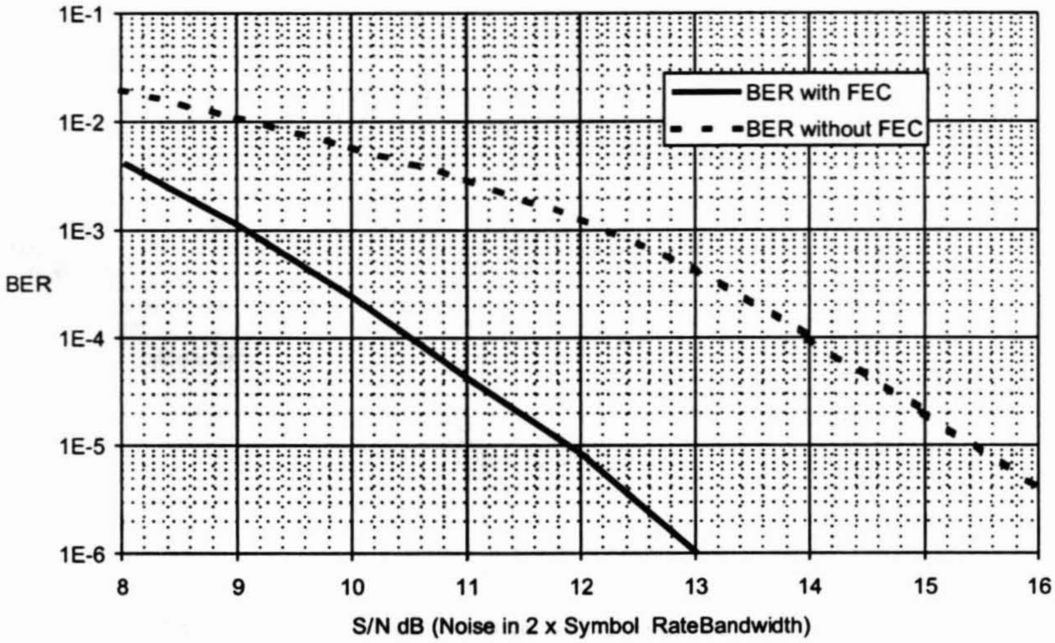


Figure 29: Typical Bit Error Rate With and Without FEC

Measured under nominal working conditions, LEVRES bits set to 'Level Track' or 'Slow Peak Detect' and PLLBW bits set to 'Medium' or 'Narrow' Bandwidth, Command Register TXIMP bit set to '0' or '1' (same for Tx and Rx devices), with pseudo-random data.

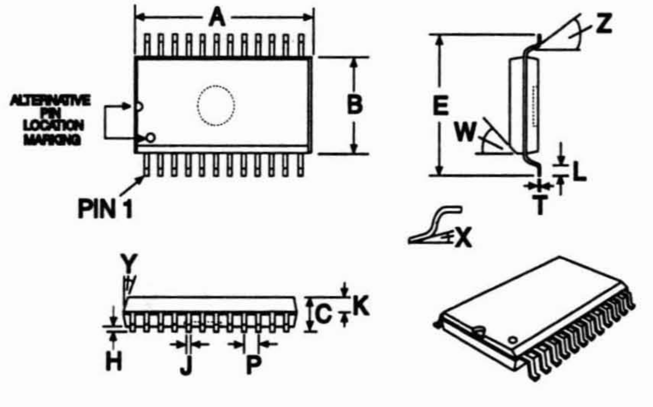
Note: S/N calculates as $20\log10\left(\frac{\text{Signal Voltage}}{\text{Noise Voltage}}\right)$

Where: Signal Voltage is the measured V_{RMS} of a random 4-level signal.

Noise Voltage is the V_{RMS} of a flat Gaussian noise signal having a bandwidth from a few Hz to twice the symbol rate (e.g. to 9600Hz when measuring a 4800 symbol/sec (9600bps) system).

Both signals are measured at the same point in the test circuit.

6.2 Packaging

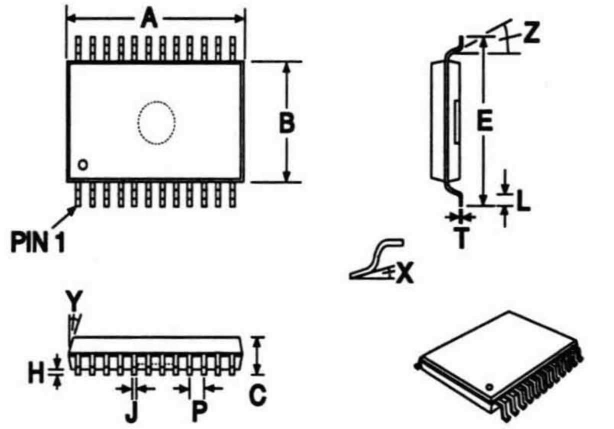


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 30: 24-pin SOIC Mechanical Outline: ***Order as part no. MX929BDW***

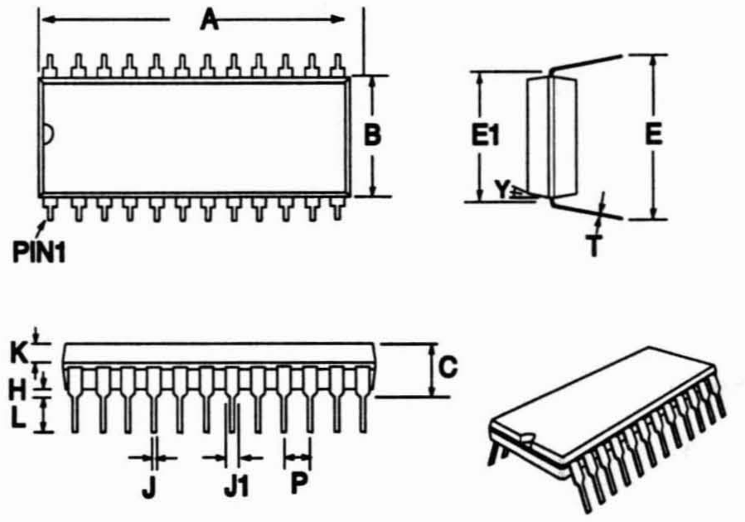


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 31: 24-pin SSOP Mechanical Outline: ***Order as part no. MX929BDS***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 32: 24-pin PDIP Mechanical Outline: ***Order as part no. MX929BP***

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX980 Digital Radio Baseband Processor for 8-PSK, π/4 DQPSK, PSK

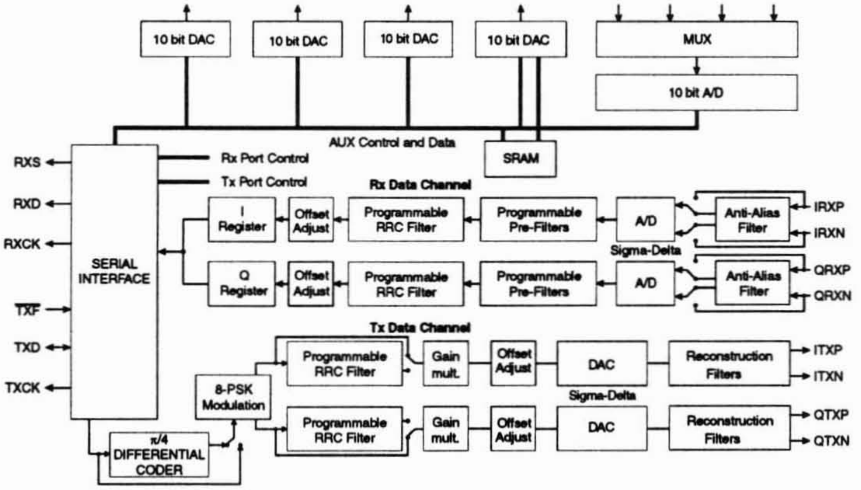
ADVANCE INFORMATION

Features

- **Tx and Rx 36kbps Baseband DSP Engine**
  - **PSK Modulation: π/4 DQPSK, 8PSK, BPSK, etc.**
  - **Root Raised Cosine (RRC) Filters**
  - **2 X 13 bit Sigma Delta D/A for quadrature Tx Signals**
  - **2 x 16 bit Sigma Delta A/D for quadrature Rx signals.**
- **Default TETRA Digital filter coefficients (can be user programmed)**
- **Low Power 3.0V - 5.5Volt Operation**
- **Integrated Analog I/O Processor for Radio Support**
  - **4 x 10-Bit D/A converters**
  - **4 Input x 10-Bit A/D converter**
  - **Integrated RF transmit power control with programmable ramp up/down attack profiles**
- **Full control, configuration, and digital signal flow via Serial Interface**

Applications

- **Digital Radio for Voice and Data**
- **Low Bandwidth,**
- **High Spectral Efficiency**


10 bit DAC
10 bit DAC
10 bit DAC
10 bit DAC
MUX
10 bit A/D
AUX Control and Data
SRAM
RXS
RXD
RXCK
TXF
TXD
TXCK
SERIAL INTERFACE
Rx Port Control
Tx Port Control
Rx Data Channel
I Register
Offset Adjust
Programmable RRC Filter
Programmable Pre-Filters
A/D
Anti-Alias Filter
IRXP
IRXN
Sigma-Delta
Q Register
Offset Adjust
Programmable RRC Filter
Programmable Pre-Filters
A/D
Anti-Alias Filter
QRXP
QRXN
Tx Data Channel
Programmable RRC Filter
Gain mult.
Offset Adjust
DAC
Reconstruction Filters
ITXP
ITXN
8-PSK Modulation
Sigma-Delta
Programmable RRC Filter
Gain mult.
Offset Adjust
DAC
Reconstruction Filters
QTXP
QTXN
π/4 DIFFERENTIAL CODER

This device is intended to act as an interface between the analog and digital sections of a Digital Radio System, and perform many critical and DSP-intensive functions. The chip is designed with the necessary capability to meet the requirements for use in both mobile and base station applications in Terrestrial Trunked Radio (TETRA) systems.

The transmit path comprises all the circuitry required to convert digital data into suitably filtered analog I and Q signals for subsequent up-conversion and transmission. This includes digital control of the Tx signal gain, offset, and programmable digital filters: default coefficients provide the RRC response required for TETRA.

The receive section accepts differential analog baseband I and Q signals and converts these into a suitably filtered digital form for external processing and data extraction. Offset correction and the digital filters are fully programmable with default coefficients providing the RRC response required for TETRA.

Auxiliary DAC and ADC functions are included for the control and measurement of the RF section of the radio system. This may include AFC, AGC, RSSI, or part of the control system for a Cartesian Loop.

The MX980 requires a 3.0V to 5.5V power supply and is available in the following packages: 44-pin PLCC (MX980L6) and 44-pin QFP (MX980L7).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

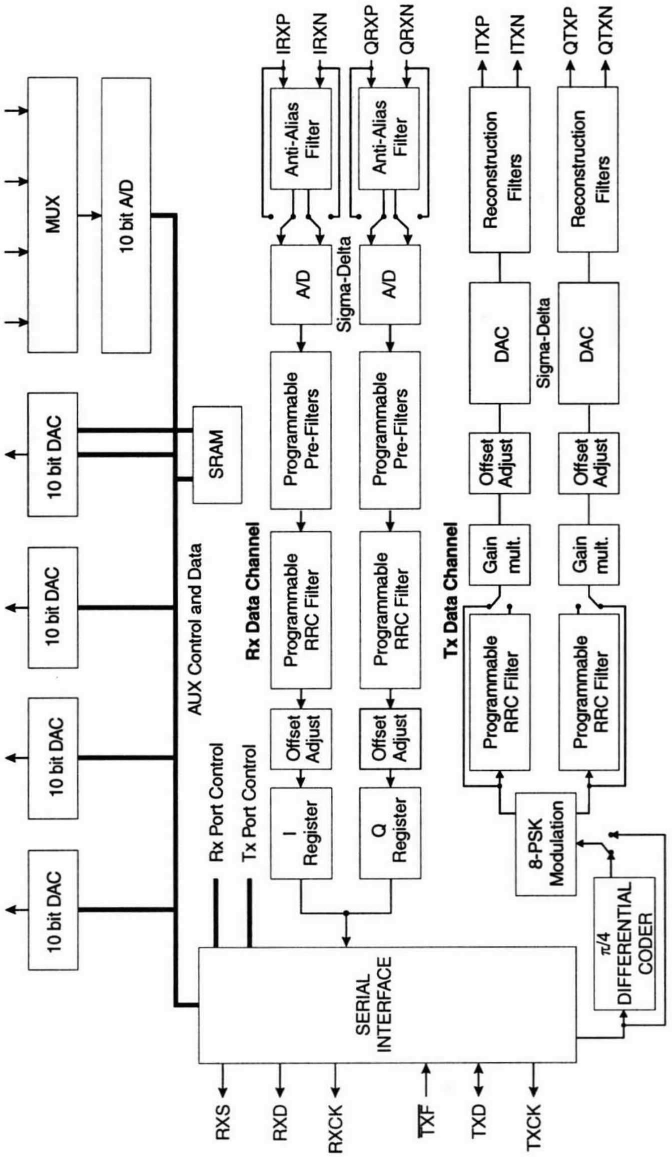

MUX
10 bit A/D
10 bit DAC
10 bit DAC
10 bit DAC
10 bit DAC
SRAM
AUX Control and Data
Rx Port Control
Tx Port Control
Rx Data Channel
IRXP
IRXN
QRXP
QRXN
Anti-Alias Filter
Anti-Alias Filter
A/D
A/D
Sigma-Delta
Programmable Pre-Filters
Programmable Pre-Filters
Programmable RRC Filter
Programmable RRC Filter
Offset Adjust
Offset Adjust
I Register
Q Register
Tx Data Channel
ITXP
ITXN
QTXP
QTXN
Reconstruction Filters
Reconstruction Filters
DAC
DAC
Sigma-Delta
Offset Adjust
Offset Adjust
Gain mult.
Gain mult.
Programmable RRC Filter
Programmable RRC Filter
8-PSK Modulation
π/4 DIFFERENTIAL CODER
SERIAL INTERFACE
RXS
RXD
RXCK
TXF
TXD
TXCK

Figure 1: Block Diagram

2 Signal List

LH Package	Signal		Description
Pin No.	Name	Type	
15	MCLK	input	Master clock input (typically 9.216MHz)
16	SClk	output	Serial interface clock
17	CmdDat		Command serial interface Data
18	CmdFS	input	Command serial interface Frame
19	CmdRdDat	output	Command serial interface Read Data
20	CmdRdFS	output	Command serial interface Read Frame
11	RxDat	output	Receive serial interface Data
12	RxFS	output	Receive serial interface Strobe
23	$\overline{\text{IRQ}}$	output	Interrupt request
14	$\overline{\text{RESET}}$	input	Chip Reset
24	SCANSEL	input	Scan Select (normally tied low)
25	ITXP	output	Transmit "I" channel, positive output
26	ITXN	output	Transmit "I" channel, negative output
30	QTXP	output	Transmit "Q" channel, positive output
29	QTXN	output	Transmit "Q" channel, negative output
42	IRXP	input	Receive "I" channel, positive input
41	IRXN	input	Receive "I" channel, negative input
38	QRXP	input	Receive "Q" channel, positive input
37	QRXN	input	Receive "Q" channel, negative input
43	AUXADC1	input	Auxiliary ADC channel 1
44	AUXADC2	input	Auxiliary ADC channel 2
1	AUXADC3	input	Auxiliary ADC channel 3
2	AUXADC4	input	Auxiliary ADC channel 4
10	AUXDAC1	output	Auxiliary DAC channel 1
9	AUXDAC2	output	Auxiliary DAC channel 2
8	AUXDAC3	output	Auxiliary DAC channel 3
7	AUXDAC4	output	Auxiliary DAC channel 4
36	BIAS1	BI	Analog bias level. This pin should be decoupled to V_{SSB}.
35	BIAS2	BI	Analog bias level. This pin should be decoupled to V_{SSB}.
32	V_{CC1}	Power	I Channel analog positive supply rail. This pin should be decoupled to V_{SS1}.
33	V_{CC2}	Power	Q Channel analog positive supply rail. This pin should be decoupled to V_{SS2}.
34	V_{CC3}	Power	Analog Bias positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SSB}.
6	V_{DD1}	Power	Auxiliary analog positive supply rail. This pin should be decoupled to V_{SSA}.
3,21	V_{DD}	Power	Digital positive supply rail. This pin should be decoupled to V_{SS}.
27,40	V_{SS1}	Ground	I Channel analog negative supply rail.
28,39	V_{SS2}	Ground	Q Channel analog negative supply rail.
31	V_{SSB}	Ground	Analog Bias negative supply rail.
5	V_{SSA}	Ground	Auxiliary analog negative supply rail.
4,13,22	V_{SS}	Ground	Primary digital negative supply rail.

Table 1: Signal List

3 External Components

3.1 Rx Inputs

When using the internal anti-alias filter, the following circuit is suggested:

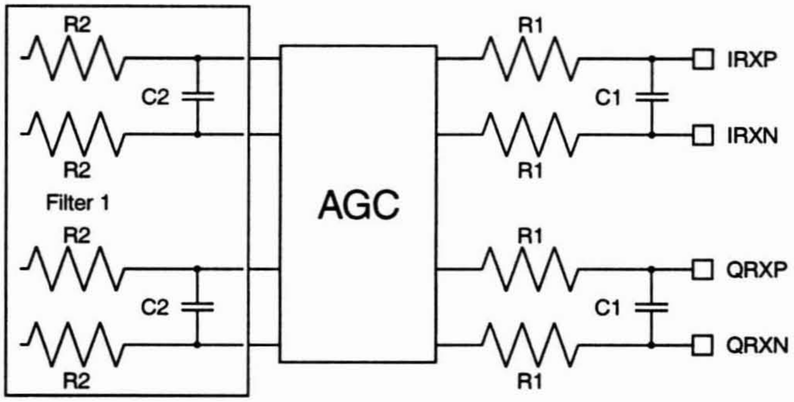

R2
C2
R2
Filter 1
R2
C2
R2
AGC
R1
C1
R1
R1
C1
R1
IRXP
IRXN
QRXP
QRXN

Figure 2: Recommended External Components - Rx Inputs

Example values:

R1	220Ω		C1	1500pF	(R1, C1 precise values are not critical) (-3dB at 240kHz)
R2	408Ω		C2	3900pF	(R2 x C2 time constant should be preserved) (-3dB at 50kHz)

When not using the internal anti alias filter, it is suggested that the user should follow the guidelines in Section 4.3.1. In both cases, there should be at least one filter pole close to the chip inputs.

3.2 Tx Outputs

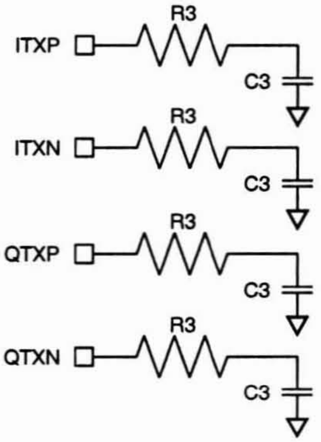

ITXP
R3
C3
ITXN
R3
C3
QTXP
R3
C3
QTXN
R3
C3

Figure 3: Recommended External Components - Tx Outputs

Example values:

Component	Value		Component	Value
R3	220Ω		C3	1000pF

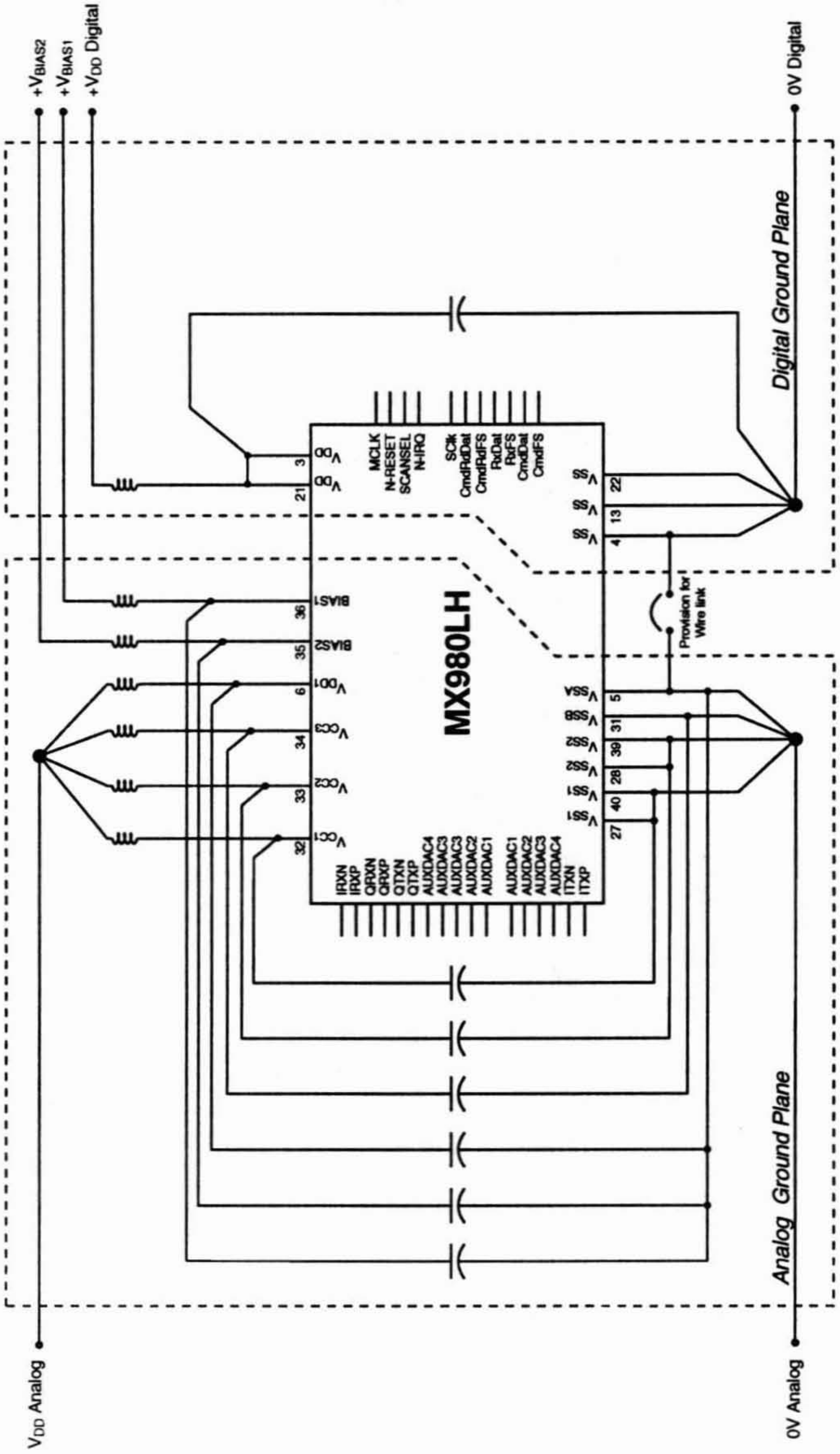
Decoupling capacitors should be employed as detailed in Section 4.1.

4 General Description

4.1 Connection and Decoupling of Power Supplies

Optimum performance from the MX980 can only be obtained by the use of adequate decoupling and the separation of analog and digital signals, including the use of separate ground planes.

Printed circuit board layout should follow the recommendations shown in Figure 4.


+V$_{BIAS2}$
+V$_{BIAS1}$
+V$_{DD}$ Digital
0V Digital
Digital Ground Plane
MX980LH
V$_{DD}$
V$_{DD}$
MCLK
N-RESET
SCANSEL
N-IRQ
SClk
CmdRdDat
CmdRdFS
RxDat
RxFS
CmdDat
CmdFS
V$_{SS}$
V$_{SS}$
V$_{SS}$
BIAS1
BIAS2
V$_{DD1}$
V$_{CC3}$
V$_{CC2}$
V$_{CC1}$
V$_{SSA}$
V$_{SSB}$
V$_{SS2}$
V$_{SS2}$
V$_{SS1}$
V$_{SS1}$
IRXN
IRXP
QRXN
QRXP
QTXN
QTXP
AUXDAC4
AUXDAC3
AUXDAC2
AUXDAC1
AUXADC1
AUXADC2
AUXADC3
AUXADC4
ITXN
ITXP
3
21
22
13
4
36
35
6
34
33
32
5
31
39
28
40
27
Provision for Wire link
Analog Ground Plane
V$_{DD}$ Analog
0V Analog

All capacitors are 0.01µF, all inductors are 0.1µH.

Figure 4: Recommended Decoupling Components

4.2 Tx Data Path

The features described below give a high degree of flexibility for the user to adjust the baseband processing to compensate for non-ideal performance in the IF, RF and RF linear amplifier sections.

4.2.1 Modulator

This takes the 2-bit symbols, performs a Gray code conversion and uses a recursive adder to generate a 3-bit code representing the 8 possible phase states. A look up table provides the digitally encoded I and Q values for each phase state. The modulator function can be by-passed if required; in this case the 3-bit code representing the 8 possible phase states are passed to the look up table directly via the serial interface.

4.2.2 Filters

Digital filtering is applied to the modulator output data; the coefficients are set as default to give a Root Raised Cosine response with roll-off factor of 0.35. These FIR filters operate at 8x the incoming symbol rate and are configured, for each channel, as two filters in cascade: the first filter has 79 taps and the second filter has 49 taps. The first filter is used to enhance stop-band rejection and act as a sampling correction filter and the second filter provides the primary shaping. Coefficients for the filters may also be downloaded to the device via the serial interface. This provides the opportunity, if required, to fine tune the frequency response of a complete system to minimize BER or to use the device in other applications. The filters can also be bypassed if required.

4.2.3 Gain Multiplier

This circuitry allows independent external control of the digital amplitudes in the I and Q channels to 12 bits of resolution. Extra circuits allow a mode of operation which will enable linear ramping up to a maximum value, stay at this value for a specified duration, then ramp back down to zero. The maximum value for each channel, the duration at maximum, the ramping up rate and the ramping down rate are all programmable via the serial interface.

4.2.4 Ramping Output Amplitude

A facility is provided to allow linear ramping of the outputs. This is accomplished, if enabled, by multiplying the gain multiplier words by the ramping control register (RCR) value. The RCR is a 12-bit word, representing a value from 0 to 1, which is designed to increment by an amount (INC) until its maximum value. This value is held until a number of symbol times from the start of transmission (TRD) when RCR decrements by an amount (DEC) until zero. INC, DEC and TRD are all 12-bit words input via the serial interface prior to the start of a transmission.

4.2.5 Offset Adjust

Offset registers allow any offsets introduced in the analog sections of the transmit path to be corrected digitally via the serial interface. The offset adjust has a resolution of 1 LSB and a maximum value of 0.25x full scale.

4.2.6 Phase Pre-distortion

A further feature allows the user to compensate for a non-orthogonal carrier phase in the external quadrature modulator by adding a programmable fraction of up to 1/8 of the filtered I and Q channel signals to each other immediately prior to the DAC input.

4.2.7 Sigma-Delta D-A Converters and Reconstruction Filters

The converters are designed to have low distortion and >80dB dynamic range. These 3rd order converters operate at a frequency of 128x symbol rate so as to over-sample the data at their inputs a further 16 times. The reconstruction filters are 5th order, switched capacitor, low pass filters designed to work in conjunction with an external RC.

4.3 Rx Data Path

4.3.1 Anti-Alias Filtering and Sigma-Delta A-D Converters

The sampling frequency of the Sigma-Delta A-D is 128x symbol rate. The high oversampling rate relaxes the design requirements on the anti-alias filter. However, to achieve optimum performance the anti-alias filter must reject the sampling frequency to about -110dB, of which at least 40dB must be provided externally. Additionally, in order to ease the complexity of the subsequent digital filters, there is a further requirement that the anti-alias filter suppress 8x symbol rate to about -30dB. The on-chip anti-alias filter is designed to achieve this when used in conjunction with some external filtering. If required, the on-chip anti-alias filter can be by-passed and powered down, although external anti-aliasing must then be provided. The 4th order Sigma-Delta

A-D converters are designed to have low distortion and >96dB dynamic range. The baseband I and Q channels must be provided as differential signals; this minimizes in-band pick up both on and off the chip.

4.3.2 Filters

Digital filtering is applied to the data from the Sigma-Delta A-D converters; the default coefficients are set to give a Root Raised Cosine response with roll-off factor of 0.35. These FIR filters are configured, for each channel, as three filters in cascade. The first filter gives sufficient rejection at 8x symbol rate to permit decimation at that frequency (note that -30dB is provided by the primary anti-alias filters). The second filter has 63 taps and is used to enhance stop-band rejection. The third filter has 49 taps and provides the primary shaping requirements. Coefficients for the second and third filters are programmable via the serial interface. This gives the opportunity, if required, to fine tune the frequency response of a complete system to minimize the BER or use the device in other applications. The filters can also be bypassed if required by setting the center coefficient to maximum and all other coefficients to zero.

4.3.3 Offset Registers

System generated offsets may be removed by control of the offset register via the serial interface.

4.3.4 I and Q Channel Gain

Programmable gain modules are provided in both I and Q channels. These blocks allow the user to adjust the dynamic range of the received data within the digital filters, thus optimizing the filter signal to noise performance for a range of levels at the Rx input pins.

The two channels are independently programmable. This enables differential gain corrections to be made within the digital domain.

4.4 Auxiliary Circuits

4.4.1 10-Bit DACs

Four 10-bit DACs are provided to assist in a variety of control functions. The DACs are designed to provide an output as a proportion of the supply voltage, depending on the digital input. They are monotonic with an absolute accuracy of better than 1%. Control and Data for these come via the serial interface.

4.4.2 10-Bit ADC

A 10-bit ADC is provided to assist in a variety of measurement and control functions. The ADC is designed to produce a digital output proportional to the input voltage; full scale being the positive supply. It is monotonic with an absolute accuracy of about 1%. An input multiplexer allows the input to be selected from one of four sources. Control and digital data output is via the serial interface.

4.4.3 Power Ramping and Control

One of the DACs has an additional feature that enables a set of values to be sequenced out at a pre-selected frequency. This is aimed at enabling power ramping of an RF output with a suitable profile. The sequence may be reversed for power down. The sequence of values is stored in a dedicated RAM, that can be loaded via the serial interface.

4.5 IRQ Function

An interrupt request (IRQ) pin is provided for asynchronous communication with an external processor. The IRQ (asserted low) will be asserted when any of the error or user information flags are activated by an internal operation. Some examples of operations that may generate an IRQ are:

- An attempt by the user to write to a full Tx data-input FIFO.
- An attempt is made by the Tx to read from the Tx data-input FIFO when it is empty.
- An internal arithmetic overflow has occurred in an FIR filter.

The IRQ feature may also be used to establish the phasing of the received I and Q channel data from the RxDat serial port should synchronization be lost for any reason.

The cause of the IRQ can be obtained by reading the error flags register. All possible causes of an IRQ are masked on reset. Mask status can be altered by writing to the IRQ mask register.

Note: Default coefficients and settings have been optimized to maximize performance and should not cause arithmetic overflows. However, use of non-default coefficients, large offset corrections or large Tx phase adjustments may cause problems that can be corrected by scaling down coefficients or via the gain multiplier feature.

4.6 Serial Interface

All digital data I/O and control functions for the MX980 are via the serial interface. It is expected that the MX980 will be used in conjunction with a DSP and/or other processor. The device has three serial interface ports and each is based on the industrial standard three wire serial interface. This interface allows communication with standard DSP ICs using a minimum of external components. The three serial interface ports are:

Cmd	Command port. Generally this is an input port receiving commands and data from the host, but may also be configured as a bi-directional I/O interface.
CmdRd	Command read port, an output port to send command read data back to the host. Read data is only sent on this port in response to a read command
RxData	Receive data port, an output port to send receive data back to the host. Data is only present on this interface when the Rx Data path is active. This port may also be configured as the *CmdRd* port.

The three interfaces consist of the following signal pins:

SClk	Output	*Serial Clock* pin. This pin is common for all three interfaces.
CmdDat	In/Out	Command port *Data* pin. This pin is, by default, an input, but it may be configured as an open drain bi-directional pin.
CmdFS	Input	Command port *Frame Sync* pin. This pin is used to mark the first bit in a serial frame.
CmdRdDat	Output	Command read port *Data* pin. This pin only has active data on it in response to a read command.
CmdRdFS	Output	Command read port *Frame Sync* pin. This pin is used to mark the first bit in a serial frame.
RxDat	Output	Receive data port *Data* pin. This pin is only active when the Rx Data path is active.
RxFS	Output	Receive data port *Frame Sync* pin. This pin is used to mark the first bit in a serial frame.

Note: All *Frame Sync* strobe signals are actually coincident with the last bit of a dataframe. See Figure 5 and Figure 6 for further details. Functions performed by the serial interface include:

1. Power up or down and optional bypassing of selected blocks.
2. Setting digital filter coefficients.
3. Loading ramp up and ramp down increments for Tx.
4. Loading and transmitting data.
5. Loading offset correction, gain multiplier and phase adjustment registers.
6. Enabling/disabling of output via the Rx serial interface.
7. Vary sampling time for Rx data relative to the symbol (144kHz) clock.
8. Loading data into auxiliary DACs.
9. Initiating conversions using auxiliary ADCs and reading results.
10. Writing data to and reading data from the Waveform Generation SRAM.
11. Power Ramping time step control.

4.6.1 Command Interface

A serial command word consists of a 16-bit frame. Each frame is marked by an active *Frame Sync* event that precedes the MSB bit. A command word can be either a Control word or a Transmit Data word.

MSB				LSB
R/$\overline{W}$	Address		Data	
15	14	8	7	0

Table 2: Command Control Serial Word

MSB				LSB
1	Tx Data Address	U/D	4/1	Tx Data
15	14 10	9	8	7 0

Table 3: Command Transmit Data Word

4.6.2 Command Read Interface

Command read data is either output on one of the serial read ports, or driven out in the last 8 bits (data field) on the *Cmd* port. When command read data is output on a serial read port, the read address is put in the most significant half of the word, and the read data in the least significant half.

MSB		LSB
0	Read Address	Data
15	14 8	7 0

Table 4: Command Read Serial Word

4.6.3 Rx Data Interface

The Rx Data interface is used only for output of the I and Q received data, unless it is operating in the mode where *CmdRd* data is directed to it. When data reception is enabled, I and Q received data will be output at either 8x or 4x the symbol rate, under control of command register **RxSetup2**. See Section 4.7.1.7. This is achieved by reducing the serial interface clock rate from MCLK/2 to MCLK/4 and discarding alternate data samples under control of command registers **ConfigCtrl1** and **RxSetup2**. 16-bit I and Q data words are output at the Rx Data interface, I data and MSB first (by default), on the rising edge of SClk.

4.6.4 Transmission of Data

The address of the Tx FIFO is given consecutive locations ($0x04-$0x07), which allows the address bits A1 and A0 (bits 11 and 10) of the Command Transmit Data Serial Word to be utilized as transmit control functions. Data to be transmitted can be in either one or four (2-bit) symbol blocks, which are subsequently modulated into the DQPSK constellation, or in 3-bit words, which map directly into constellation points according to the table shown below.

3 bit code	000	001	010	011	100	101	110	111
I	1	0.7071	0	-0.7071	-1	-0.7071	0	0.7071
Q	0	0.7071	1	0.7071	0	-0.7071	-1	-0.7071

Table 5: Constellation Map

The user initiates a transmit frame by asserting the *TxEn* bit in the **TxSetup** register. However, internal transmission of the data will wait until specific conditions have been met. Firstly, a valid data word must be written into the FIFO with the *TxRampEn* bit of the **TxSetup** register asserted. Secondly, the internal symbol clock must be active. Therefore, there is a variable delay between asserting the *TxEn* bit and transmission starting. The user may poll the *TxPathEn* bit of the **TxFIFOStatus** register to establish when transmission has started, and in this case the active state of *TxPathEn* is High. In general, the user will wish to know when the transmit frame has completed. This is indicated by *TxPathEn* returning to a Low state.

To relieve the user of polling overheads when waiting for Tx frame completion, an interrupt can be set up to occur on the transition of the *TxPathEn* bit from High to Low. In such circumstances, the interrupt activation state of the *TxPathEn* can be considered Low.

Two control bits are associated with each data transmission word. One controls the format of the word and the other initiates and terminates a transmission cycle. This close association enables precise control of the transmission frame. To relieve the user of the need to synchronize each **TxData** write with the internal transmit cycle, transmit data words are written into an internal 4-word-deep FIFO. Symbols or constellation points are then read as needed from this FIFO. It is necessary to make sure that there is always a word to be read, and also that the FIFO is never written to when full. This may be accomplished by using one of two data interlock mechanisms.

4.6.4.1 Data Interlock Mechanisms

There are two possible transmission data interlock mechanisms. It is recommended that the user should always use one of these methods.

1. Software polling: *Software polling* requires the user to first check that the FIFO is not full before writing each **TxData** word. This may be accomplished by inspecting the relevant FIFO status bits before writing one or more **TxData** words.
2. Serial Clock when ready: The *Serial Clock when ready* method is a hardware interlock mechanism (enabled by setting the *TxHandshakeEn* bit of **ConfigCtrl1** register active). The mechanism allows the user to write **TxData** words without doing any FIFO checks: the hardware handshake is implemented by stopping the serial port clock when the FIFO is full. To prevent a serial port lockout-condition, the handshake is only enabled once the transmission frame has been initiated and is automatically disabled at the end of a frame. This mechanism should be used with care, because stopping the clock will freeze all other serial port transfers (the serial port clock SClk is common to all three serial ports), including access to auxiliary data converters and receive data.

4.6.4.2 Power Ramping and Frame Interlock

The *RampUp* bit in the **TxData** word is used to control both the power ramping function and the frame activation. To start a transmission frame, a transmission word is written with the *RampUp* bit active. All subsequent **TxData** words prior to frame termination must also have this bit active. The frame is terminated by writing transmit data words with the *RampUp* bit inactive. Subsequent **TxData** words must also have this bit inactive, until initiation of a new frame is required. While the power ramping is active (up or down) the user must supply transmission symbols or valid constellation points. Once the ramp down operation has completed, all subsequent **TxData** writes with the *RampUp* bit inactive will be ignored.

4.6.5 Command Control Serial Word

A command word either directly accesses an internal register for a read or write operation, or addresses a memory access point to indirectly access a block of internal memory. For test purposes all registers that can be written may also be read. Not all registers may be written, as some are just status registers. Each register or memory access point is assigned a unique address: the whole (8-bit) address range is reserved for the MX980.

4.6.5.1 Indirect Memory Addressing

All internal memory access is via an access point. First, a command word access is used to reset the internal address pointer, then data port access operations post-increment this address pointer.

Example: To program the fifth and sixth locations of the Auxiliary SRAM with $0x01AA the commands would be:

$0x0000⇒Cmd	;	set **ConfigCtrl1** all bits Low	;	use default conditions
$0x0118⇒Cmd	;	set **ConfigCtrl2** bits 7 and 6 Low	;	required by default for these Reserved bits
	;	set **ConfigCtrl2** bit 4 High	;	post-increment addresses on a read operation
	;	set **ConfigCtrl2** bit 3 High	;	enable read/write access to the Auxiliary SRAM
$0xF300⇒Cmd	;	read **SramData** LSB register	;	read fourth memory location (LSB). Post-increment pointer.
CmdRd⇒$0xF3xx	;	**SramData** LSB register data returned	;	discard this byte
$0x7002⇒Cmd	;	write **SramData** LSB register	;	write $0x02 to fifth memory location (LSB)
$0x716A⇒Cmd	;	write **SramData** MSB register	;	write $0x6A to sixth memory location (MSB)
$0xF000⇒Cmd	;	read **SramData** LSB register	;	read fifth memory location (LSB)
CmdRd⇒$0xF002	;	**SramData** LSB register data returned	;	check this byte is $0x02
$0xF100⇒Cmd	;	read **SramData** MSB register	;	read sixth memory location (MSB)
CmdRd⇒$0xF16A	;	**SramData** MSB register data returned	;	check this byte is $0x6A
$0x0110⇒Cmd	;	set **ConfigCtrl2** bit 3 Low	;	disable read/write access to the Auxiliary SRAM

4.6.6 Coefficient Memory

The convention for naming filter coefficients is A1 to An, where n is given by (Filter Length + 1)/2, i.e. for the 15-tap filter, n = 8. This arises from the internal architecture of the filters and the fact that they are all "odd" and symmetrical. Write or read operations beyond this coefficient number will be reflected about the central coefficient e.g. the tenth read operation from the 15-tap filter would access coefficient location A6.

There is no practical reason to write or read beyond location n, but the user in any case must avoid write operations at the (Filter Length + 1) location. This location (A0) location must be zero for the filters to operate correctly. The global reset (N-RESET pin) establishes this condition when taken Low.

4.7 Register Description

This section describes in detail each of the registers and access points addressed by the Command Control Serial Word.

Key to Register Map

The following sections describe in detail the operation and use of each of the registers in the device. The registers are split into their functional groups, grouping associated registers together. Each section consists of a Title, an Address, a Function Reference Field, a Description, and a Bit Specification.

The Function Reference Field describes the overall access available to this section (RW/W/R, where R = Read and W = Write).

The Bit Specification describes the function of each individual bit, or a range of bits within a register. There is a separate line for each distinct field of bits. The State column indicates the action available to each group of bits (RW/W/R).

Register Reset State

All I/O access points (both read and write) are reset to logic zero on taking $\overline{\text{RESET}}$ Low, except where explicitly shown in this document. The reset state of status bits will depend on the level of the status signal being monitored. Other registers (both read and write) are not affected by taking $\overline{\text{RESET}}$ Low.

4.7.1 Register and Access Point Summary

Control and Status Registers		
$0x00	**ConfigCtrl1**	Configuration control register 1
$0x01	**ConfigCtrl2**	Configuration control register 2
$0x02	**PowerDownCtrl**	Power control register
$0x03	**TxSetup**	Transmit set-up register
$0x04-$0x07	**TxData**	Transmit data registers
$0x08	**RxSetup1**	Receive set-up control register 1
$0x09	**RxSetup2**	Receive set-up control register 2
$0x0A	**AnaCtrl**	Analog configuration control register
$0x0B	**AuxAdcCtrl**	Auxiliary ADC data converter control register
$0x0C	**RamDacCtrl**	Ram Dac control register
$0x0D	**LoopBackCtrl**	Loopback control register
$0x0E	**TxErrorStatus**	Transmit error status register
$0x0F	**TxErrStatMask**	Transmit error status interrupt mask register
Auxiliary Function Registers		
$0x10-$0x17	**AuxAdcData**	Auxiliary ADC data registers
$0x18-$0x1F	**AuxDacData**	Auxiliary DAC data registers
Status and Interrupt Registers		
$0x20	**RxErrorStatus**	Receive error status register
$0x21	**RxErrorStatMask**	Receive error status interrupt mask register
$0x22	**TxFIFOStatus**	Transmission data FIFO status register
$0x23	**TxFIFOStatMask**	Tx data FIFO status interrupt mask register

Memory I/O Access Points		
$0x24-$0x2D	**CoeffRamData**	Coefficient memory I/O access addresses
$0x2E-$0x2F		Not Used.
Rx Data Path Registers		
$0x30-$0x31	**RxIQGainMult**	Receive I channel gain attenuation registers
$0x32-$0x33	**RxIQOffset**	Receive I channel offset correction registers
$0x34-$0x35	**RxIQGainMult**	Receive Q channel gain attenuation registers
$0x36-$0x37	**RxIQOffset**	Receive Q channel offset correction registers
Rx Data Path Access Points		
$0x38-$0x39	**RxDataAccess**	Receive path data access point (I)
$0x3A-$0x3B	**RxDataAccess**	Receive path data access point (Q)
$0x3C-$0x3F		Not Used
Tx Data Path Registers		
$0x40-$0x41	**TxPhase**	Transmit I channel phase correction registers
$0x42-$0x43	**TxIQGainMult**	Transmit I channel gain attenuation registers
$0x44-$0x45	**TxIQOffset**	Transmit I channel offset correction registers
$0x46-$0x47	**TxPhase**	Transmit Q channel phase correction registers
$0x48-$0x49	**TxIQGainMult**	Transmit Q channel gain attenuation registers
$0x4A-$0x4B	**TxIQOffset**	Transmit Q channel offset correction registers
$0x4C-$0x4D	**TxRampUpInc**	Transmit ramp-up increment registers
$0x4E-$0x4F	**TxRampDnDec**	Transmit ramp-down decrement registers
Tx Data Path Access Points		
$0x50-$0x51	**TxDataAccess**	Transmit path data access point (I)
$0x52-$0x53	**TxDataAccess**	Transmit path data access point (Q)
$0x54-$0x5F		Not Used
Self Test Registers		
$0x60-$0x61	**BISTPRSG**	Built-in self test pseudo-random sequence generator
$0x62	**BISTControl**	Built-in self test control register
$0x63		Not Used
$0x64-$0x6D	**BISTCRCRegisters**	Built-in self test cyclic redundancy code checkers
$0x6E-$0x6F		Not Used
SRAM Memory Access Points		
$0x70-$0x73	**SramData**	Auxiliary DAC1 memory I/O access addresses
$0x74-$0x7F		Not Used

Note: Addresses $0x80 to $0xFF cannot be used as the MSB controls the direction of data flow:
"1" = High = Read and "0" = Low = Write.

4.7.1.1 ConfigCtrl1

Title:	Configuration Control register
Address:	$0x00
Function:	RW
Description:	General configuration bits, together with operational control signal bits.

Bit	Name	Active	State	Function
7	*DataRateHi*	High	RW	When set active all serial port data transfers will be at half of the master clock rate. When inactive, all serial port data rates will be at a quarter of the master clock rate. This has the effect of altering the Rx sample output rate from 8 times the symbol rate when active to 4 times when inactive.
6	*TxHandshakeEn*	High	RW	When set active enable the transmit hardware interlock protocol, thereby stopping the *Serial Clock* (SClk) if the transmit path is enabled and the transmit FIFO is full.
5	*BiDirCmdPortEn*	High	RW	When this bit is set active the *Cmd* port will drive its data line out of the chip for the last 8 bits of read operations. When set inactive command read data will be returned on either the *Rx* or the *CmdRd* port (default).
4	*RxDataForCmdRdEn*	High	RW	This bit only takes effect if the *BiDirCmdPortEn* bit is inactive. When set active this bit causes all command read operations to respond with data on the *Rx* serial port. When set inactive the command read data will be output via the *CmdRd* port (default).
(5,4)	*CommandReadDataMode*		RW	The *BiDirCmdPortEn* bit and *RxDataForCmdRdEn* bit together control the method by which command read data is returned to the user.
		00		(Default) Read data returned on *CmdRd* port.
		01		Read data returned on *Rx* port and *CmdRd port*
		10,11		Read data returned on *Cmd* port.
3	*LowRxRdFS*	High	RW	When set active both the CmdRdFS and the RxFS output pins will be driven active low, when set inactive the two frame sync's will be driven active high (default).
2	*RxDataPortDisable*	High	RW	When set active tristates the RxDat and RxFS pins.
1	*RdCmdPortDisable*	High	RW	When set active tristates the CmdRdDat and CmdRdFS pins.
0	*SymboModuBypass*	High	RW	Setting this bit bypasses the Modulator, thereby taking the least significant 3 bits of each Command Transmit Data Serial Word received via the serial interface to represent an absolute constellation mapping.

- **Address and Data format for ConFigCtrl1 access**

Address field [6:0]						
0	0	0	0	0	0	0

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.2 ConfigCtrl2

Title: Configuration Control register

Address: $0x01

Function: RW

Description: General configuration bits, together with operational control signal bits.

Bit	Name	Active	State	Function
7			RW	Reserved. Set this bit Low. Undefined on read.
6			RW	User defined bit. This bit has no internal functionality and is reset Low with the global $\overline{\text{RESET}}$ pin. The user may employ this bit for any useful purpose.
5	*n_SlowDown*	Low	RW	When active, this bit reduces the slew rate of digital output pins. This reduces power consumption, ground bounce and reflection problems associated with fast edges on poorly terminated lines. De-activation speeds up the digital outputs, but increases power consumption, ground bounce and reflection problems. It is anticipated that the latter mode will be used only in 3.3V systems.
4	*SRamIoRdInc*	High	RW	This bit determines whether a read or write operation to the Auxiliary SRAM will increment the address pointers. When set active causes read operations to move the address pointer on, this would therefore allow an efficient write then read verify scheme to be used. When set inactive write operations increment the address pointer.
3	*SRamIoEn*	High	RW	When set active allows read/write access to the Auxiliary SRAM. It is only valid to activate this bit when the SRAM is not being accessed by the RamDac. When this bit is set active, the first access to SramData will access the first SRAM address location. Subsequent read or write accesses will increment the address pointer to the next memory location.
2	*CoeffRamIoRdInc*	High	RW	This bit determines whether a read or write operation to a coefficient memory will increment the address pointers. When set active the address pointer is incremented by any coefficient ram read operation, thereby allowing a write then read verification. When set inactive, write operations increment the address pointer.
1	*CoeffRamIoEn*	High	RW	When set active allows read/write access to all the coefficient memories. This bit is valid only when the Tx and Rx Data paths are inactive. When this bit is set active, the first access to any of the coefficient memories will access the first coefficient location (A1). Subsequent read or write accesses to any coefficient memory will increment the address pointers for all the coefficient memories.
0	*n_BigEndData*	Low	RW	When set active causes serial port read data, from the *Rx* port to be generated with the MSB data bit as the first serial word bit. If inactive, the LSB is first. On taking $\overline{\text{RESET}}$ Low this bit is active (i.e. the default is MSB first).

- **Address and Data format for ConFigCtrl2 access**

Address field [6:0]						
0	0	0	0	0	0	1

Data field [7:0]							
R	D6	D5	D4	D3	D2	D1	D0

4.7.1.3 PowerDownCtrl

Title: Power Control register

Address: $0x02

Function: RW

Description: This register, together with the following bits, controls the power saving features:

TxEn	bit of register	**TxSetup**
RxEn	bit of register	**RxSetup1**
TxClkStop	bit of register	**TxSetup**
RxClkStop	bit of register	**RxSetup1**

Bit	Name	Active	State	Function
7			RW	Reserved. Set this bit Low. Undefined on read.
6	*BiasICtrl*	High	RW	When set active, increases Tx and Rx analog bias currents.
5	*BiasPowDn*	Low	RW	When set active powers down the analog bias section.
4	*AuxDac4PowDn*	Low	RW	When set active powers down Auxiliary Dac4.
3	*AuxDac3PowDn*	Low	RW	When set active powers down Auxiliary Dac3.
2	*AuxDac2PowDn*	Low	RW	When set active powers down Auxiliary Dac2.
1	*AuxDac1PowDn*	Low	RW	When set active powers down Auxiliary Dac1.
0	*RxAafPowDn*	Low	RW	When set active powers down the receive analog anti-alias filter (AAF).

- **Address and Data format for PowerDownCtrl access**

Address field [6:0]						
0	0	0	0	0	1	0

Data field [7:0]							
R	D6	D5	D4	D3	D2	D1	D0

4.7.1.4 TxSetup

Title:	Transmit Set-up register
Address:	$0x03
Function:	RW
Description:	Sets up the transmit functions.

Bit	Name	Active	State	Function
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3	*TxClkStop*	High	RW	When set active causes the *TxEn* bit to also be used to gate the Tx Data path master clock. When inactive (default state) the Tx Data path master clock is always supplied.
2	*TxEn*	High	RW	When set active, enables the Tx Data path, allowing transmission to start when the correct enable sequence has been seen. This bit may only be cleared when the *TxPathEn* status bit in the TxFIFOStatus register is inactive, setting inactive during a transmission cycle will cause erroneous behaviour. This bit also acts as a transmit section power enable bit.
1	*TxRampEn*	High	RW	When set active, this bit enables the transmit amplitude ramping function. Ramping is then controlled by the *TxRampUp* bit of the TxData register When this bit is inactive, the *TxRampUp* bit will directly control the transmit amplitude (High meaning full amplitude, Low meaning zero amplitude).
0	*TxFirCoeffReset*	Low	RW	When set active this bit forces all the Tx Data path filters to load their default coefficient values. This bit will be set active on taking $\overline{\text{RESET}}$ Low, and therefore needs to be deactivated before default filter coefficients can be overwritten.

- **Address and Data format for TxSetup access**

Address field [6:0]						
0	0	0	0	0	1	1

Data field [7:0]							
R	R	R	R	D3	D2	D1	D0

4.7.1.5 TxData

Title: Transmit Data register

Address: $0x04 - $0x07 (Mapped over four locations, two address bits being used as data bits)

Function: W FIFO input
R FIFO output

Description: This transmit data register is 10 bits wide. The two least significant bits of the address bus are used to drive bits 8 and 9, hence it can be considered to be mapped over four consecutive locations. This data word is written into a FIFO. The function is only decoded when the FIFO is read (there is an exception for the first data word). The FIFO will be read when the Tx Data path demands data. This will only occur when the *TxEn* bit of the **TxSetup** register is set active. For test purposes the FIFO data output may be accessed by reading these registers.

Data write with symbol modulator not bypassed

Bit	Name	Active	State	Function
9	*TxRampUp*	High	W	This bit is written to the FIFO. While the *TxEn* bit of the TxSetup register is active, it controls the Tx Data path ramping. Setting it active will cause the amplitude to ramp up to its full value, conversely setting the bit inactive will cause the amplitude to ramp down to its minimum value. If the bit is changed while the amplitude is being ramped, the ramp direction will change to the direction set by this bit. While the *TxRampEn* bit is inactive, the *TxRampUp* bit will directly control the transmit amplitude (High meaning full amplitude and Low meaning zero amplitude).
8	*MultiSymbol*	High	W	This bit is written to the FIFO and when this bit is set active, the FIFO symbol data will be marked as a four symbol word. When set inactive, the FIFO symbol data will be marked as a single symbol word. This bit is inactive if the *SymbModuBypass* bit of the ConfigCtrl1 register is active.
7:6	*TxRelSymbol4*	Data	W	Fourth symbol in word to be written to FIFO.
5:4	*TxRelSymbol3*	Data	W	Third symbol in word to be written to FIFO.
3:2	*TxRelSymbol2*	Data	W	Second symbol in word to be written to FIFO.
1:0	*TxRelSymbol1*	Data	W	First symbol in word to be written to FIFO.

Data write with symbol modulator bypassed

Bit	Name	Active	State	Function
9	*TxRampUp*	High	W	(See above)
8:3	(not used)	Data	W	Redundant data which is still written into the FIFO. Set these bits Low.
2:0	*TxAbsSymbol*	Data	W	IQ constellation point which is written into the FIFO.

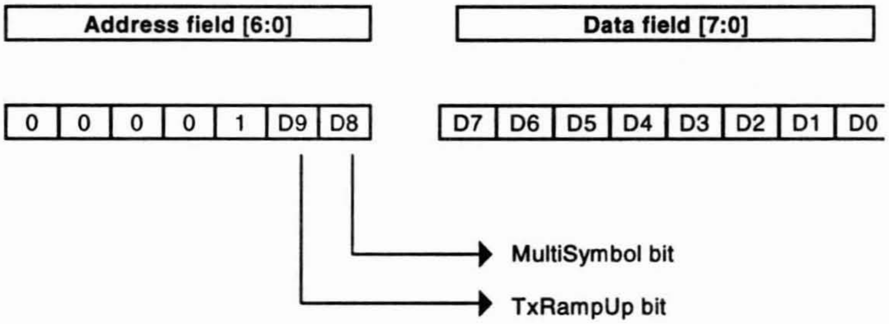
Read operation

Bit	Name	Active	State	Function
Address $0x04				
7:2				Reserved. Bit values are not defined.
1:0	*UpperFIFORdData*	Data	R	Reads address access bits 9 and 8 of the FIFO data output register, these are placed in bits 1 and 0.
Address $0x05				
7:0	*LowerFIFORdData*	Data	R	Reads address access bits 7 to 0 of the FIFO data output register. Reading this location also performs a FIFO read operation, thereby moving the next (if any) FIFO data location into the FIFO data output register.

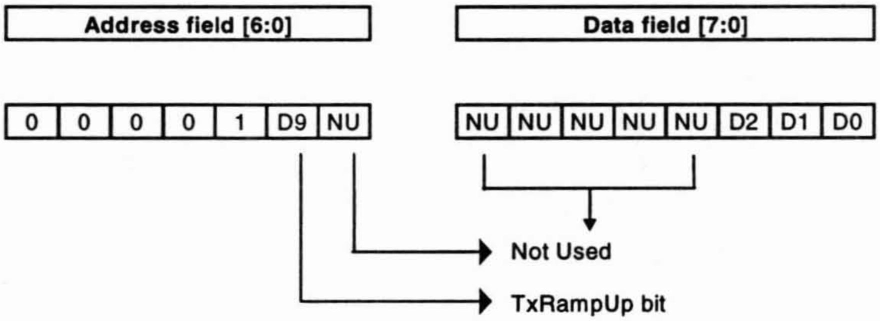
Address $0x06 and $0x07				
7:0			R	Reserved. Bit values are not defined.

For these read operations to be valid, the Tx Data path must be active *(TxEn* bit of **TxSetup** register set active) and the *SymbModuBypass* bit of the **ConfigCtrl1** register must also be set active.

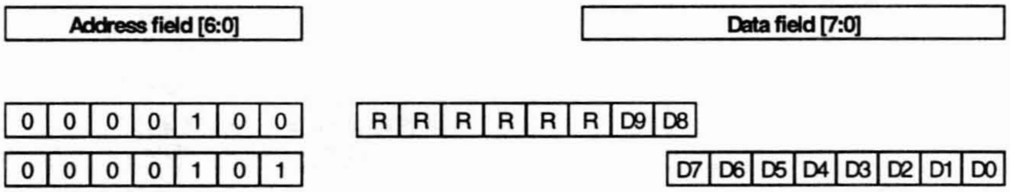
Address and Data format for TxData Write access


Address field [6:0]
Data field [7:0]
0
0
0
0
1
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
MultiSymbol bit
TxRampUp bit

Address and Data format for TxData (Modulator Bypass Mode) Write access


Address field [6:0]
Data field [7:0]
0
0
0
0
1
D9
NU
NU
NU
NU
NU
NU
D2
D1
D0
Not Used
TxRampUp bit

Address and Data format for TxData Read access


Address field [6:0]
Data field [7:0]
0 0 0 0 1 0 0
R R R R R R D9 D8
0 0 0 0 1 0 1
D7 D6 D5 D4 D3 D2 D1 D0

4.7.1.6 RxSetup1

Title: First Receive Set-up control register

Address: $0x08

Function: RW

Description: Receive path set-up and initialization control bits.

Bit	Name	Active	State	Function
7	*Rx32BitMode*	High	RW	When set active, the *Rx* port operates on 32-bit frames - I data in the MSB word, Q data in the LSB word.
6	*RxSampleSel*	High	RW	This bit is used to select which pair of I, Q samples is supplied from the possible two when the *DataRateHi* bit in ConfigCtrl1 register is in the low mode (inactive). It has no effect when *DataRateHi* is active.
5	*RxClkStop*	High	RW	When set active causes the *RxEn* bit to also be used to gate the Rx Data path master clock. When inactive (default state) the Rx Data path master clock is always supplied.
4	*RxEn*	High	RW	When set active, enables the Rx Data path, which then starts to process the differential data on the IRXP, IRXN and QRXP, QRXN pins, outputting results via the *Rx* serial port. This bit also acts as a receive section power enable bit.
3	*RxBistActive*	High	RW	When set active, enables Rx Built In Self Test (BIST) operation.
2	*AnaAdcReset*	Pulse	W	When this bit is set High, a 4-clock-cycle ADC auto reset event is generated. It is not necessary to clear this bit before another ADC auto reset event is initiated.
			R	The read state of this bit indicates the logic level last written to this bit. It does not have a functional significance and is only available for test purposes.
1	*AnaEnAutoReset*	Low	RW	When active this bit enables the ADC auto reset function. On taking $\overline{\text{RESET}}$ Low, this bit is set active, which is the default operating condition.
0	*RxFirCoeffReset*	Low	RW	When set active forces all the Rx Data path filters to load their default coefficient values. This bit will be set active on taking $\overline{\text{RESET}}$ Low, and therefore needs to be deactivated before default filter coefficients can be overwritten. Normal filter operation is unaffected by leaving this bit set.

- **Address and Data format for RxSetup1 access**

Address field [6:0]						
0	0	0	1	0	0	0

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.7 RxSetup2

Title: Second Receive Set-up control register
Address: $0x09
Function: RW
Description: Receive I and Q Vernier control bits.

Bit	Name	Active	State	Function
7:4	*QvernierDelay*	High	RW	Q channel Vernier sampling delay, allowing the sampling point to be adjusted to a resolution of 1/16 of the input sample clock rate.
3:0	*IvernierDelay*	High	RW	I channel Vernier sampling delay, allowing the sampling point to be adjusted to a resolution of 1/16 of the input sample clock rate.

Note: The values are in the format of 4 bit signed 2s-complement integers - the MSB being the sign. Thus it can be interpreted as adjusting the reference phase by ± 7/16 of the sample clock period.

- **Address and Data format for RxSetup2 access**

Address field [6:0]						
0	0	0	1	0	0	1

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.8 AnaCtrl

Title: Analog configuration Control register
Address: $0x0A
Function: RW
Description: Reserved. All bits should be set Low.

4.7.1.9 AuxAdcCtrl

Title:	Auxiliary ADC data converter Control register
Address:	$0x0B
Function:	RW
Description:	This register controls the operation of the four ADC channels. These are implemented using a single ADC converter, which is multiplexed on to each of the ADC channels. A conversion cycle consists of performing a conversion for each of the active channels in turn.

Bit	Name	Active	State	Function
7			RW	Reserved. Set this bit Low. Undefined on read.
6	*AdcConvertRate*	High	RW	This bit changes the ADC conversion rate. If this bit is set Low, the ADC is clocked by MCLK/8, yielding a conversion time of 80x MCLK periods per ADC channel. The maximum sample rate is lower than this. With a single channel selected, the maximum rate is MCLK/112 samples/second. Setting this bit high will halve the ADC clock rate, and hence double the conversion time.
5	*AdcContConv*	High	RW	Continuous conversion mode control bit; when inactive, sets the ADCs into one-shot conversion mode; when active, the ADCs will continuously convert. One-shot conversion mode is initiated by the *StartConvert* bit. In continuous convert mode, the ADC will start a new conversion cycle on all active channels after the previous cycle has completed.
4	*EnableAdc4*	High	RW	Setting this bit high will enable ADC channel 4 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
3	*EnableAdc3*	High	RW	Setting this bit high will enable ADC channel 3 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
2	*EnableAdc2*	High	RW	Setting this bit high will enable ADC channel 2 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
1	*EnableAdc1*	High	RW	Setting this bit high will enable ADC channel 1 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
0	*StartConvert*	High		One-shot conversion control bit. Only valid when the ADCs are set to one-shot conversion mode.
			W	Setting this bit High starts the ADC data conversion. Setting this bit Low will stop the conversion. This should only be used for test purposes, because the ADC conversion logic will automatically set this bit Low when the conversion operation has completed.
			R	This bit can be set High or Low by the serial interface, but the ADC conversion logic will automatically set it Low when the current conversion cycle has completed.

- **Address and Data format for Auxillary ADC Control access**

Address field [6:0]						
0	0	0	1	0	1	1

Data field [7:0]							
R	D6	D5	D4	D3	D2	D1	D0

4.7.1.10 AuxAdcData

Title: Auxiliary ADC Data registers

Address: (Eight registers) $0x10 to $0x17

Function: R

Description: These registers enable the user to inspect the conversion value for each of the four auxiliary ADCs. There are two read registers per ADC, one to obtain the least significant two bits of the data, the other for the most significant eight bits. Reading these registers does not affect the ADC conversion cycle. Reading the MSB read register directly reads the ADC output and simultaneously causes the two bits in the LSB read register to be written into a holding register. This holding register is read when the LSB read register is read. This mechanism is necessary to allow the user to read MSB and LSB data from the same ADC conversion cycle. If only the MSB read register is read, the converter can be considered as an 8-bit ADC. If a 10-bit conversion is required, the MSB read register must be read first.

Bit	Name	Active	State	Function
Address $0x10				
7:0	*Adc1MsbData*	Data	R	Most significant eight bits of the data from the last conversion of *AuxAdc1*.
Address $0x11				
7:2			R	Reserved. Bit values are not defined.
1:0	*Adc1LsbData*	Data	R	Least significant two bits of the data from the last conversion of *AuxAdc1*.
Address $0x12				
7:0	*Adc2MsbData*	Data	R	Most significant eight bits of the data from the last conversion of *AuxAdc2*.
Address $0x13				
7:2			R	Reserved. Bit values are not defined.
1:0	*Adc2LsbData*	Data	R	Least significant two bits of the data from the last conversion of *AuxAdc2*.
Address $0x14				
7:0	*Adc3MsbData*	Data	R	Most significant eight bits of the data from the last conversion of *AuxAdc3*.
Address $0x15				
7:2			R	Reserved. Bit values are not defined.
1:0	*Adc3LsbData*	Data	R	Least significant two bits of the data from the last conversion of *AuxAdc3*.
Address $0x16				
7:0	*Adc4MsbData*	Data	R	Most significant eight bits of the data from the last conversion of *AuxAdc4*.
Address $0x17				
7:2			R	Reserved. Bit values are not defined.
1:0	*Adc4LsbData*	Data	R	Least significant two bits of the data from the last conversion of *AuxAdc4*.

Address and Data format for Auxillary ADC Data access

Address field [6:0]						
0	0	1	0	N1	N0	0
0	0	1	0	N1	N0	1

Data field [9:0]									
		R	R	R	R	R	R	D1	D0
D9	D8	D7	D6	D5	D4	D3	D2		

N1	N0	ADC Channel
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

4.7.1.11 RamDacCtrl

Title:	RamDac Control register
Address:	$0x0C
Function:	RW
Description:	This register controls the operation of DAC 1, together with the operation of the memory (DacSram) which can be used to drive the digital input of DAC 1.

Bit	Name	Active	State	Function
7:6			RW	Reserved. These bits should be set Low. Undefined on read.
5:3	*RamDacRate*	High	RW	These three bits set the rate at which the RamDac memory's DAC access address pointer changes. The three bit value (RamDacRate) causes a change rate of (36 x $2^{RamDacRate}$) kHz. See table below.
2	*RamDacInc*	High	RW	This bit activates the RamDac memory scan operation. Setting it active will cause the memory address to increment up to the top (highest) location, conversely setting the bit inactive will cause the memory address to decrement down to the bottom location. If the bit is changed while the memory is being scanned, the current scan will complete before the new state of the *RamDacInc* bit takes effect.
1	*AutoCycle*	High	RW	This bit is only valid if the *RamDacActive* bit is active. When set active, the Auxiliary SRAM memory will be continually scanned at the rate set by the *RamDacRate* bits. This enables a symmetrical periodic waveform to be driven out on the AUXDAC1 pin. The Auxiliary SRAM address cycles from the bottom location up to the top location, and back down to the bottom again.
0	*RamDacActive*	High	RW	DAC 1 input mode bit. When inactive, the AuxDacData registers (offsets 0 and 1) are used as the source for conversion. If this bit is active, the DAC is driven from the output of the RamDac memory.

RamDacCtrl[5:3]	Dac Update Frequency (kHz)
0 0 0	36
0 0 1	72
0 1 0	144
0 1 1	288
1 0 0	576
1 0 1	1152
1 1 0	2304
1 1 1	4608

Ram Dac Rate Select Table

- **Address and Data format for RamDacCtrl access**

Address field [6:0]

0	0	0	1	1	0	0

Data field [7:0]

R	R	D5	D4	D3	D2	D1	D0

4.7.1.12 AuxDacData

Title:	Auxiliary DAC Data registers
Address:	(Eight registers) $0x18 to $0x1F
Function:	RW
Description:	There are two input registers for each of the four auxiliary DACs. Writing to the *AuxDac#LsbData* register writes the least significant two bits of DAC data. Writing to the *AuxDac#MsbData* register writes the most significant eight bits of DAC data and then passes all ten bits to the appropriate DAC input (only if the *RamDacActive* bit is set Low for DAC 1). If the *AuxDac#MsbData* register is written while the *AuxDac#LsbData* register is left constant, the converter may be treated as an 8-bit DAC.

Bit	Name	Active	State	Function
Address $0x18				
7:2			RW	Reserved. These bits should be set Low. Undefined on read.
1:0	*AuxDac1LsbData*	Data	RW	Writing to this address writes the least significant two bits of the *DacData1* register. These two bits may be read for test purposes.
Address $0x19				
7:0	*AuxDac1MsbData*	Data	RW	Writing to this address writes the most significant eight bits of the *DacData1* register and updates DAC 1. This register may also be read for test purposes.
Address $0x1A				
7:2			RW	Reserved. These bits should be set Low. Undefined on read.
1:0	*AuxDac2LsbData*	Data	RW	Writing to this address writes the least significant two bits of the *DacData2* register. These two bits may be read for test purposes.
Address $0x1B				
7:0	*AuxDac2MsbData*	Data	RW	Writing to this address writes the most significant eight bits of the *DacData2* register and updates DAC 2. This register may also be read for test purposes.
Address $0x1C				
7:2			RW	Reserved. These bits should be set Low. Undefined on read.
1:0	*AuxDac3LsbData*	Data	RW	Writing to this address writes the least significant two bits of the *DacData3* register. These two bits may be read for test purposes.
Address $0x1D				
7:0	*AuxDac3MsbData*	Data	RW	Writing to this address writes the most significant eight bits of the *DacData3* register and updates DAC 3. This register may also be read for test purposes.
Address $0x1E				
7:2			RW	Reserved. These bits should be set Low. Undefined on read.
1:0	*AuxDac4LsbData*	Data	RW	Writing to this address writes the least significant two bits of the *DacData4* register. These two bits may be read for test purposes.
Address $0x1F				
7:0	*AuxDac4MsbData*	Data	RW	Writing to this address writes the most significant eight bits of the *DacData4* register and updates DAC 4. This register may also be read for test purposes.

- **Address and Data format for Auxillary DAC Data access**

Address field [6:0]

0	0	1	1	N1	N0	0
0	0	1	1	N1	N0	1

Data field [9:0]

R	R	R	R	R	R	D1	D0
D9	D8	D7	D6	D5	D4	D3	D2

N1 N0	Channel Selected
0 0	Channel 1
0 1	Channel 2
1 0	Channel 3
1 1	Channel 4

4.7.1.13 LoopBackCtrl

Title: LoopBack Control register

Address: $0x0D

Function: RW

Description: This register is only used for test purposes. For normal operation all these bits should be inactive.

Bit	Name	Active	State	Function
7:6			RW	Reserved. These bits should be set Low. Undefined on read.
5	*FirReset*	High	RW	When active, this bit holds all FIR filters in reset, by resetting the FIR address pointers. This by itself does not reset the data register RAMs. A separate access is provided to disable the complete Tx or Rx Data path. Taking $\overline{\text{RESET}}$ Low will also reset the FIR filter coefficients to their default values.
4	*DigLoopBack*	High	RW	When set active this bit enables the digital loopback feature. This connects the output of the Rx Data path 49-tap filter to the input of the Tx Data path 49-tap digital filter, thereby allowing an analog signal presented at the Rx inputs to be filtered by a raised cosine filter and monitored at the Tx outputs as an analog signal.
3	*AnaLoopBack*	High	RW	When set active this bit enables the analog loopback feature. This connects the output of the Tx Data path DAC to the input of Rx Data path ADC, thus passing transmit constellation data through a raised cosine filter and allowing the resultant data samples to be monitored digitally at the Rx output.
2	*RxDPAccessSel*	High	RW	When set active this bit disables the Rx Data path sample clock, thereby enabling the Data path access register to directly update the output of the Rx Data path operator.
1	*TxDPAccessSel*	High	RW	When set active this bit disables the Tx Data path sample clock, thereby enabling the Data path access register to directly update the input to the 15-tap digital filter without the data being overridden by subsequent sample clocks
0	*TxtoRxDataPath*	High	RW	When set active this bit connects the Tx (I,Q) DAC input to the serial receive port (*Rx*). This enables the output of the transmit 15-tap filter to be observed in real time. Data is taken from the I and Q channels on alternate 144kHz sample clocks.

- **Address and Data format for LoopBackCtrl access**

Address field [6:0]						
0	0	0	1	1	0	1

Data field [7:0]							
R	R	D5	D4	D3	D2	D1	D0

4.7.1.14 TxErrorStatus

Title:	Transmit Error Status register.
Address:	$0x0E
Function:	R
Description:	This register is the Tx Data path error status register. The *TxIrqActive* bit is set active when one of the other bits in this register is the source of an interrupt event. All these error conditions are caused by transitory events, therefore the error condition is latched (marked with an 'L'). Reading this status register causes all latched bits to be set inactive, unless an error event is currently pending.

Setting any bit of this register High will cause an interrupt to be generated ($\overline{IRQ}$ will be set Low) if the source of the interrupt has not been masked in the corresponding Mask register.

Bit	Name	Active	State	Function
7			R	Reserved. Bit value is not defined.
6	*TxDataPathQOF*	High	RL	Data path gain, phase and offset (GPO) adjustment-unit: Q channel overflow error status bit.
5	*TxDataPathIOF*	High	RL	Data path gain, phase and offset (GPO) adjustment-unit: I channel overflow error status bit.
4	*Tx15tapQOF*	High	RL	15-tap Q filter data accumulator overflow error status bit.
3	*Tx15tapIOF*	High	RL	15-tap I filter data accumulator overflow error status bit.
2	*Tx49tapOF*	High	RL	49-tap I and Q filter data accumulator overflow error status bit.
1	*Tx79tapOF*	High	RL	79-tap I and Q filter data accumulator overflow error status bit.
0	*TxIrqActive*	High	RL	This bit is set High if there is an active interrupt caused by one of the status bits in this register.

- **Address and Data format for TxErrorStatus access**

Address field [6:0]						
0	0	0	1	1	1	0

Data field [7:0]							
R	D6	D5	D4	D3	D2	D1	D0

4.7.1.15 TxErrStatMask

Title:	Transmit Error Status interrupt Mask register
Address:	$0x0F
Function:	RW
Description:	Masks interrupts in the **TxErrorStatus** register. On taking $\overline{\text{RESET}}$ Low, these bits are set active, so masking out all possible interrupt sources. Each bit which is taken inactive will allow its associated status bit, when active, to generate an interrupt.

Bit	Name	Active	State	Function
7		Data	RW	Reserved for manufacturer's test purposes. This bit should be set Low.
6	*n_TxDataPathQOF_Mask*	Low	RW	GPO Q channel error interrupt mask bit.
5	*n_TxDataPathIOF_Mask*	Low	RW	GPO I channel error interrupt mask bit.
4	*n_Tx15tapQOF_Mask*	Low	RW	15-tap Q filter error interrupt mask bit.
3	*n_Tx15tapIOF_Mask*	Low	RW	15-tap I filter error interrupt mask bit.
2	*n_Tx49tapOF_Mask*	Low	RW	49-tap I and Q filter error interrupt mask bit.
1	*n_Tx79tapOF_Mask*	Low	RW	79-tap I and Q filter error interrupt mask bit.
0		Data		Reserved for manufacturer's test purposes. This bit should be set Low.

- **Address and Data format for TxErrStatMask access**

Address field [6:0]						
0	0	0	1	1	1	1

Data field [7:0]							
R	D6	D5	D4	D3	D2	D1	R

4.7.1.16 RxErrorStatus

Title:	Receive Error Status register.
Address:	$0x20
Function:	R
Description:	This register is the Rx Data path error status register. The *RxIrqActive* bit is set active when one of the other bits in this register is the source of an interrupt event. All these error conditions are caused by transitory events, therefore the error condition is latched (marked with an 'L'). Reading this status register causes all latched bits to be set inactive unless an error event is currently pending. Setting any bit of this register High will cause an interrupt to be generated ($\overline{IRQ}$ will be set Low) if the source of the interrupt has not been masked in the corresponding Mask register.

Bit	Name	Active	State	Function
7	*RxDataPathQOF*	High	RL	Data path gain, phase and offset (GPO) adjustment unit: Q channel overflow error status bit.
6	*RxDataPathIOF*	High	RL	Data path gain, phase and offset (GPO) adjustment unit: I channel overflow error status bit.
5	*AdcQOF*	High	RL	ADC Q channel overflow error due to excessive input amplitude.
4	*AdcIOF*	High	RL	ADC I channel overflow error due to excessive input amplitude.
3	*Rx63tapOF*	High	RL	63-tap I and Q filter data accumulator overflow error status bit.
2	*Rx49tapOF*	High	RL	49-tap I and Q filter data accumulator overflow error status bit.
1	*EvenSamplePhase*	High	RL	When this status bit is active, the associated interrupt may be used to re-synchronize the Rx data if for any reason data synchronization is lost. If the corresponding mask bit is set inactive, an interrupt will be generated on the next Q-phase data in the Rx output register. The next falling edge of SClk with RxFS High indicates the LSB of the Q channel data. The mask bit should be disabled after this to prevent continuous Q-phase interrupts.
0	*RxIrqActive*	High	RL	This bit is set High if there is an active interrupt caused by one of the status bits in this register.

- **Address and Data format for RxErrorStatus access**

Address field [6:0]						
0	1	0	0	0	0	0

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.17 RxErrorStatMask

Title:	Receive Error Status interrupt Mask register.
Address:	$0x21
Function:	RW
Description:	Masks interrupts in the **RxErrorStatus** register. On taking $\overline{\text{RESET}}$ Low, these bits are set active, so masking out all possible interrupt sources. Each bit which is taken inactive will allow its associated status bit, when active, to generate an interrupt.

Bit	Name	Active	State	Function
7	*n_RxDataPathQOF_Mask*	Low	RW	GPO Q channel error interrupt mask bit.
6	*n_RxDataPathIOF_Mask*	Low	RW	GPO I channel error interrupt mask bit.
5	*n_AdcQOF_Mask*	Low	RW	ADC Q channel error interrupt mask bit.
4	*n_AdcIOF_Mask*	Low	RW	ADC I channel error interrupt mask bit.
3	*n_Rx63tapOF_Mask*	Low	RW	63-tap I and Q filter error interrupt mask bit.
2	*n_Rx49tapOF_Mask*	Low	RW	49-tap I and Q filter error interrupt mask bit.
1	*EvenSamplePhase_Mask*	Low	RW	Rx data Q-phase interrupt mask bit.
0		Data	RW	Reserved for manufacturer's test purposes. This bit should be set Low.

- **Address and Data format for RxStatMask access**

Address field [6:0]						
0	1	0	0	0	0	1

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	R

4.7.1.18 TxFIFOStatus

Title: Transmit data FIFO Status register

Address: $0x22

Function: R

Description: This register is the Tx Data FIFO status register. The *TxIrqActive* bit is set active when one of the other bits in this register is the source of an interrupt event. Some of these status conditions are caused by transitory events, therefore their state is latched (marked with an 'L'). The bits marked with a parenthesized 'L' are only latched in their interrupt generation state if their associated mask bit is inactive. Reading this status register causes all latched bits to be set inactive, unless an error event is currently pending.

Setting any bit of this register High will cause an interrupt to be generated ($\overline{\text{IRQ}}$ will be set Low) if the source of the interrupt has not been masked in the corresponding Mask register.

Bit	Name	Active	State	Function
7	*TxPathEn*	High/Low	R(L)	When active (High) this bit shows that the Tx Data path is currently active. This enables the user to confirm that ramp down has completed. For interrupt generation purposes, a logic Low on this bit will be considered as active.
6	*FIFOUnderRead*	High	RL	Error status bit. When active indicates a read from the FIFO occurred while the FIFO was empty.
5	*FIFOOverWrite*	High	RL	Error status bit. When active indicates a write to the FIFO occurred while the FIFO was full.
4	*FIFOFull*	High/ Low	R(L)	Most significant FIFO length status bit. When active (High) this bit also indicates the FIFO is full. For interrupt generation purposes, a logic Low on this bit will be considered as active.
3:2	*FIFOLength*	(Low)	R(L)	These two bits contain the pointer to the next free FIFO address and indicate the following status: 00 - indicates FIFO is empty 01 - one location used 10 - two locations used 11 - three locations used For interrupt generation purposes, a logic Low on either of these bits will be considered as active.
1	*FIFOEmpty*	High	R(L)	When active indicates the FIFO is empty.
0	*FifoIrqActive*	High	RL	This bit is set High if there is an active interrupt caused by one of the status bits in this register.

- **Address and Data format for TxFIFOStatus access**

Address field [6:0]						
0	1	0	0	0	1	0

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.19 TxFIFOStatMask

Title:	Transmit data FIFO Status interrupt Mask register
Address:	$0x23
Function:	RW
Description:	Masks interrupts in the **TxFIFOStatus** register. On taking $\overline{\text{RESET}}$ Low, these bits are set active, so masking out all possible interrupt sources. Each inactive bit will allow its associated status bit to generate an interrupt. In the case of the status bits marked in the **TxFIFOStatus** register with a parenthesized 'L', taking the mask bit inactive will enable the latching mechanism.

Bit	Name	Active	State	Function
7	*n_TxPathEn_Mask*	Low	RW	Tx Data path active interrupt mask bit.
6	*n_FIFOUnderRead_Mask*	Low	RW	FIFO underflow interrupt mask bit.
5	*n_FIFOOverWrite_Mask*	Low	RW	FIFO overflow interrupt mask bit.
4	*n_FIFOFull_Mask*	Low	RW	FIFO full interrupt mask bit.
3	*n_FIFOLength1_Mask*	Low	RW	FIFO length status (MSB) interrupt mask bit.
2	*n_FIFOLength0_Mask*	Low	RW	FIFO length status (LSB) interrupt mask bit.
1	*n_FIFOEmpty_Mask*	Low	RW	FIFO empty interrupt mask bit.
0		Data	RW	Reserved for manufacturer's test purposes. This bit should be set Low.

- **Address and Data format for TxFIFOStatMask access**

Address field [6:0]						
0	1	0	0	0	1	1

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	R

4.7.1.20 CoeffRamData

Title: I/O access addresses for the five coefficient memories.

Address: $0x24 to $0x2D (mapped over 10 locations)

Function: RW

Description: Each coefficient RAM has both MSB and LSB address ports assigned for read/write access. There are three transmit (Tx) FIR filters with read/write coefficients and two receive (Rx) filters, with coefficient sizes of 12 and 16 bits respectively. Access to the coefficient memory is valid when the *CoeffRamIoEn* bit is active.

Asserting the *CoeffRamIoEn* will reset the *Coefficient Address Pointer* to the first location (A1). The MSB port should be accessed first, as accessing the LSB port will move the *Coefficient Address Pointer* to the next coefficient location (A[n+1]) (refer to description of *CoeffRamIoRdInc* bit for details). Subsequent accesses to the LSB port of the coefficient address will increment the *Coefficient Address Pointer.*

As all filters are symmetrical and "odd", only $\frac{N+1}{2}$ locations can be programmed, where N is the filter tap length. Performing an I/O access after the last *Coefficient Address Pointer* is not valid, and may corrupt existing coefficients. Only one FIR filter coefficient RAM may be accessed at a time. If further memories are to be accessed then the *CoeffRamIoEn* must first be deactivated, and then activated again, allowing the next FIR filter coefficient RAM to be incrementally accessed.

Bit	Name	Active	State	Function
Address $0x24				
7:0	*Tx15tapCoeffLSB*	Data	RW	Transmit 15-tap filter LSB coefficient data port. Post-increment the coefficient address pointer.
Address $0x25				
7:4			RW	Reserved. Set these bits High. Undefined on read.
3:0	*Tx15tapCoeffMSB*	Data	RW	Transmit 15-tap filter MSB coefficient data port.
Address $0x26				
7:0	*Tx49tapCoeffLSB*	Data	RW	Transmit 49-tap filter LSB coefficient data port. Post-increment the coefficient address pointer.
Address $0x27				
7:4			RW	Reserved. Set these bits High. Undefined on read.
3:0	*Tx49tapCoeffMSB*	Data	RW	Transmit 49-tap filter MSB coefficient data port.
Address $0x28				
7:0	*Tx79tapCoeffLSB*	Data	RW	Transmit 79-tap filter LSB coefficient data port. Post-increment the coefficient address pointer.
Address $0x29				
7:4			RW	Reserved. Set these bits High. Undefined on read.
3:0	*Tx79tapCoeffMSB*	Data	RW	Transmit 79-tap filter MSB coefficient data port.
Address $0x2A				
7:0	*Rx49tapCoeffLSB*	Data	RW	Receive 49-tap filter LSB coefficient data port. Post-increment the coefficient address pointer.
Address $0x2B				
7:0	*Rx49tapCoeffMSB*	Data	RW	Receive 49-tap filter MSB coefficient data port.
Address $0x2C				
7:0	*Rx63tapCoeffLSB*	Data	RW	Receive 63-tap filter LSB coefficient data port. Post-increment the coefficient address pointer.
Address $0x2D				
7:0	*RX63tapCoeffMSB*	Data	RW	Receive 63-tap filter MSB coefficient data port.

- **Address and Data format for 15-tap Tx FIR Coefficient Ram IO access**

Address field [6:1]												**Coefficient Data field [11:0]**										
0	1	0	0	1	0	A0																
(Coefficient Pointer)++						0									D7	D6	D5	D4	D3	D2	D1	D0
Coefficient Pointer						1	R	R	R	R	D11	D10	D9	D8								

- **Address and Data format for 49-tap Tx FIR Coefficient Ram IO access**

Address field [6:1]												**Coefficient Data field [11:0]**										
0	1	0	0	1	1	A0																
(Coefficient Pointer)++						0									D7	D6	D5	D4	D3	D2	D1	D0
Coefficient Pointer						1	R	R	R	R	D11	D10	D9	D8								

- **Address and Data format for 79-tap Tx FIR Coefficient Ram IO access**

Address field [6:1]												**Coefficient Data field [11:0]**										
0	1	0	1	0	0	A0																
(Coefficient Pointer)++						0									D7	D6	D5	D4	D3	D2	D1	D0
Coefficient Pointer						1	R	R	R	R	D11	D10	D9	D8								

- **Address and Data format for 49-tap Rx FIR Coefficient Ram IO access**

Address field [6:1]							**Coefficient Data field [15:0]**															
0	1	0	1	0	1	A0																
(Coefficient Pointer)++						0									D7	D6	D5	D4	D3	D2	D1	D0
Coefficient Pointer						1	D15	D14	D13	D12	D11	D10	D9	D8								

- **Address and Data format for 63-tap Rx FIR Coefficient Ram IO access**

Address field [6:1]							**Coefficient Data field [15:0]**															
0	1	0	1	1	0	A0																
(Coefficient Pointer)++						0									D7	D6	D5	D4	D3	D2	D1	D0
Coefficient Pointer						1	D15	D14	D13	D12	D11	D10	D9	D8								

4.7.1.21 SramData

Title: I/O access address for the auxiliary DAC1 memories.

Address: $0x70 to $0x73 (mapped over 4 locations)

Function: RW

Description: These four address locations allow access to the 64 x 10 bit SRAM. The contents of this RAM can be pre-loaded with a table of values which can be automatically sent to auxiliary DAC1 in either a single cycle or continuous mode, see RamDacCtrl for details. Therefore the RAM can be used in conjunction with DAC1 to enable user defined profile power ramping of an external RF power transmitter stage.

The RAM contents are addressed incrementally by first taking the *SRamIoEn* bit active. While this bit is inactive the *SRam Address Pointer* is held reset. The physical address applied to the RAM is formed from the 4-bit *SRam Address Pointer* and the two LSB bits from the I/O Access address (A1,A0). Therefore four locations in the RAM can be accessed by directly addressing $0x70 to $0x73. However, accessing location $0x73 post-increments (by a block of four addresses) the *SRam Address Pointer*, thus moving the pointer to the next RAM location block.

The 10-bit data word is split between "odd" and "even" locations with the MSB byte in "odd" addresses
(A0 = 1) and 2 LSB's in "even" addresses.

The *SRamIoRdInc* bit determines whether a read or a write operation will increment the *SRam Address Pointer*. All 16 locations are accessed incrementally, further accesses to this port while the *SRamIoEn* bit is active are not valid and may cause data loss.

Bit	Name	Active	State	Function
Address $0x70				
7:2			RW	Reserved. Set these bits Low. Undefined on read.
1:0	*SRamLSBPort0*	Data	RW	Access port for the LSB register.
Address $0x71				
7:0	*SRamMSBPort0*	Data	RW	Access port for the MSB register
Address $0x72				
7:2			RW	Reserved. Set these bits Low. Undefined on read.
1:0	*SRamLSBPort1*	Data	RW	Access port for the LSB register.
Address $0x73				
7:0	*SRamMSBPort3*	Data	RW	Access port for the MSB register. Post-increment *Sram* address pointer.

- **Address and Data format for Sram Data I/O access**

Address field [6:0]							**Data field [9:0]**								
1	1	1	0	0	A1	A0									
Sram Address Pointer					0	0			R	R	R	R	R	R	D1	D0
Sram Address Pointer					0	1	D9	D8	D7	D6	D5	D4	D3	D2		
Sram Address Pointer					1	0			R	R	R	R	R	R	D1	D0
(Sram Address Pointer)++					1	1	D9	D8	D7	D6	D5	D4	D3	D2		

4.7.1.22 TxRampUpInc

Title: Transmit Ramp Up Increment registers.

Address: $0x4C to $0x4D (mapped over 2 locations)

Function: RW

Description: The value in this register sets the scale of the Tx amplitude gain increments which occur over each sample clock period, thus determining the Tx amplitude ramp up time period. The value is always positive. The ramp up rate, in terms of the number of symbols, is given by the formula:

$$N_{symbols} = \frac{64}{N_{dec}}$$

Where: $N_{symbols}$ is the ramp time in terms of number of symbols.

N_{dec} is the value in the register.

Bit	Name	Active	State	Function
Address $0x4C				
7:0	*RampUpIncLSB*	Data	RW	Least significant 8 bits of the ramp up increment register.
Address $0x4D				
7:1			RW	Reserved. Set these bits Low. Undefined on read.
0	*RampUpIncMSB*	Data	RW	Most significant bit of the ramp up increment register.

- **Address and Data format for TxRampUpInc access**

Address field [6:0]	Data field [8:0]
1 0 0 1 1 0 0	D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1 1 0 1	R R R R R R R D8

4.7.1.23 TxRampDnDec

Title:	Transmit Ramp Down Decrement registers.
Address:	\$0x4E to \$0x4F (mapped over 2 locations)
Function:	RW
Description:	The value in this register sets the scale of the Tx amplitude gain decrements which occur over each sample clock period, thus determining the Tx amplitude ramp down time period. The value is always positive. The ramp down rate, in terms of the number of symbols, is given by the formula:

$$N_{symbols} = \frac{64}{N_{inc}}$$

Where: $N_{symbols}$ is the ramp time in terms of number of symbols.

N_{inc} is the value in the register.

Bit	Name	Active	State	Function
Address \$0x4E				
7:0	*RampDnIncLSB*	Data	RW	Least significant 8 bits of the ramp down increment register.
Address \$0x4F				
7:1			RW	Reserved. Set these bits Low. Undefined on read.
0	*RampDnIncMSB*	Data	RW	Most significant bit of the ramp down increment register.

- **Address and Data format for TxRampDnDec access**

Address field [6:0]							Data field [8:0]															
1	0	0	1	1	1	0									D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	1	R	R	R	R	R	R	R	D8								

4.7.1.24 TxIQGainMult

Title: Transmit I and Q channel Gain Multiplier registers

Address: $0x42, $0x43 , $0x48 and $0x49 (4 locations)

Function: RW

Description: A 2s-complement multiplication is performed on the magnitude of the Tx Data path signal and the result is then re-normalized to the system's dynamic range: thus the function may be considered as a digital attenuator. This register sets the multiplier, the result being given by the formula:

$$D_{out} = D_{in}\left[\frac{G_{val}}{2^{11}}\right]$$

Where:
D_{in} is the signal input,
D_{out} is the signal output,
G_{val} is the value in the register.

Bit	Name	Active	State	Function
Address $0x42				
7:0	*TxIGainLSB*	Data	RW	Least significant 8 bits of the TxIGain register (G_{val}).
Address $0x43				
7:3			RW	Reserved. Set these bits Low. Undefined on read.
2:0	*TxIGainMSB*	Data	RW	Most significant 3 bits of the TxIGain register (G_{val}).
Address $0x48				
7:0	*TxQGainLSB*	Data	RW	Least significant 8 bits of the TxQGain register (G_{val}).
Address $0x49				
7:3			RW	Reserved. Set these bits Low. Undefined on read.
2:0	*TxQGainMSB*	Data	RW	Most significant 3 bits of the TxQGain register (G_{val}).

- **Address and Data format for TxIGain access**

Address field [6:0]							Data field [10:0]							
1	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	1	R	R	R	R	R	D10	D9	D8

- **Address and Data format for TxQGain access**

Address Field [6:0]							Data field [10:0]							
1	0	0	1	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	R	R	R	R	R	D10	D9	D8

4.7.1.25 TxIQOffset

Title: Transmit I and Q channel Offset correction register

Address: $0x44, $0x45, $0x4A, and $0x4B (4 locations)

Function: RW

Description: This register controls the Tx Data path signal offset. This offset is a 2s-complement value (N_{offset}), which is applied to the Tx signal after the Gain Multiplier (G_{val}), but before the DAC. The offset applied is at the discretion of the user. Inappropriate values may cause arithmetic overflow in the subsequent operator sections. The result is given by the formula:

$$D_{out} = D_{in} + \left[\frac{N_{offset}}{2^{15}}\right]$$

Where:

D_{in} is the signal input,

D_{out} is the signal output,

N_{offset} is the 2s-complement value in the register.

Bit	Name	Active	State	Function
Address $0x44				
7:0	*TxIOffsetLSB*	Data	RW	Least significant 8 bits of the TxIOffset register (N_{offset}).
Address $0x45				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	*TxIOffsetMSB*	Data	RW	Most significant 4 bits of the TxIOffset register (N_{offset}).
Address $0x4A				
7:0	*TxQOffsetLSB*	Data	RW	Least significant 8 bits of the TxQOffset register (N_{offset}).
Address $0x4B				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	*TxQOffsetMSB*	Data	RW	Most significant 4 bits of the TxQOffset register (N_{offset}).

- **Address and Data format for TxIOffset access**

Address field [6:0]							Data field [11:0]											
1	0	0	0	1	0	0					D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	R	R	R	R	D11	D10	D9	D8				

- **Address and Data format for TxQOffset access**

Address field [6:0]							Data field [11:0]											
1	0	0	1	0	1	0					D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	1	R	R	R	R	D11	D10	D9	D8				

4.7.1.26 TxPhase

Title:	Transmit I and Q channel Phase correction register
Address:	\$0x40, \$0x41, \$0x46, \$0x47 (4 locations)
Function:	RW
Description:	This register controls the Tx Data path I and Q channel phase compensation. The phase may be adjusted by ±7.1° with respect to the input data signal phase. As each channel has separate phase adjustments the maximum differential phase compensation that can be achieved is ±14.2°. The phase adjustment value written to this register is a 2s-complement value (N_{phase}).

The amount of phase adjustment applied is given by the formula:

$$\phi = \tan^{-1}\left[\frac{N_{phase}}{2^{11}}\right]$$

Where:

ϕ is the phase adjustment,

N_{phase} is the value in the register and has a range of -256 to +255.

Note: Although each channel is separately adjustable with its own compensation value, the effect of phase adjustment is only detectable by measuring the phase angle between I and Q channels. It should be noted that the N_{phase} value has the effect of lagging the I channel for positive values of N_{phase} (conversely, leading the phase for negative values) and leading the Q channel for positive values of N_{phase} (conversely, lagging the phase for negative values). For example, putting the value 10 (decimal) into both TxIPhase and TxQPhase would produce a differential phase on I and Q of:

$$90^{\circ} - 2(\tan^{-1}(4.88\times10^{-3})) = 89.44^{\circ}$$

Bit	Name	Active	State	Function
Address \$0x40				
7:0	TxIPhaseLSB	Data	RW	Least significant 8 bits of the TxIPhase register (N_{phase}).
Address \$0x41				
7:1			RW	Reserved. Set these bits Low. Undefined on read.
0	TxIPhaseMSB	Data	RW	Most significant bit of the TxIPhase register (sign bit).
Address \$0x46				
7:0	TxQPhaseLSB	Data	RW	Least significant 8 bits of the TxQPhase register (N_{phase}).
Address \$0x47				
7:1			RW	Reserved. Set these bits Low. Undefined on read.
0	TxQPhaseMSB	Data	RW	Most significant bit of the TxQPhase register (sign bit).

- **Address and Data format for TxIPhase access**

Address field [6:0]		Data field [9:0]
1 0 0 0 0 0 0		D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 1	R R R R R R R D8	

- **Address and Data format for TxQPhase access**

Address field [6:0]		Data field [9:0]
1 0 0 0 1 1 0		D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 1 1 1	R R R R R R R D8	

4.7.1.27 TxDataAccess

Title: Tx Data path Access point.

Address: $0x50 to $0x53 (mapped over 4 locations)

Function: RW

Description: This register block allows direct access to the Tx Data path values just after the gain, phase and offset adjustment block. Both read and write operations are permitted. A read operation reads the signal values on the I and Q channels. A write operation will write data to the data path just before the 15-tap filter. To prevent normal Tx data overwriting this value the *TxDPAccessSel* bit in the **LoopBackCtrl** register should be set active. The MSB read data register is buffered to enable access to a discrete sample value (if this register was not buffered, data from different sample periods could be in the MSB and LSB registers). Therefore the LSB register must be read first for correct operation.

Bit	Name	Active	State	Function
Address $0x50				
7:0	*TxDPIDataLSB*	Data	RW	Least significant 8 bits of the TxDPIData register. This register must be read before its associated MSB register.
Address $0x51				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	*TxDPIDataMSB*	Data	RW	Most significant 2 bits of the TxDPIData register.
Address $0x52				
7:0	*TxDPQDataLSB*	Data	RW	Least significant 8 bits of the TxDPQData register. This register must be read before its associated MSB register.
Address $0x53				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	*TxDPQDataMSB*	Data	RW	Most significant 2 bits of the TxDPQData register.

- **Address and Data format for TxDPIData access**

Address field [6:0]	Data field [11:0]
1 0 1 0 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 0 0 0 1	R R R R D11 D10 D9 D8

- **Address and Data format for TxDPQData access**

Address field [6:0]	Data field [11:0]
1 0 1 0 0 1 0	D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 0 0 1 1	R R R R D11 D10 D9 D8

4.7.1.28 RxIQGainMult

Title: Receive I and Q channel Gain Multiplier register

Address: $0x30, $0x31, $0x34 and $0x35 (4 locations)

Function: RW

Description: A 2s-complement multiplication is performed on the magnitude of the Rx Data path signal and the result is then re-normalized to the system's dynamic range: thus the function may be considered as a digital attenuator. This multiplication is applied to the Rx signal after the ADC decimation filter, but before offset adjustment and the 63-tap and 49-tap FIR filters. This register sets the multiplier, the result being given by the formula:

$$D_{out} = D_{in}\left[\frac{G_{val}}{2^{15}}\right]$$

Where:

D_{in} is the signal input,

D_{out} is the signal output,

G_{val} is the value in the register.

Bit	Name	Active	State	Function
Address $0x30				
7:0	*RxIGainLSB*	Data	RW	Least significant 8 bits of the RxIGain register (G_{val}).
Address $0x31				
7:3			RW	Reserved. Set these bits Low. Undefined on read.
2:0	*RxIGainMSB*	Data	RW	Most significant 3 bits of the RxIGain register (G_{val}).
Address $0x34				
7:0	*RxQGainLSB*	Data	RW	Least significant 8 bits of the RxQGain register (G_{val}).
Address $0x35				
7:3			RW	Reserved. Set these bits Low. Undefined on read.
2:0	*RxQGainMSB*	Data	RW	Most significant 3 bits of the RxQGain register (G_{val}).

- **Address and Data format for RxIGain access**

Address field [6:0]	Data field [10:0]
0 1 1 0 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
0 1 1 0 0 0 1	R R R R R D10 D9 D8

- **Address and Data format for RxQGain access**

Address field [6:0]	Data field [10:0]
0 1 1 0 1 0 0	D7 D6 D5 D4 D3 D2 D1 D0
0 1 1 0 1 0 1	R R R R R D10 D9 D8

4.7.1.29 RxIQOffset

Title: Receive I and Q Channel Offset correction register

Address: $0x32, $0x33, $0x36, and $0x37 (4 locations)

Function: RW

Description: This register controls the Rx Data path signal offset. This offset is a 2s-complement value (N_{offset}), which is applied to the Rx signal after the Gain Multiplier (G_{val}), but before the 63-tap and 49-tap FIR filters. The offset applied is at the discretion of the user. Inappropriate values may cause arithmetic overflow in the subsequent operator sections. The result is given by the formula:

$$D_{out} = D_{in} + \left[\frac{N_{offset}}{2^{15}}\right]$$

Where:

D_{in} is the signal input,

D_{out} is the signal output,

N_{offset} is the 2s-complement value in the register.

Bit	Name	Active	State	Function
Address $0x32				
7:0	*RxIOffsetLSB*	Data	RW	Least significant 8 bits of the RxIOffset register (N_{offset}).
Address $0x33				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	RxIOffsetMSB	Data	RW	Most significant 4 bits of the RxIOffset register (N_{offset}).
Address $0x36				
7:0	RxQOffsetLSB	Data	RW	Least significant 8 bits of the RxQOffset register (N_{offset}).
Address $0x37				
7:4			RW	Reserved. Set these bits Low. Undefined on read.
3:0	RxQOffsetMSB	Data	RW	Most significant 4 bits of the RxQOffset register (N_{offset}).

- **Address and Data format for RxIOffset access**

Address field [6:0]							Data field [11:0]							
0	1	1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	1	1	R	R	R	R	D11	D10	D9	D8

- **Address and Data format for RxQOffset access**

Address field [6:0]							Data field [11:0]							
0	1	1	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	1	1	R	R	R	R	D11	D10	D9	D8

4.7.1.30 RxDataAccess

Title: Rx Data path Access point.

Address: $0x38 to $0x3B (mapped over 4 locations)

Function: RW

Description: This register block allows direct access to the Rx Data path values just after the 59-tap (Rx anti-alias) filter. Both read and write operations are permitted. A read operation reads the signal values on the I and Q channels. A write operation will write data to the Rx Data path operator output. To prevent normal Rx data overwriting this value the *RxDPAccessSel* bit in the **LoopBackCtrl** register should be set active. The MSB read data register is buffered to enable access of a discrete sample value (if this register was not buffered, data from different sample periods could be in the MSB and LSB registers). Therefore the LSB register must be read first for correct operation.

Bit	Name	Active	State	Function
Address $0x38				
7:0	*RxDPIDataLSB*	Data	RW	Least significant 8 bits of the RxDPIData register. This register must be read before its associated MSB register.
Address $0x39				
7:0	*RxDPIDataMSB*	Data	RW	Most significant 8 bits of the RxDPIData register.
Address $0x3A				
7:0	*RxDPQDataLSB*	Data	RW	Least significant 8 bits of the RxDPQData register. This register must be read before its associated MSB register.
Address $0x3B				
7:0	*RxDPQDataMSB*	Data	RW	Most significant 8 bits of the RxDPQData register.

- **Address and Data format for RxDPIData access**

Address field [6:0]							Data field [15:0]															
0	1	1	1	0	0	0									D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	1	D15	D14	D13	D12	D11	D10	D9	D8								

- **Address and Data format for RxDPQData access**

Address field [6:0]							Data field [15:0]															
0	1	1	1	0	1	0									D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	1	D15	D14	D13	D12	D11	D10	D9	D8								

4.7.1.31 BISTControl

Title: Built In Self Test Control register

Address: $0x62

Function: RW

Description: This register block allows control of BIST operations.

Bit	Name	Active	State	Function
7	*TestCompleteAck*	High/Low	RW	This bit is set by the user and cleared by the BIST controller when a BIST cycle has been completed.
6	*n_RampDelayEn*	Low	RW	Allow Ramp control signal delay. This delay is required for normal operations, by matching the FIR filter delays. For BIST operations, it can be disabled thus reducing BIST test time.
5	*BISTDataRateHi*	High	RW	Selects BIST data rate = 2.34 MHz Default rate (Low) = 1.44 kHz
4	*BISTEn*	High	RW	Enables BIST operations.
3	*ContinuousBIST*	High	RW	Selects continuous BIST mode. Default (Low) selects single cycle mode.
2	*EnRxDigitalFeedBack*	High	RW	Selects Rx digital loop feedback for 49-tap Tx FIR input data. Default (Low) selects normal Tx data.
1	*En49tIQData*	High	RW	Selects BIST data for 49-tap Tx FIR filter input. Default (Low) selects normal data.
0	*EnSymTestData*	High	RW	Selects BIST data for 79-tap FIR filter input. Default (Low) selects normal data.

- **Address and Data format for BistControl access**

Address field [6:0]						
1	1	0	0	0	1	0

Data field [7:0]							
D7	D6	D5	D4	D3	D2	D1	D0

4.7.1.32 BISTPRSG

Title:	Built In Self Test Pseudo Random Sequence Generator
Address:	$0x60 to $0x61 (2 locations)
Function:	RW
Description:	This register block allows control of BIST operations. This 16-bit number controls the length of the BIST data sequence. It is the initial value (or seed) written to the pseudo-random sequence generation logic. The length of the BIST data sequence is a function of the feedback logic equation and this initial value. The feedback function is fixed so run lengths are therefore controlled by this value. Which values to apply to give specific run lengths can be determined from a look-up table. This table may be provided on request.

Bit	Name	Active	State	Function
Address $0x60				
7:0	*BISTPRSGLSB*	Data	RW	Least significant 8 bits of the BISTPRSG register. This register must be read before its associated MSB register.
Address $0x61				
7:0	*BISTPRSGMSB*	Data	RW	Most significant 8 bits of the BISTPRSG register. This register must be read after its associated LSB register.

- **Address and Data format for BISTPRSG access**

Address field [6:0]							Data field [15:0]															
1	1	0	0	0	0	0									D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	1	D15	D14	D13	D12	D11	D10	D9	D8								

4.7.1.33 BISTCRCRegisters

Title: Built In Self Test Cyclic Redundancy Code checking Registers

Address: $0x64 to $0x6D (10 locations)

Function: RW

Description: This register block allows BIST CRC checksums to be read.

Bit	Name	Active	State	Function
Address $0x64				
7:0	*79tapI_CRCLSB*	Data	RW	Transmit I channel 79-tap filter LSB register.
Address $0x65				
7:0	*79tapI_CRCMSB*	Data	RW	Transmit I channel 79-tap filter MSB register.
Address $0x66				
7:0	*79tapQ_CRCLSB*	Data	RW	Transmit Q channel 79-tap filter LSB register.
Address $0x67				
7:0	*79tapQ_CRCMSB*	Data	RW	Transmit Q channel 79-tap filter MSB register
Address $0x68				
7:0	*SDM_CRCLSB*	Data	RW	Transmit SDM DAC LSB register.
Address $0x69				
7:0	*SDM_CRCMSB*	Data	RW	Transmit SDM DAC MSB register.
Address $0x6A				
7:0	*RXI_CRCLSB*	Data	RW	Receive I channel LSB register.
Address $0x6B				
7:0	*RXQ_CRCLSB*	Data	RW	Receive I channel MSB register.
Address $0x6C				
7:0	*RXQ_CRCLSB*	Data	RW	Receive Q channel LSB register.
Address $0x6D				
7:0	*RXQ_CRCMSB*	Data	RW	Receive Q channel MSB register.

- **Address and Data format for 79-tap I channel CRC req access**

Address field [6:0]							**Data field [15:0]**															
1	1	0	0	1	0	0									D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	1	0	1	D15	D14	D13	D12	D11	D10	D9	D8								

- **Address and Data format for 79-tap Q channel CRC req access**

Address field [6:0]							**Data field [15:0]**															
1	1	0	0	1	1	0									D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	1	1	1	D15	D14	D13	D12	D11	D10	D9	D8								

- **Address and Data format for SDM CRC req access**

Address field [6:0]	Data field [15:0]
1 1 0 1 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 1 0 0 1	D15 D14 D13 D12 D11 D10 D9 D8

- **Address and Data format for RX I Channel CRC req access**

Address field [6:0]	Data field [15:0]
1 1 0 1 0 1 0	D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 1 0 1 1	D15 D14 D13 D12 D11 D10 D9 D8

- **Address and Data format for RX Q Channel CRC req access**

Address field [6:0]	Data field [15:0]
1 1 0 1 1 0 0	D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 1 1 0 1	D15 D14 D13 D12 D11 D10 D9 D8

5 Application Notes

5.1.1 General

5.1.2 Transmitter

5.1.3 Receiver

5.1.4 Timing

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply			
V_{DD} - V_{SS}	-0.3	7.0	V
V_{CC1} - V_{SS1}	-0.3	7.0	V
V_{CC2} - V_{SS2}	-0.3	7.0	V
V_{CC3} - V_{SSB}	-0.3	7.0	V
V_{DD1} - V_{SSA}	-0.3	7.0	V
Voltage on any pin to			
V_{SS}	-0.3	V_{DD} + 0.3	V
V_{SS1}	-0.3	V_{CC1} + 0.3	V
V_{SS2}	-0.3	V_{CC2} + 0.3	V
V_{SSA}	-0.3	V_{DD1} + 0.3	V
V_{SSB}	-0.3	V_{CC3} + 0.3	V
Current into or out of V_{DD}, V_{CC1}, V_{CC2}, V_{CC3}, V_{DD1}, V_{SS}, V_{SS1}, V_{SS2}, V_{SSB}, V_{SSA}	-30	30	mA
Current into or out of any other pin	-20	20	mA
Voltage differential between power supplies			
(V_{DD}, V_{CC1}, V_{CC2}, V_{CC3} and V_{DD1})	0	0.3	V
(V_{SS}, V_{SS1}, V_{SS2}, V_{SSB} and V_{SSA})	0	50	mV
LH Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply				
V_{DD} - V_{SS}		4.5	5.5	V
V_{CC1} - V_{SS1}		4.5	5.5	V
V_{CC2} - V_{SS2}		4.5	5.5	V
V_{CC3} - V_{SSB}		4.5	5.5	V
V_{DD1} - V_{SSA}		4.5	5.5	V
Operating Temperature		-40	85	°C
MCLK Frequency		TBD	TBD	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

MCLK Frequency = 9.216MHz, Symbol Rate = 18k bits/sec,
$(V_{DD} - V_{SS}) = (V_{CC1} - V_{SS1}) = (V_{CC2} - V_{SS2}) = (V_{CC3} - V_{SSB}) = (V_{DD1} - V_{SSA})$ = 3.0V to 3.6V for 3.3V parameters; 4.5V to 5.5V, for 5.0V parameters. T_{AMB} = - 40°C to +85°C.

At 5V *Bias/Ctrl* = 0 and at 3.3V *Bias/Ctrl* = 1 in **PowerDownCtrl** register will optimize the analog performance in the Tx and Rx sections.

It is assumed that all powersave and clock stop bits are set, where appropriate.

	Notes	Min.	Typ.	Max.	Units
5V DC Parameters (MCLK not toggled)					
I_{DD} (Tx powersaved)	1		20		mA
I_{DD} (Rx powersaved)	1		20		mA
I_{DD} (Aux powersaved)	1		34		mA
I_{DD} (All powersaved)	1			50	µA
I_{DD} (Not powersaved)	1		36		mA
5V AC Parameters (MCLK at 9.216MHz)					
I_{DD} (Tx powersaved)	1		40		mA
I_{DD} (Rx powersaved)	1		35		mA
I_{DD} (Aux powersaved)	1		62		mA
I_{DD} (All powersaved)	1		12		mA
I_{DD} (Not powersaved)	1		64		mA
3.3V DC Parameters (MCLK not toggled)					
I_{DD} (Tx powersaved)	1		18		mA
I_{DD} (Rx powersaved)	1		18		mA
I_{DD} (Aux powersaved)	1		31		mA
I_{DD} (All powersaved)	1			50	µA
I_{DD} (Not powersaved)	1		32		mA
3.3V AC Parameters (MCLK at 9.216MHz)					
I_{DD} (Tx powersaved)	1		31		mA
I_{DD} (Rx powersaved)	1		33		mA
I_{DD} (Aux powersaved)	1		48		mA
I_{DD} (All powersaved)	1		7.5		mA
I_{DD} (Not powersaved)	1		49		mA
MCLK Input					
'High' pulse width	2	40			ns
'Low' pulse width	2	40			ns
Input impedance (at 100Hz)		10			MΩ

Table 6: Operating Characteristics

Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. Timing for an external input to the MCLK pin.

6.1.3.1 Transmit Parameters

All parameters refer to the entire Tx baseband I and Q channels, unless otherwise indicated.

Parameter	Notes	Min	Typ	Max	Units
Input bit rate	1		36		kbps
No. of channels (I and Q)			2		
Default Modulation type			π/4 DQPSK		
Default RRC Characteristics					
Roll-off coefficient (a)			0.35		
|H(f)| 0 - 5.85kHz	2	-0.3	0	0.3	dB
|H(f)| @ 9kHz	2	-3.3	-3	-2.7	dB
|H(f)| @ 10.05kHz	2	-7.0	-6	-5.0	dB
|H(f)| @ 12.15kHz	2			-30	dB
Max spurii relative to maximum passband signal level					
@ 16kHz			-60		dBc
@ 25kHz			-68		dBc
@ 50kHz			-78		dBc
@ 75kHz			-80		dBc
FIR filter sampling rate			144		kHz
DAC					
Output update rate			2.304		MHz
Resolution			12		Bits
Integral accuracy				±0.5	LSB
Differential accuracy				±0.25	LSB
Offset without adjustment	6			25	mV
Gain matching, without adjustment, I to Q	5	-0.3		0.3	dB
Gain matching, normalized, 0 - 9kHz, (I or Q) to ideal Tx	5	-0.3		0.3	dB
Phase matching, after adjustment, 0 - 9kHz, I to Q		-0.5		0.5	Degrees
Storage time				18	Symbols
Active Power					
3.3V, Rx, aux. powered down				105	mW
Vector Error					
RMS	3		0.017	0.025	
PEAK	3		0.045	0.07	
I,Q output level					
V_{CC} = 5.0V	4		2.5		V_{P-P}
V_{CC} = 3.3V	4		1.65		V_{P-P}

Table 7: Transmit Parameters

Notes:

1. 2 bits/symbol.
2. Reference 1V_{P-P}.
3. Vector errors measured with ideal IF and RF sections after gain and offset adjustment, and specified as a fraction of the nominal vector value.
4. Peak to peak, differential at maximum gain.
5. A gain multiplier function allows independent proportional control of each channel. The multiplier is a 12-bit word for each channel, input via the serial interface, representing a value from 0 to 1. This multiplication is applied to the signals from the FIR filters.
6. Offset adjustment for each channel is available by loading a 12-bit word into the transmit offset register via the serial interface.

6.1.3.2 Receive Parameters

Offset adjustment for each channel is available by loading a 16-bit word into the receive offset register via the serial interface.

Optimally, anti-alias filtering should be carried out as much as possible prior to any AGC function before the receive inputs. This allows the AGC to act on a reduced bandwidth signal and thereby improve the relative magnitude of the wanted part. The device has been designed to reduce the complexity of any external anti-alias filter as much as possible and a 4-pole Butterworth with a -3dB point at about 60kHz should be adequate. The internal anti-alias filter, if used, cannot provide the required 120dB attenuation at 2.3MHz and must be supplemented by external filtering. The most simple supplementary system may be a one or two-pole filter before the AGC and an RC network after the AGC with a -3dB point on each filter of about 200kHz.

Parameter	Notes	Min	Typ	Max	Units
Input impedance					
Resistive		100			kΩ
Capacitive load to V_{SS1} or V_{SS2}	1			10	pF
Differential Input voltage range					
V_{CC}=5.0V	2		2.8		V_{P-P}
V_{CC}=3.3V	3		1.8		V_{P-P}
3rd order intercept			TBD		
Anti -alias attenuation requirements					
With internal anti-alias filter disabled					
@ 130kHz (Reference maximum input level)		30			dB
@ 2.3MHz (Reference maximum input level)		120			dB
With internal anti-alias filter enabled					
@ 130kHz (Reference maximum input level)		10			dB
@ 2.3MHz (Reference maximum input level)		50			dB
ADC					
Sampling rate			2.304		MHz
Resolution			16		Bits
Integral accuracy				±1	LSB
Differential accuracy				±1	LSB
Default RRC Characteristics					
Roll-off coefficient (a)			0.35		
$\lvert H(f)\rvert$ 0 - 5.85kHz	4	-0.2	0	0.2	dB
$\lvert H(f)\rvert$ @ 9kHz	4	-3.2	-3	-2.8	dB
$\lvert H(f)\rvert$ @ 10.05kHz	4	-7.0	-6	-5.0	dB
$\lvert H(f)\rvert$ @ 12.15kHz	4			-30	dB
$\lvert H(f)\rvert$ @ 16kHz	4			-70	dB
$\lvert H(f)\rvert$ @ 25kHz	4			-70	dB
$\lvert H(f)\rvert$ @ 50kHz	4			-80	dB
$\lvert H(f)\rvert$ @ 75kHz	4			-90	dB
FIR filter sampling rate					
Decimation sections			2.304		MHz
RRC sections			144		kHz
Output Word Rate (16 bit words per channel) - selectable	5	72		144	kHz
Offset without adjustment				10	mV
Gain matching without adjustment, 0 -10kHz, I to Q		-0.1		0.1	dB
Phase matching, 0 - 10kHz, I to Q		-0.5		0.5	Degrees

Parameter	Notes	Min	Typ	Max	Units
Storage time				15	Symbols
Active Power					
3.3V power supply				100	mW

Table 8: Receive Parameters

Notes:

1. Source should be < 1000 Ω.
2. This means ±0.7V on each input of the differential pair.
3. This means ±0.45V on each input of the differential pair.
4. Reference 1V_{P-P}.
5. Output via the serial interface at 4.608 MHz or 2.304MHz.

6.1.3.3 Auxiliary Circuit Parameters

Parameter	Notes	Min	Typ	Max	Units
DACs					
Resolution			10		Bits
Settling time to 0.5 LSB	1			10	µSec
Output resistance				250	Ω
Integral non-linearity				4	Bits
Differential non-linearity (guaranteed monotonic)				1	Bits
Zero error (offset)		-20		20	mV
Power (all DACs operating)				10	mW
Resistive Load requirement		5			kΩ
RMS output noise voltage in 30kHz bandwidth			10		µV
ADC and Multiplexed inputs					
Input source impedance requirement	2			25	kΩ
Resolution			10		Bits
Input signal "linear rate of change" for < 1 bit error				0.27	mV/µs
Conversion time			12		µSec
Integral non-linearity (no missing codes)				2	Bits
Differential non-linearity				1	Bits
Zero error (offset)		-20		20	mV
ADC Clock frequency			MCLK/8		
Input capacitance				5	pF
Power				3	mW

Table 9: Auxiliary Circuit Parameters

Notes:

1. Worst case large signal transition.
2. For less than 1 bit error.

6.1.3.4 Timing Diagrams

The following timings are provisional:

6.1.3.4.1 Serial Ports

Timing Parameter	Marker	Min	Max	Units
MCLK to SClk out - low to high	t_{CSLH}	15	50	ns
MCLK to SClk out - high to low	t_{CSHL}	10	35	ns
CmdDat set-up to falling edge of SClk	T_{SIS}	35		ns
CmdFS set-up to falling edge of SClk	T_{SIS}	35		ns
CmdDat hold from fall edge of SClk	T_{SIH}		0	ns
CmdFS hold from fall edge of SClk	T_{SIH}		0	ns
RxDat propagation from rising edge of SClk	T_{SOP}		5	ns
RxFS propagation from rising edge of SClk	T_{SOP}		5	ns
CmdRdDat propagation from rising edge of SClk	T_{SOP}		5	ns
CmdRdFS propagation from rising edge of SClk	T_{SOP}		5	ns
RxDat hold from rising edge of SClk	T_{SOH}	-5		ns
RxFS hold from rising edge of SClk	T_{SOH}	-5		ns
CmdRdDat hold from rising edge of SClk	T_{SOH}	-5		ns
CmdRdFS hold from rising edge of SClk	T_{SOH}	-5		ns
**Cmd port in Bi-dir mode **				
CmdDat propagation from rising edge of SClk	T_{SOP}		7	ns
CmdDat hold from rising edge of SClk	T_{SOH}	-7		ns

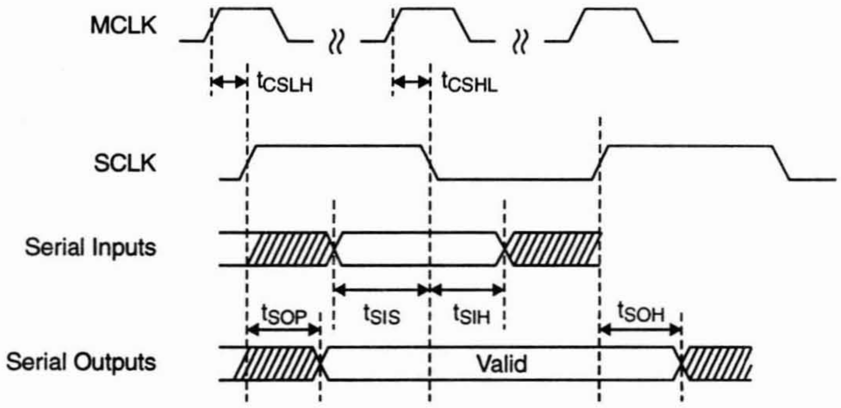

MCLK
t_{CSLH}
t_{CSHL}
SCLK
Serial Inputs
t_{SOP}
t_{SIS}
t_{SIH}
t_{SOH}
Serial Outputs
Valid

Figure 5: Serial Port Interfaces - Timing Parameters

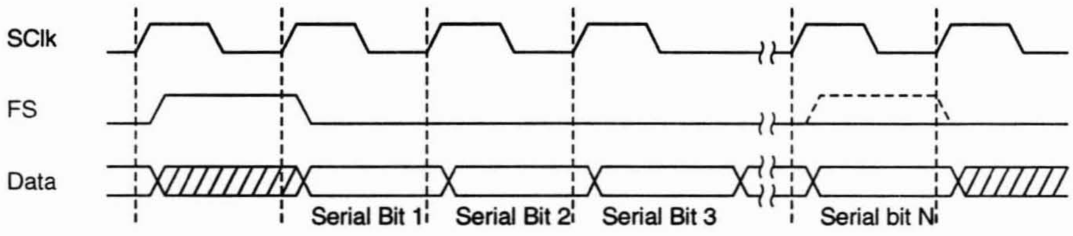

SClk
FS
Data
Serial Bit 1
Serial Bit 2
Serial Bit 3
Serial bit N

Figure 6: Basic Serial Port Signals

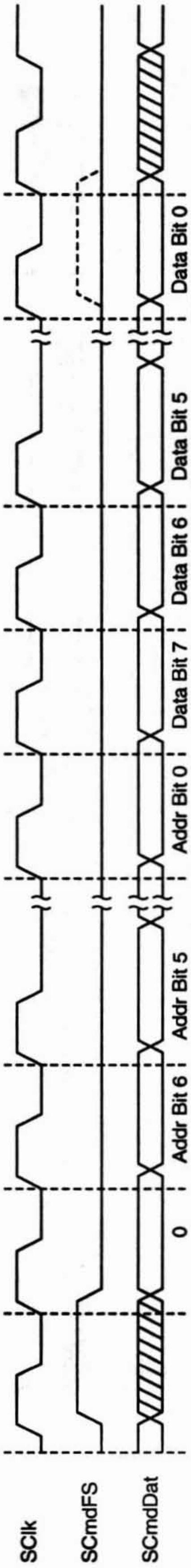

SClk
SCmdFS
SCmdDat
0
Addr Bit 6
Addr Bit 5
Addr Bit 0
Data Bit 7
Data Bit 6
Data Bit 5
Data Bit 0

Figure 7: Command Write Operation

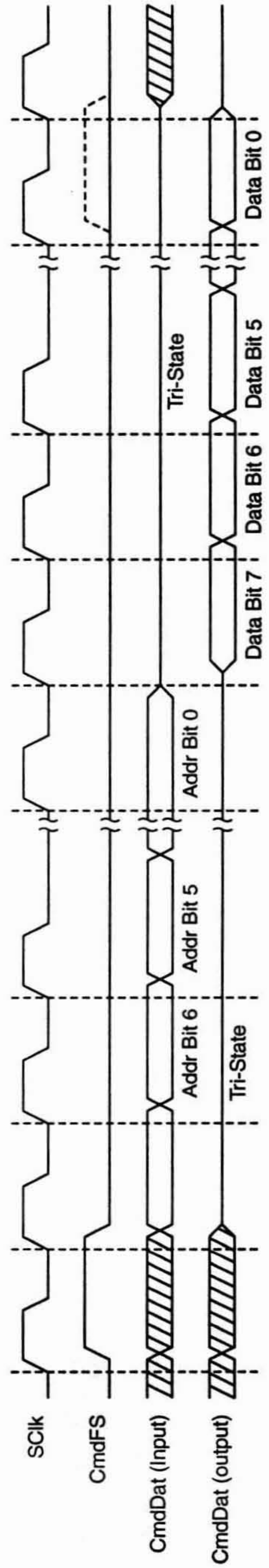

SClk
CmdFS
CmdDat (Input)
CmdDat (output)
Addr Bit 6
Addr Bit 5
Addr Bit 0
Tri-State
Data Bit 7
Data Bit 6
Data Bit 5
Data Bit 0
Tri-State

Figure 8: Bi-Directional Command Read Operation

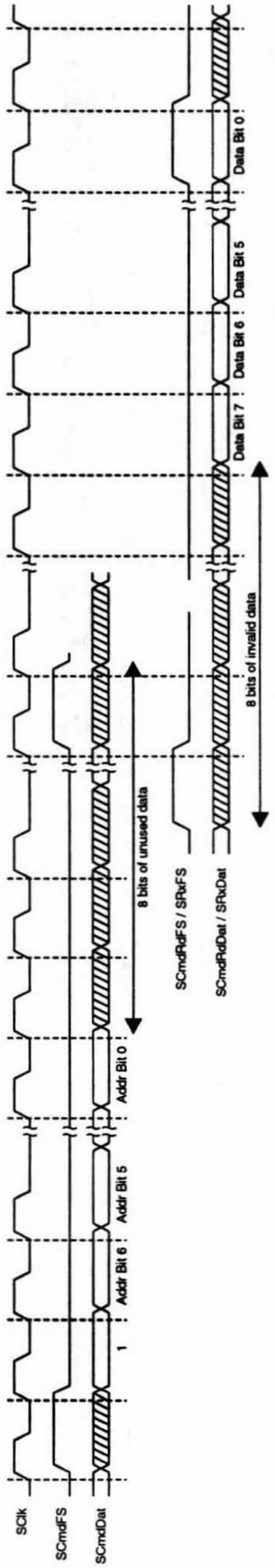

SClk
SCmdFS
SCmdDat
1
Addr Bit 6
Addr Bit 5
Addr Bit 0
8 bits of unused data
SCmdRdFS / SRxFS
SCmdRdDat / SRxDat
8 bits of invalid data
Data Bit 7
Data Bit 6
Data Bit 5
Data Bit 0

Figure 9: Non Bi-Directional Command Read Operation

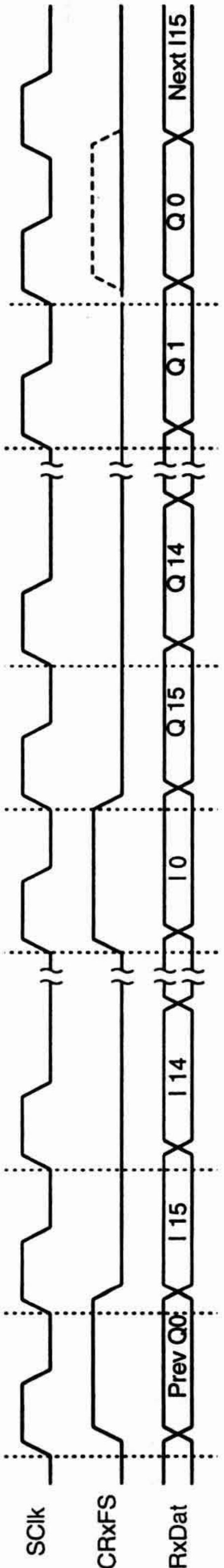
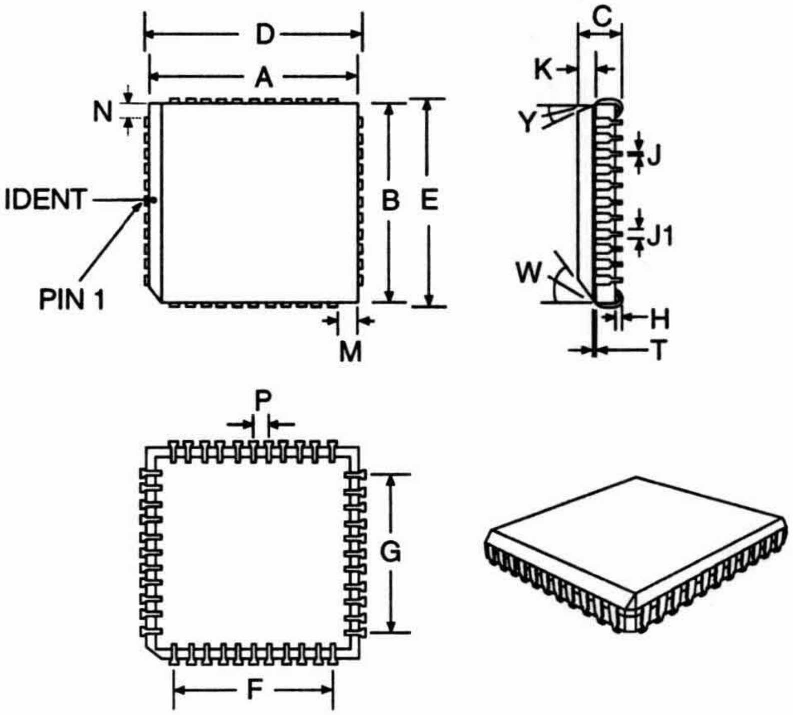

SClk
SCRxFS
SRxDat
Prev Q0
I 15
I 14
I 0
Q 15
Q 14
Q 1
Q 0
Next I15

Figure 10: Rx Data Serial Port Read Operation

6.2 Packaging

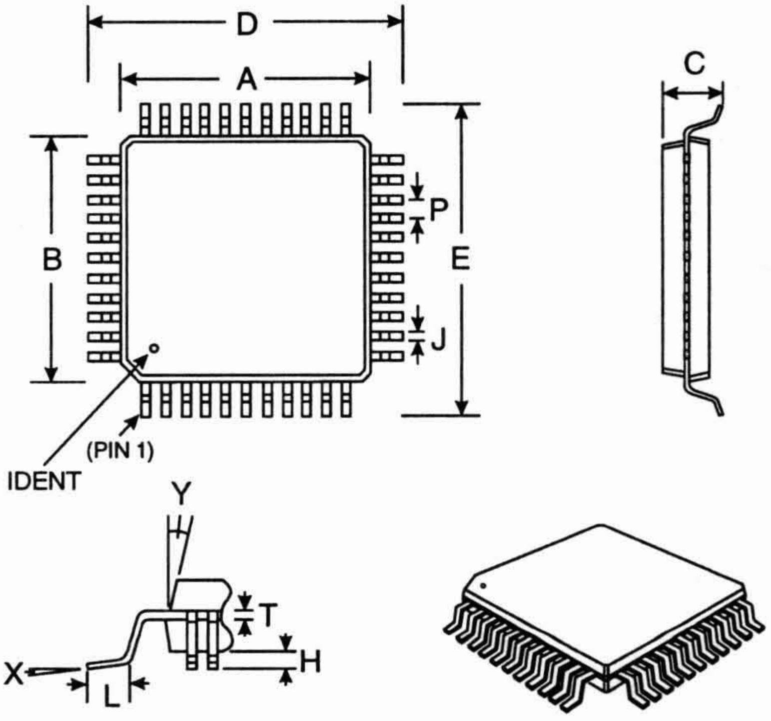


DIM.	MIN.	TYP.	MAX.
A	0.650 (16.51)		0.656 (16.66)
B	0.650 (16.51)		0.656 (16.66)
C			0.180 (4.57)
D	0.685 (17.40)		0.695 (17.65)
E	0.685 (17.40)		0.695 (17.65)
F		0.500 (12.7)	
G		0.500 (12.7)	
H	0.020 (0.51)		
J	0.013 (0.33)		0.021 (0.53)
J1		0.029 (0.74)	
K		0.070 (1.78)	
M		0.062 (1.57)	
N		0.062 (1.57)	
P		0.050 (1.27)	
T		0.010 (0.25)	
W		0.30 (7.62) x 45°	
Y		7°	

NOTE : All dimensions in inches (mm.)

Angles in degrees

Figure 11: 44-pin PLCC Mechanical Outline: ***Order as part no. MX980L6***



DIM.	MIN.	TYP.	MAX.
A	0.390 (9.90)		0.398 (10.11)
B	0.390 (9.90)		0.398 (10.11)
C	0.055 (1.40)		0.063 (1.60)
D	0.465 (11.80)		0.480 (12.20)
E	0.465 (11.80)		0.480 (12.20)
H	0.002 (0.04)		0.006 (0.16)
J	0.009 (0.24)		0.018 (0.45)
L	0.016 (0.40)		0.030 (0.75)
P		0.031 (0.80)	
T	0.004 (0.09)		0.008 (0.20)
W	0°		7°
Y	10°		14°

NOTE : All dimensions in inches (mm.)

Angles in degrees

Figure 12: 44-pin QFP Mechanical Outline: ***Order as part no. MX980L7***

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APPLICATION NOTE

GMSK **Practical GMSK Data Transmission**

Practical GMSK Data Transmission

Introduction

The proliferation of computers in today's society has increased the demand for transmission of data over wireless links. Binary data, composed of sharp "one to zero" and "zero to one" transitions, results in a spectrum rich in harmonic content that is not well suited to RF transmission. Hence, the field of digital modulation has been flourishing. Recent standards such as Cellular Digital Packet Data (CDPD) and Mobitex* specify Gaussian filtered Minimum Shift Keying (GMSK) for their modulation method.

GMSK is a simple yet effective approach to digital modulation for wireless data transmission. To provide a good understanding of GMSK, we will review the basics of MSK and GMSK, as well as how GMSK is implemented in CDPD and Mobitex systems.

GMSK modems reduce system complexity, and in turn lower system cost. There are, however, some important implementation details to be considered. This paper will cover some of these details, focusing on interfacing a single chip baseband modem to the IF/RF section of a "typical" FM radio topology.

Background

If we look at a Fourier series expansion of a data signal we see harmonics extending to infinity. When these harmonics are summed, they give the data signal its sharp transitions. Hence, an unfiltered NRZ data stream used to modulate an RF carrier will produce an RF spectrum of considerable bandwidth. Of course, the FCC has strict regulations about spectrum usage and such a system is generally considered impractical. But if we start to remove the high frequency harmonics from the Fourier series (i.e. pass the data signal through a lowpass filter), the transitions in the data will become progressively less sharp. This suggests that pre-modulation filtering is an effective method for reducing the occupied spectrum for wireless data transmission. In addition to a compact spectrum, a wireless data modulation scheme must have good bit error rate (BER) performance under noisy conditions. Its performance should also be independent of power amplifier linearity to allow the use of class C power amplifiers.

The academic field of "Data Transmission" is loaded with modulation strategies that attempt to meet the above criteria. Most involve translation of data bits or patterns into a particular combination of phase, frequency or amplitude. Some of the more notable techniques are listed in Table 1.

MODULATION TECHNIQUE	COMMON ACRONYM
Frequency Shift Keying	FSK
Multi-level Frequency Shift Keying	MFSK
Continuous Phase Frequency Shift Keying	CPFSK
Minimum Shift Keying	MSK
Gaussian Minimum Shift Keying	GMSK
Tamed Frequency Modulation	TFM
Phase Shift Keying	PSK
Quadrature Phase Shift Keying	QPSK
Differential Quadrature Phase Shift Keying	DQPSK
Pi/4 Differential Quadrature Phase Shift Keying	Pi/4 DQPSK
Quadrature Amplitude Modulation	QAM

Table 1: Modulation Formats

** Mobitex is a trademark owned by the Telia Corporation.*

Each of the modulation formats listed in Table 1 is suited to specific applications. In general, schemes that rely on more than two levels (e.g. QAM, QPSK) require better signal to noise ratios (SNR) than two-level schemes for similar BER performance. Additionally, in a wireless environment, multi-level schemes generally require greater power amplifier linearity than two-level schemes. The fact that GMSK uses a two-level continuous phase modulation (CPM) format has contributed to its popularity. Another point in its favor is that it allows the use of class C power amplifiers (relatively non-linear) and data rates approaching the channel BW (dependent on filter bandwidth and channel spacing).

GMSK Basics

Prior to discussing GMSK in detail we need to review MSK, from which GMSK is derived. MSK is a continuous phase modulation scheme where the modulated carrier contains no phase discontinuities and frequency changes occur at the carrier zero crossings. MSK is unique due to the relationship between the frequency of a logical zero and one: the difference between the frequency of a logical zero and a logical one is always equal to half the data rate. In other words, the modulation index is 0.5 for MSK, and is defined as

$$m = \Delta f \times T$$

where,

$$\Delta f = |f_{logic\ 1} - f_{logic\ 0}|$$

$$T = 1/\text{bit rate}$$

For example, a 1200 bit per second baseband MSK data signal could be composed of 1200 Hz and 1800 Hz frequencies for a logical one and zero respectively (see Figure 1).

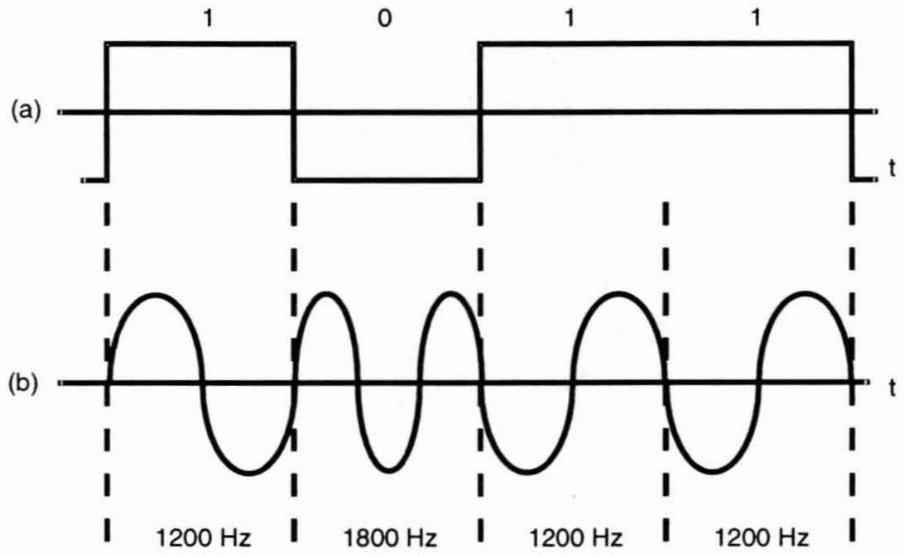


Figure 1: 1200 baud MSK data signal; a) NRZ data, b) MSK signal.

Baseband MSK, as shown in Figure 1, is a robust means of transmitting data in wireless systems where the data rate is relatvely low compared to the channel BW. MX-COM devices such as the MX429 and MX469 are single chip solutions for baseband MSK systems, incorporating modulation and demodulation circuitry on a single chip.

An alternative method for generating MSK modulation can be realized by directly injecting NRZ data into a frequency modulator with its modulation index set for 0.5 (see Figure 2). This approach is essentially equivalent to baseband MSK. However, in the direct approach the VCO is part of the RF/IF section, whereas in baseband MSK the voltage to frequency conversion takes place at baseband.

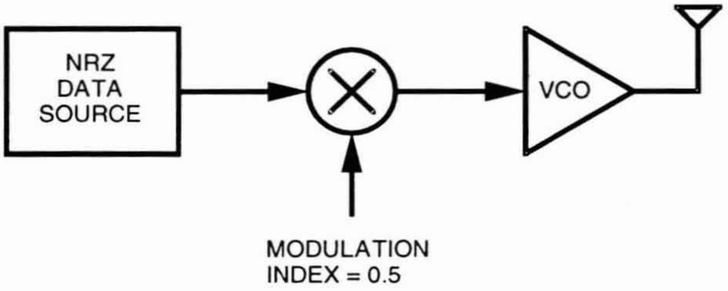


Figure 2: Direct MSK modulation

The fundamental problem with MSK is that the spectrum is not compact enough to realize data rates approaching the RF channel BW. A plot of the spectrum for MSK reveals sidelobes extending well above the data rate (see Figure 4). For wireless data transmission systems which require more efficient use of the RF channel BW, it is necessary to reduce the energy of the MSK upper sidelobes. Earlier we stated that a straightforward means of reducing this energy is lowpass filtering the data stream prior to presenting it to the modulator (pre-modulation filtering). The pre-modulation lowpass filter must have a narrow BW with a sharp cutoff frequency and very little overshoot in its impulse response. This is where the Gaussian filter characteristic comes in. It has an impulse response characterized by a classical Gaussian distribution (bell shaped curve), as shown in Figure 3. Notice the absence of overshoot or ringing.

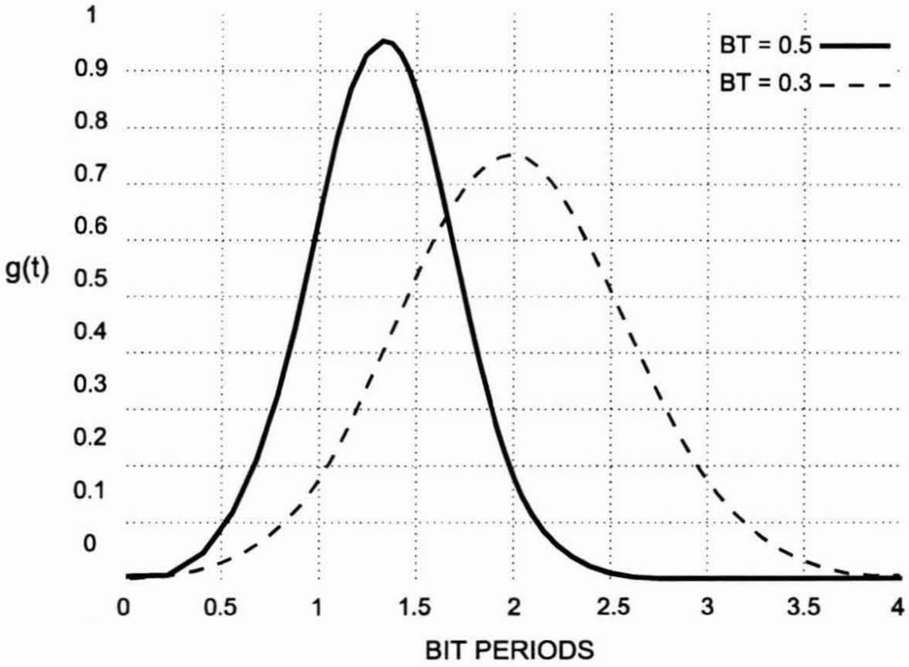


Figure 3: Gausssian filter impluse response for BT = 0.3 and BT = 0.5

Figure 3 depicts the impulse response of a Gaussian filter for BT = 0.3 and 0.5. BT is related to the filter's -3dB BW and data rate by

$$BT = \frac{f_{-3dB}}{\text{BIT RATE}}$$

Hence, for a data rate of 9.6 kbps and a BT of 0.3, the filter's -3dB cutoff frequency is 2880Hz.

Still referring to Figure 3, notice that a bit is spread over approximately 3 bit periods for BT=0.3 and two bit periods for BT=0.5. This gives rise to a phenomena called inter-symbol interference (ISI). For BT=0.3 adjacent symbols or bits will interfere with each other more than for BT=0.5. GMSK with BT=∞ is equivalent to MSK. In other words, MSK does not intentionally introduce ISI. Greater ISI allows the spectrum to be more compact, making demodulation more difficult. Hence, spectral compactness is the primary trade-off in going from MSK to Gaussian pre-modulation filtered MSK. Figure 4 displays the normalized spectral densities for MSK and GMSK. Notice the reduced sidelobe energy for GMSK. Utlimately, this means channel spacing can be tighter for GMSK when compared to MSK for the same adjacent channel interference.

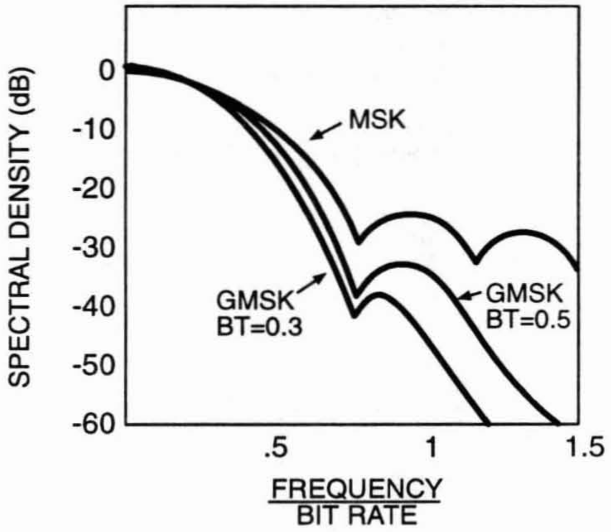


Figure 4: Spectral density for MSK and GMSK

Performance Measurements

The performance of a GMSK modem is generally quantified by measurement of the signal-to-noise ratio (SNR) versus BER. SNR is related to E_b/N_0 by

$$\frac{E_b}{N_0} = \frac{S}{RN_0} = \frac{S}{N}\left(\frac{B_n}{R}\right)$$

where,
S = signal power
R = data rate in bits per second
N_0 = noise power spectral density (watts/Hz)
E_b = energy per bit
$B_n \times N_0 = N$ = noise power
B_n = noise BW of IF filter

Recent Standards

GMSK has been adopted by many wireless data communication protocols. Two of the systems specifying GMSK modulation are Cellular Digital Packet Data (CDPD) and Mobitex.

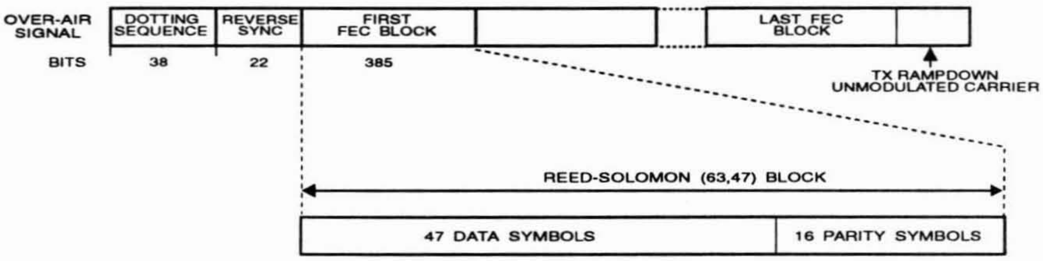
CDPD uses the dead air time on cellular systems by sending data packets on idle cellular voice channels. Data is transmitted at 19.2kbps using a BT of 0.5. This high data rate is facilitated by the 30kHz channel spacing of the cellular network and the spectral conservation of GMSK. Voice has priority over data and will interrupt data transmission, forcing the CDPD system to seek a new idle cellular channel. This could prove to be an obstacle to the throughput promised by its 19.2kbps data rate when implemented in a highly congested area where dead time is limited.

CDPD is being added to the existing cellular infrastructure and therefore promises to offer widespread coverage. The coverage and ease of adaptation appear to be the greatest strengths of the CDPD system. The slower-than-expected deployment of CDPD has many people anxious and perhaps a bit nervous about its potential.

Competition from dedicated data systems such as Mobitex is not insignificant. While Mobitex has a lower data rate than CDPD (8kbps), it is not sharing its channels with cellular voice transmissions. Several subtleties such as this will make it more difficult for end users to select the system best suited to their needs by obscuring the actual throughput potential of the systems. Mobitex's choice of 8kbps and a BT of 0.3 afford it a much tighter channel spacing (12.5kHz) than CDPD, but the greater inter-symbol interference for BT=0.3 limits the system's tolerance to noise and distortion. The narrower channel also limits Mobitex's tolerance to frequency offsets between units.

Both CDPD and Mobitex employ forward error correction in their packetting of data. Figure 5 shows the typical packet structures of these two systems for comparison. Forward error correction (FEC) helps improve the systems' throughput when less than ideal channel conditions exist.

CDPD Reverse Channel Frame Transmission Structure



Mobitex Frame Structure

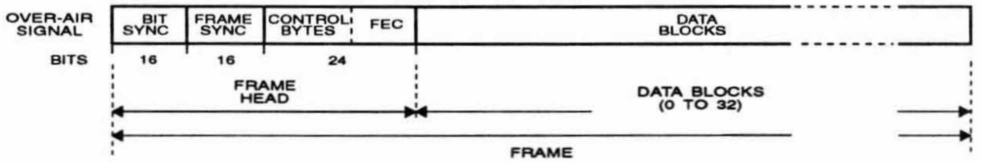


Figure 5: Typical packet structures for CDPD and Mobitex

Implementation Considerations

The design of a GMSK modulator/demodulator appears to be a straightforward task. Most textbooks present the modulator as a "simple" Gaussian filter cascaded with a VCO. However, in practice it is generally not that simple. Many of the sections in a typical radio such as the synthesizer, IF filter, power amplfier, etc. have far from ideal behavior. In particular, the synthesizer presents a unique problem for GMSK modulation. Data patterns consisting of several consectutive ones or zeros have a spectral response extending down to near DC. Most frequency synthesizers will not respond to this low frequency signal (a typical synthesizer effectively has a highpass filter characteristic).Two of the most common modulation methods, which help considerably where the non-ideal behavior of the synthesizer is concerned, are "Two-point modulation" and "Quadrature modulation."

Two point modulation

Two point modulation (see Figure 5) circumvents this synthesizer problem by splitting the Gaussian filtered signal; one portion is directed to the VCO modulation input, the other portion is used to modulate the TCXO. The TCXO is not in the frequency control feedback loop. Hence, the TCXO can be modulated by the low frequency portion of the signal, and its output is effectively summed with the signal modulating the VCO in the synthesizer. The composite signal has a spectral response extending down to DC.

frequency portion of the signal, and its output is effectively summed with the signal modulating the VCO in the synthesizer. The composite signal has a spectral response extending down to DC.

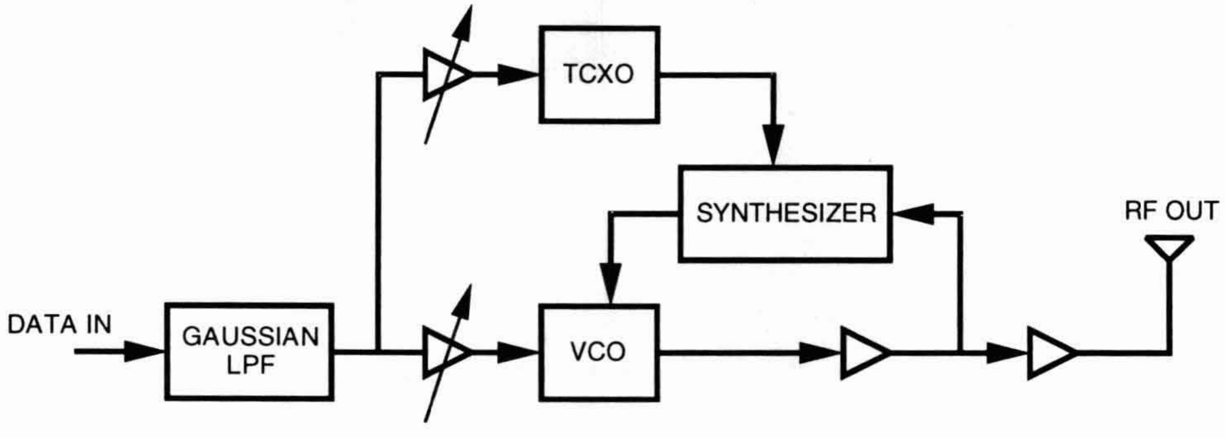


Figure 6: Two point modulation radio block diagram

I and Q modulation

Quadrature (I and Q) modulation can also be effective in eliminating synthesizer shortcomings. In I and Q modulation, the Gaussian filtered data signal is separated into in-phase (I) and quadrature phase (Q) components. The modulated RF signal is created by mixing the I and Q components up to the frequency of the RF carrier, where they are summed together. The role of the synthesizer has now been reduced to merely changing carrier frequency for channel selection. The key to optimum performance with quadrature modulation is accurate creation of the I and Q components.

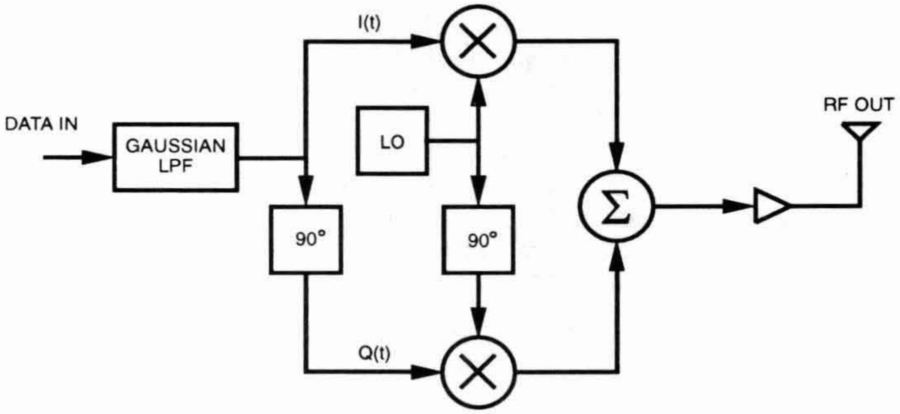


Figure 7: I and Q radio block diagram

Baseband I and Q signals can be created by using an all-pass phase shifting network. This network must maintain a 90 degree phase relationship between the I and Q signals for all frequencies in the band of interest.

Demodulation

Demodulation of the GMSK signal requires as much attention to the preservation of an unadulterated wave form as does modulation of the signal. The choice of a Gaussian shaped pre-modulation filter was made for three main reasons[1]:

1) narrow bandwidth and sharp cutoff
2) lower overshoot impulse response
3) preservation of the filter output pulse area.

The first condition gives GMSK modulation its spectral efficiency. It also improves its noise immunity when demodulating. The second condition affords GMSK low phase distortion. This is a major concern when the and not realizable with a physical Gaussian filter, the phase response can be kept linear and therefore sufficient for coherent demodulation.

In most systems the constraints on the above goals also include

- Data Rate
- Tx filter bandwidth (BT)
- Channel Spacing
- Allowable adjacent channel interference
- Peak carrier deviation
- Tx and Rx carrier frequency accuracy
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics.

These constraints are all part of the balance that must be struck to provide a robust GMSK system. The data rate, Tx BT, peak carrier deviation, and carrier frequency accuracy between receiver and transmitter all contribute to the necessary width of the IF filter. The IF filter should have sufficient width to accommodate the maximum variations in the above parameters so that the received signal will not run into the skirts of the filter. The skirts of the IF filter can introduce excessive amounts of group delay (phase distortion) in the higher frequency components of the received data. The passband of the IF filter should have little or no group delay. The more group delay introduced, the more degraded the bit error rate (BER) performance of the receiver will become. Rules of thumb for group delay dictate less than 10% of a bit time is tolerable. How happy you are with this level of performance is very dependent on the other factors that influence the BER of your system: BT, signal strength, fading, etc. Phase equalization measures can also be taken to help reduce group delay, but if there is control over the IF filter's design these steps can be avoided.

The CDPD and Mobitex standards mentioned earlier are addressed by two devices manufactured by MX-COM: the MX589 and the MX909. Both devices are designed to interface to the transmitter and receiver of a system at baseband. The MX589 is a versatile device capable of operating at data rates from 4kbps-40kbps and at BT's of 0.5 or 0.3. The device is implemented in a CMOS process that allows it to operate at low supply voltages (3.0-5.0 volts) and draw little current (1.5mA @ 3.0V). The digital data interface is a synchronous serial bit stream for both receive and transmit.

The MX909, also fabricated in a CMOS process, is specifically intended for Mobitex type systems, and has a corresponding BT of 0.3. Its data rate can be varied from 4kbps-19.2kbps, but should be set to 8kbps to achieve Mobitex compatibility. It can be operated from a supply voltage of 4.5-5.5 volts and typically draws 3.0mA. The data interface is a parallel microprocessor I/O compatible bus, and the MX909 contains all the circuitry needed to implement the forward error correction encoding and decoding of the Mobitex format.

The demodulation of the baseband GMSK signal presented to these devices is accomplished using a Gaussian shaped lowpass filter, clock extraction and reference level compensation circuitry in concert with data extraction circuitry. The signal first goes through a Gaussian lowpass filter similar to that used by the transmit section. The signal's zero crossing reference and clock timing are then extracted using peak detection circuitry and a phase lock loop in coordination. This cooperative effort helps improve both section's immunity to noise. Once "lock" has been achieved accurate demodulation of data from the data extraction circuitry can be expected.

The peak detection circuitry can adjust to large changes in DC level of the signal within 1.5 bit periods. This "clamping" mode is used when the carrier is first detected by the receiver. The PLL has a wideband acquire mode that can lock onto a signal in less than 8 zero crossings. Using these two modes allows the devices to start decoding data very shortly after the receiver senses carrier. Both the phase lock loop and the peak tracking circuitry have less aggressive modes that afford better noise immunity once the initial acquire modes have obtained lock. The nature of the GMSK signal at baseband requires good response of the system near DC as mentioned in the section on modulation. A more random data pattern does not have as large a DC component and is less sensitive to the highpass characteristics of any AC coupling that might need to be used to interface the baseband signal to the GMSK modulator or demodulator. The bit error rate (BER) performance of the MX589 is shown in Figure 8. The figure shows the effect of various highpass characteristics on the BER profile of the device.

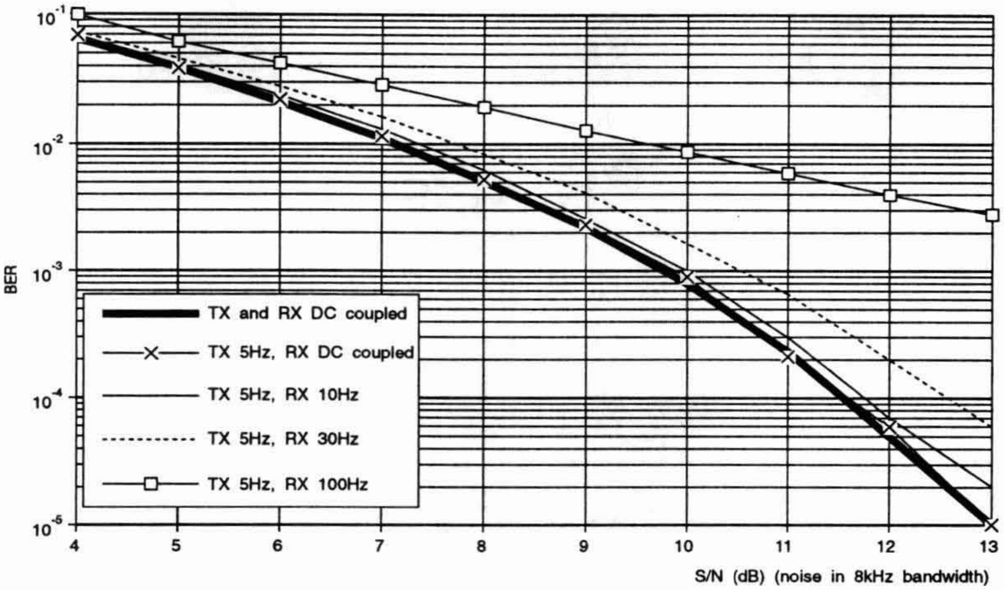


Figure 8: BER performance of the MX589

This figure represents data taken from a static system running at 8kbps with a BT of 0.3 and a noise bandwidth equal to the bit rate. With the noise bandwidth equal to the bit rate, and assuming the noise spectrum at baseband is flat, the x-axis is in essence E_b/N_0. As an alternative to a full DSP implementation, these two devices offer cost-effective and space conservative solutions to the modulation and demodulation requirements of the CDPD and Mobitex GMSK based systems.

Summary

GMSK provides a straightforward, spectrally efficient modulation method for wireless data transmission systems (e.g. CDPD and Mobitex). MX-COM's MX589 and MX909 baseband GMSK modems offer single-chip solutions, facilitating the implementation of a GMSK system using standard FM radio topologies.

Although the MX-COM baseband modems integrate the majority of the modulation signal processing requirements, some key aspects of system design must not be neglected. For instance, the modulator configuration must have a flat spectral response down to DC. In addition, the receiver's phase response must be linear across the BW occupied by the data with special attention focused on the IF filters. Following these recommendations in conjunction with a single-chip baseband modem insures excellent BER performance, low power consumption and low cost.

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[1] Murota, K. and Hirade, K., "GMSK Modulation for Digital Mobile Radio Telephony," IEEE Transactions on Communications, vol COM-29, No. 7. pp. 1044-1050, July 1981.

[2] Pebbles, P. Jr., "Digital Communication Systems," Prentice-Hall, Englewood Cliffs,

NJ, 1987.

[3] Sklar, B., "Digital Communications: Fundametals and Applications," Prentice-Hall, Englewood Cliffs, NJ, 1988.

[4] "Cellular Digital Packet Data System Specification, Release 1.0," 1993.

[5] "Radio/Modem Reference Design Guide, Issue 1, Revision 0," RAM Mobile Data, Woodbridge, NJ, 1991.

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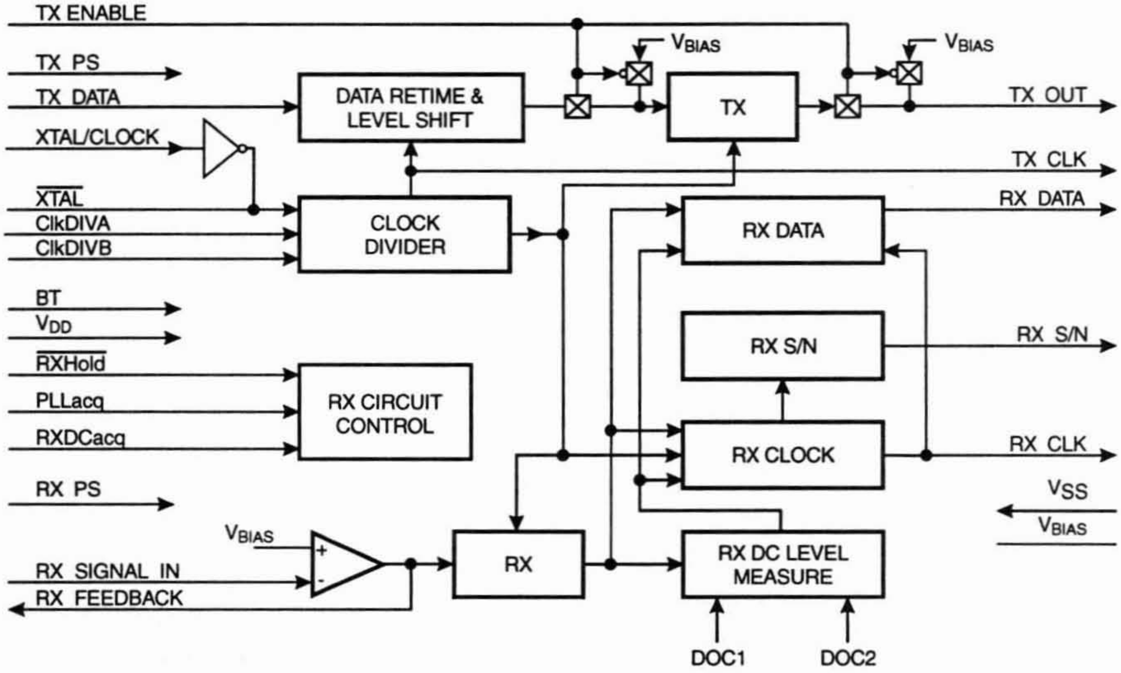
MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX589 GMSK MODEM Application


TX ENABLE
TX PS
TX DATA
XTAL/CLOCK
$\overline{\text{XTAL}}$
ClkDIVA
ClkDIVB
BT
V_{DD}
$\overline{\text{RXHold}}$
PLLacq
RXDCacq
RX PS
V_{BIAS}
RX SIGNAL IN
RX FEEDBACK
DATA RETIME & LEVEL SHIFT
CLOCK DIVIDER
RX CIRCUIT CONTROL
RX
V_{BIAS}
TX
V_{BIAS}
TX OUT
TX CLK
RX DATA
RX DATA
RX S/N
RX S/N
RX CLOCK
RX CLK
V_{SS}
V_{BIAS}
RX DC LEVEL MEASURE
DOC1
DOC2

This application note is to be read in conjunction with the current MX589 Data Bulletin. This document is issued to clarify points in currently published documents and to present new information that will enable the user to easily understand and implement this GMSK product.

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Data Transmission by FM Radio

The simplest method of sending data over FM radio is to shift the RF carrier frequency in one direction to represent a logic '1' and in the other direction for a logic '0'. This direct method is known as Frequency Shift Keying (FSK); FSK can be successful but results in a very wide transmission bandwidth requirement.

To reduce the transmission bandwidth required input data may be pre-filtered prior to modulation using a specific form of lowpass filtering. One effective method is Gaussian Filtered Minimum Shift Keying (GMSK). Figure 4 is a comparison of the bandwidth requirements of direct FSK and Gaussian filtered data.

2. Gaussian Filtered Minimum Shift Keying (GMSK)

GMSK is a method of data modulation for sending high-speed data in narrow band FM radio channels.

In its simplest form, GMSK involves passing a digital bitstream through a Gaussian filter before applying it to the input of a frequency modulator.

A Gaussian filter is a lowpass element which when excited by an impulse at its input, gives a Gaussian shaped output response.

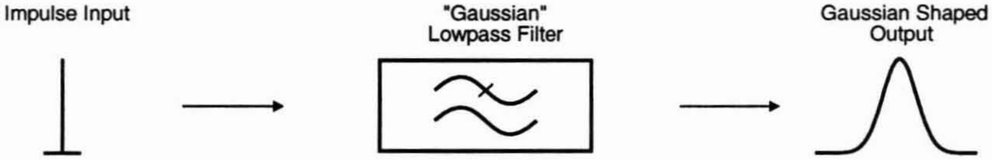

Impulse Input
"Gaussian"
Lowpass Filter
Gaussian Shaped
Output

Figure 1: The Performance of a Gaussian filter

3. GMSK in FM Radio

In an FM radio system using a GMSK modem the data flow is as shown below:

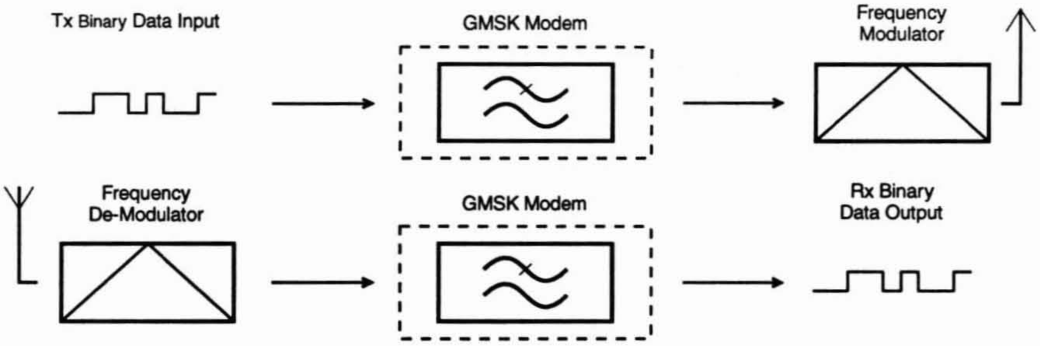

Tx Binary Data Input
GMSK Modem
Frequency
Modulator
Frequency
De-Modulator
GMSK Modem
Rx Binary
Data Output

Figure 2: Data flow in a GMSK FM Radio Modem

4. GMSK

The diagram below shows GMSK filter outputs for a logic input of '10001000'. Note that a filter delay is present and that the individual output pulse spreads across more than one bit-period.

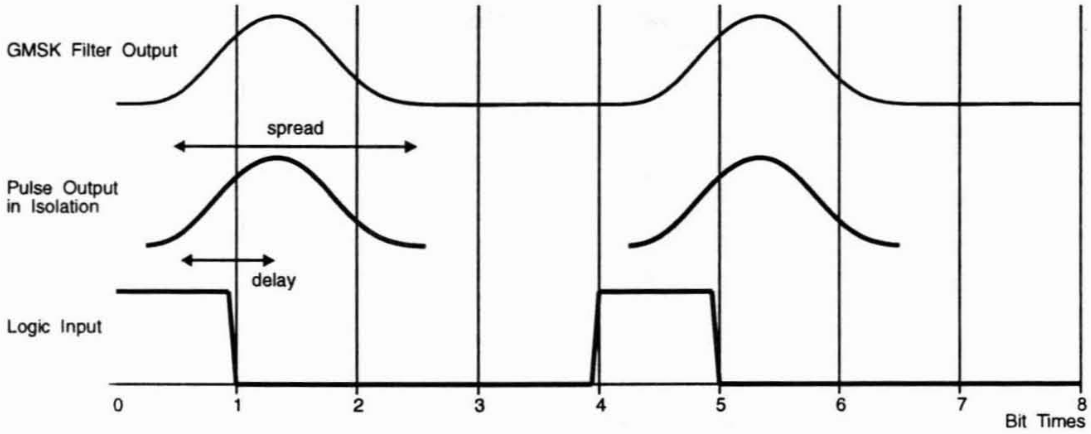
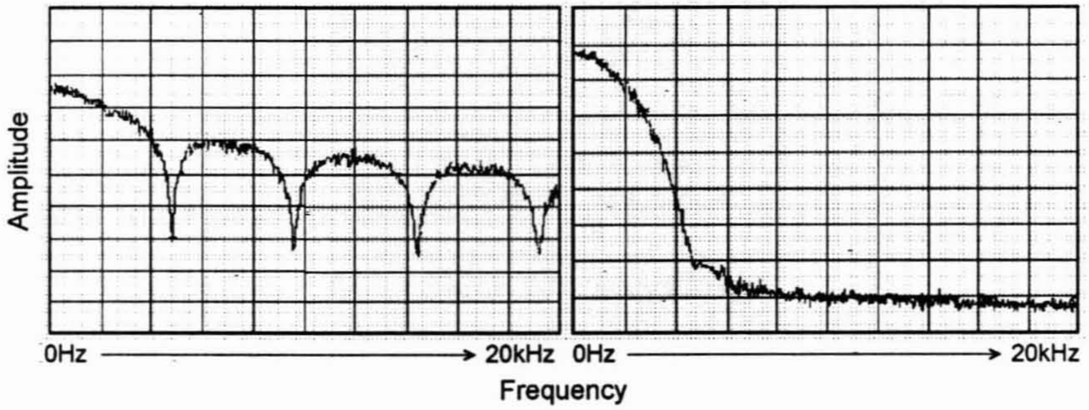


Figure 3: GMSK Filter Input/Output Relationships

True GMSK transmission, in radio, is achieved when the data output of the Gaussian filter is passed through an FM modulator having a continuous phase response, with peak deviation being set to half of the applied bit rate.

$$\text{Max deviation (Hz)} = \frac{\text{Data Rate}}{2}$$

For example: DEV_{MAX} = 2kHz for a data rate of 4kbps



4800bps random data **4800bps 'Gaussian' filtered random data**

Figure 4: Spectral Comparison of FSK and Gaussian MSK Requirements

5. Implementation of GMSK using the MX589

GMSK, as a form of modulation for high-speed data transfer is relatively simple to implement as long as careful attention is paid to several points:

5.1 Bitrate, BT, and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

1. Channel spacing
2. Allowable adjacent channel interference
3. Tx filter bandwidth (BT)
4. Peak carrier deviation (Modulation Index)
5. Tx and Rx carrier frequency accuracy
6. Modulator and Demodulator linearity
7. Rx IF filter frequency and phase characteristics
8. Use of error correction techniques
9. Acceptable error-rate

5.2 Data Formats

The receive section of the MX589 gives the lowest bit error rate with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeros' with no long sequences of consecutive 'ones' or 'zeroes'.

5.3 Coupling of Rx and Tx signals

Ideally, the Rx demodulator should be DC coupled to the MX589 'Rx Signal In' pin (with a DC bias added to center the signal around V_{BIAS} [= $V_{DD}/2$]), however AC coupling can be used provided that -

1. The 3dB cut-off frequency is 20Hz (at 8kbps) or below (i.e. a 0.1uF capacitor in series with 100kΩ). The cut-off frequency requirement changes proportionally with the applied data rate.
2. The data does not contain long sequences (in excess of 100 bits) of consecutive ones or zeroes.
3. Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a RF carrier) for the voltage into the MX589 to settle before the 'RxDCacq' line is strobed.

In practical applications, it will usually be possible to arrange for any AC coupling between the MX589 Tx output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but AC coupling between the receive discriminator and the input of the MX589 may need to have a shorter time constant to avoid problems with voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5Hz in the Tx path, 20Hz in Rx, at 8kbps.

Figure 5 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions (8kbps, V_{DD}= 5.0V, T_{AMB} = 25°C, Tx BT=0.3) for various degrees of AC coupling at the Rx Input and the Tx Output.

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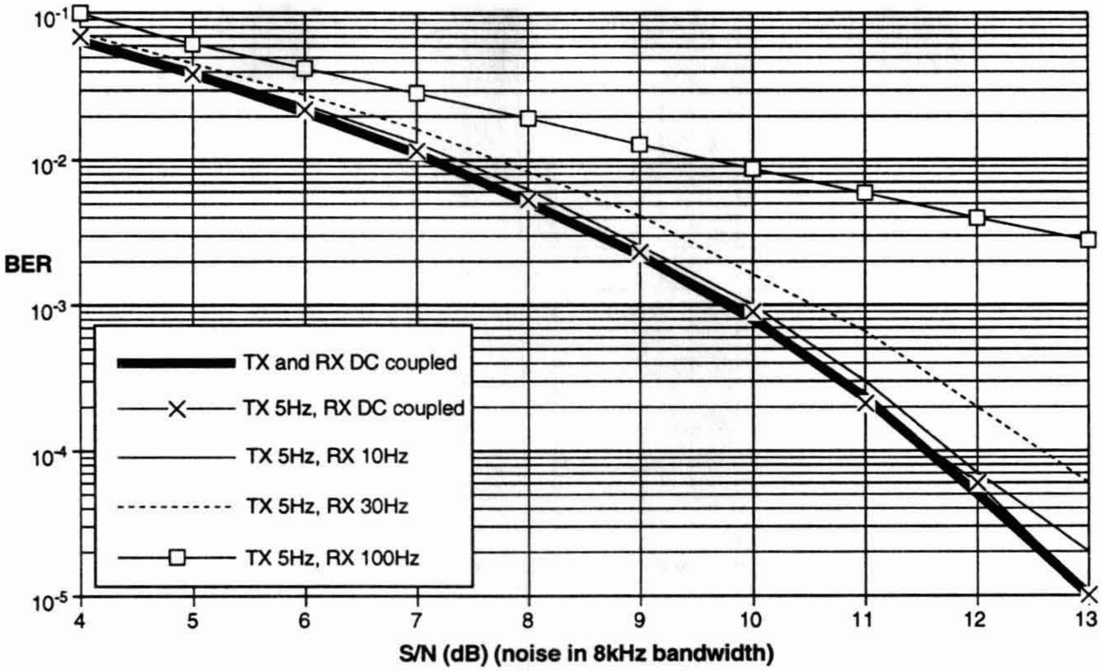


Figure 5: Typical Static Bit Error Rates

5.4 Baseband and RF Bandwidth

The required baseband bandwidth, and therefore the RF bandwidth requirement of a GMSK system is principally determined by two factors: the data rate and the system filter's response. The response characteristic with respect to an applied data rate is referred to as the system BT (bandwidth - data rate) factor.

The BT factor is the ratio of the -3dB point of the filter ($-3dBf_0$) and the applied data rate.

$$BT = \frac{-3dBf_0}{\text{Data Rate}} \qquad \text{i.e. } -3dBf_0 = BT \times \text{Data Rate}$$

As can be seen from Figure 6, a lower BT figure (0.3) allows less high-frequency components and produces, theoretically, a narrower bandwidth requirement. However, the interference caused by one bit symbol overlapping another (intersymbol interference) is increased (Figure 7).

The MX589 is capable, within the current specification, of operating to data rates of between 4kbps and 40kbps at a BT of 0.3 and 0.5; Table 1 provides a very rough guide to GMSK capabilities in narrow RF bandwidths. However, the details of the relevant system specification should always be adhered to.

Figure 6 shows the MX589 Tx filter response at BT values of 0.3 and 0.5.

BT	Channel Bandwidth (kHz)	Data Rate Max. (bps)	BT	Channel Bandwidth (kHz)	Data Rate Max. (bps)
0.5	12.5	4800	0.3	12.5	8000
0.5	25.0	9600	0.3	25.0	16000
0.5	50.0	19200	0.3	50.0	32000

Table 1: Typical GMSK/Bandwidth Capabilities

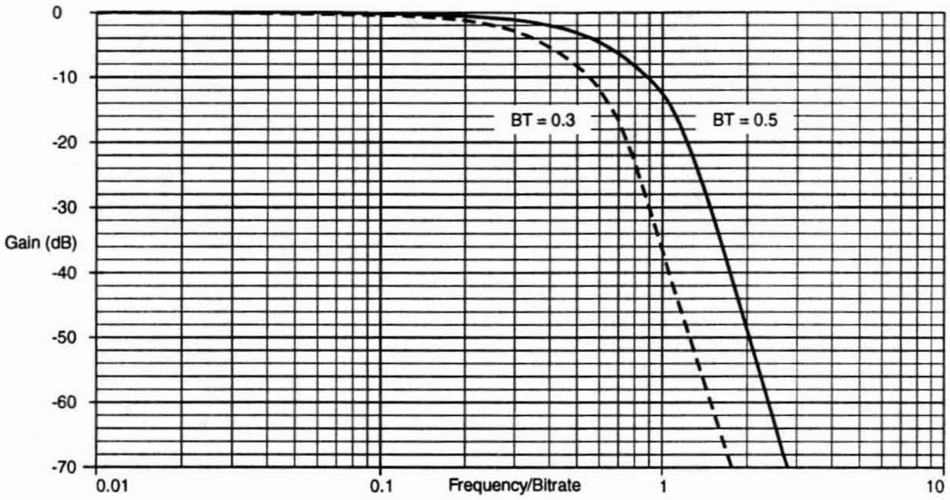


Figure 6: MX589 Tx Filter Response

5.5 Intersymbol Interference

This is the effect of one data bit overlapping the next due to the lowpass filtering. As this effect becomes more pronounced the receiving modem may have trouble deciding whether the bit is a '1' or a '0'.

Figure 7 shows the output of the GMSK modem for an input of "1 1 0 1 1 1 1 1" with BT settings of 0.5 and 0.3; the increasing effect of intersymbol interference can be clearly seen.

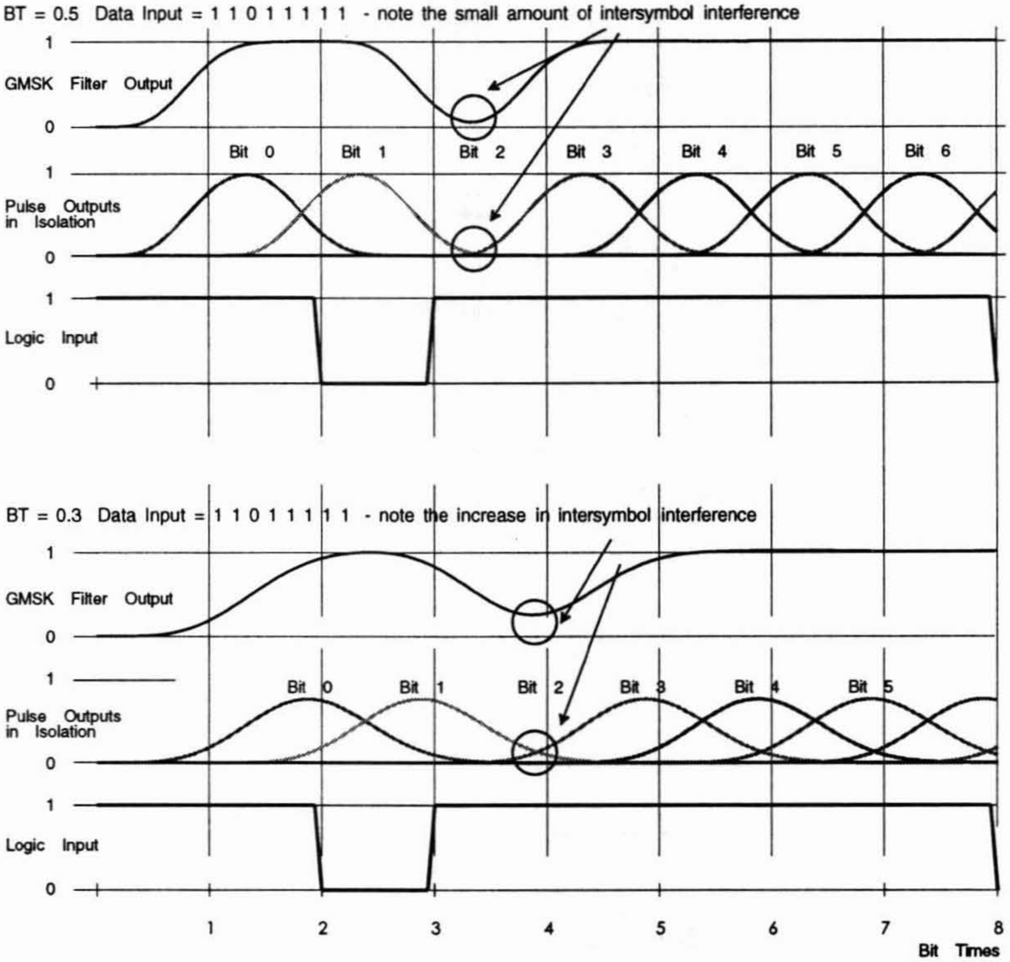


Figure 7: Illustration of Intersymbol Interference Increase due to Decrease in BT Value

6. FM Modulator, Demodulator, and IF Performance

6.1 The Eye Pattern

The EYE pattern diagram is an oscilloscope-type trace of the baseband signal (at the input to the FM modulator or at the output of the FM discriminator).

It is an indication of the condition of the signal and its path and therefore the FM modulator, demodulator, IF circuit, and channel circuit performance.

The EYE diagram provides information about the following parameters of the signal and/or system:

Channel signal/noise conditions -

Channel amplitude and phase responses -

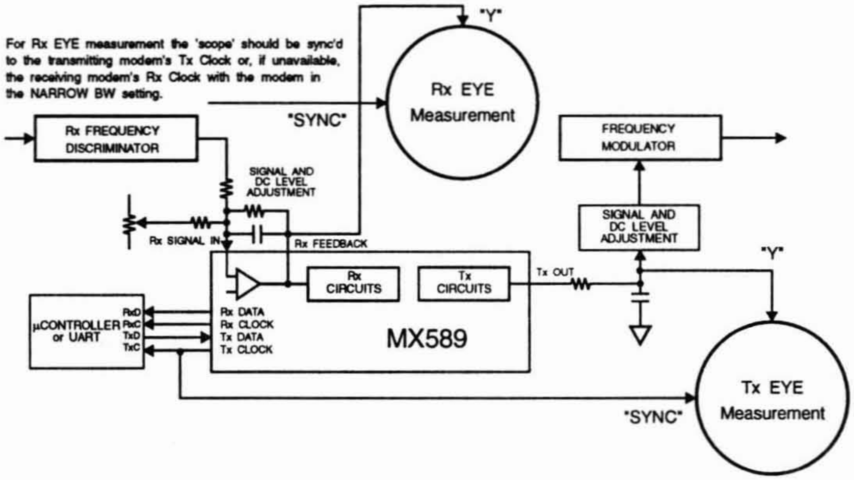
For optimum performance, the EYE pattern of the received signal applied to the MX589 for random transmitted data should be as close as possible to the examples given in Figure 9.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening (which should be approximately 0.48 of the total for a BT of 0.3, about 0.9 for a BT of 0.5).

To achieve this, attention must be paid to -

1. Linearity and frequency/phase response of the Tx frequency modulator and discriminator. The modulator frequency response should extend down to a few Hertz; two-point modulation is necessary for synthesized radios.
2. Bandwidth and phase response of the Rx IF filters.
3. Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

The diagrams on the following pages provide examples of various EYE patterns and their causes.



For Rx EYE measurement the 'scope' should be sync'd to the transmitting modem's Tx Clock or, if unavailable, the receiving modem's Rx Clock with the modem in the NARROW BW setting.

"Y"
Rx EYE Measurement
"SYNC"
Rx FREQUENCY DISCRIMINATOR
SIGNAL AND DC LEVEL ADJUSTMENT
Rx SIGNAL IN
Rx FEEDBACK
Rx CIRCUITS
Tx CIRCUITS
Tx OUT
MX589
µCONTROLLER or UART
RxD
RxC
TxD
TxC
Rx DATA
Rx CLOCK
Tx DATA
Tx CLOCK
FREQUENCY MODULATOR
SIGNAL AND DC LEVEL ADJUSTMENT
"Y"
Tx EYE Measurement
"SYNC"

Figure 8: Measurement of an EYE Pattern

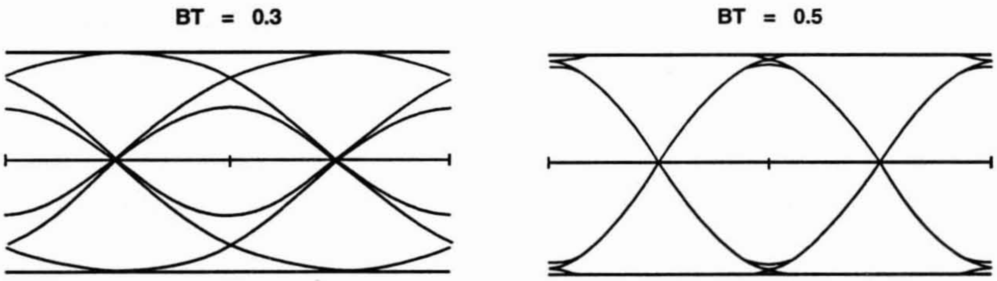


Figure 9: Typical Good EYE Patterns diagrams

6.1.1 Example Eye Patterns

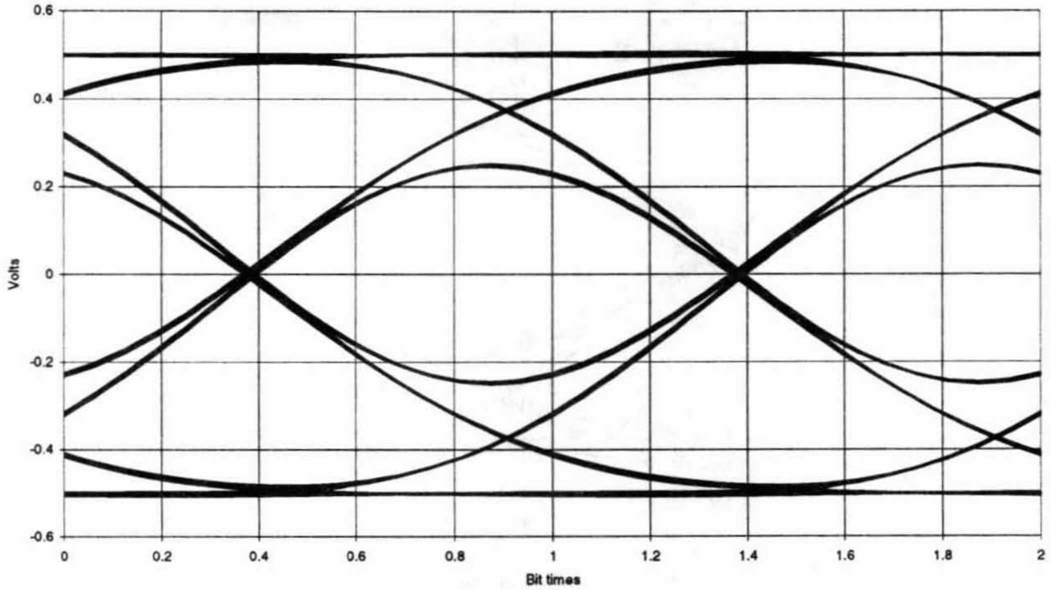


Figure 10: Good Rx EYE (BT = 0.3)

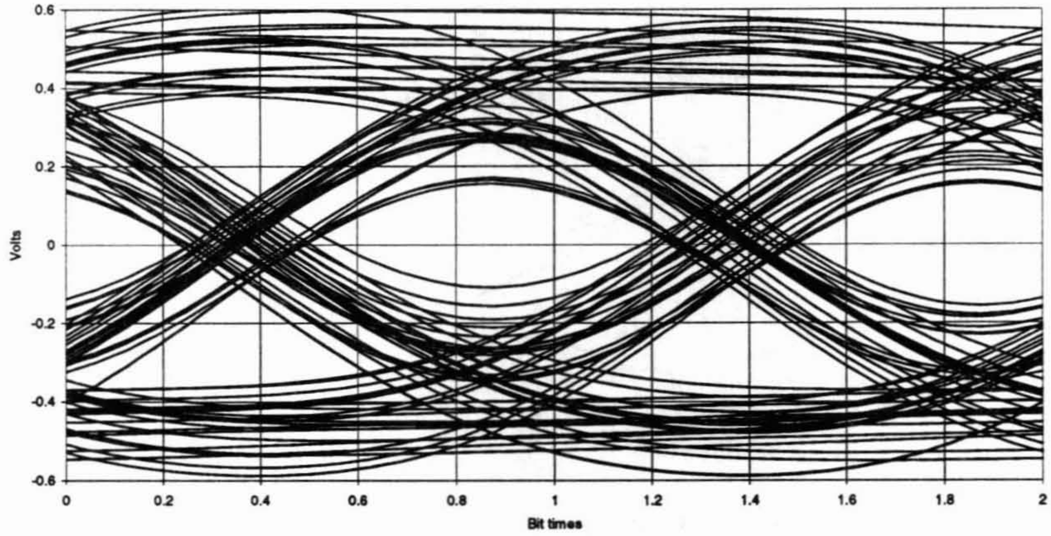


Figure 11: Effect of AC coupling (BT = 0.3)
Corner frequency approx. 1% of bitrate

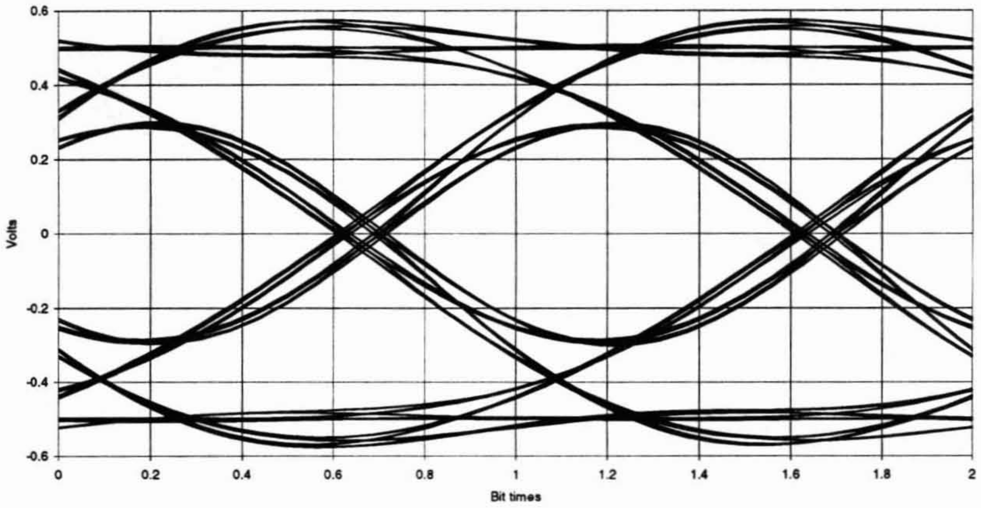


Figure 12: Effect of Poor Channel Amplitude and Phase Response (BT = 0.3)

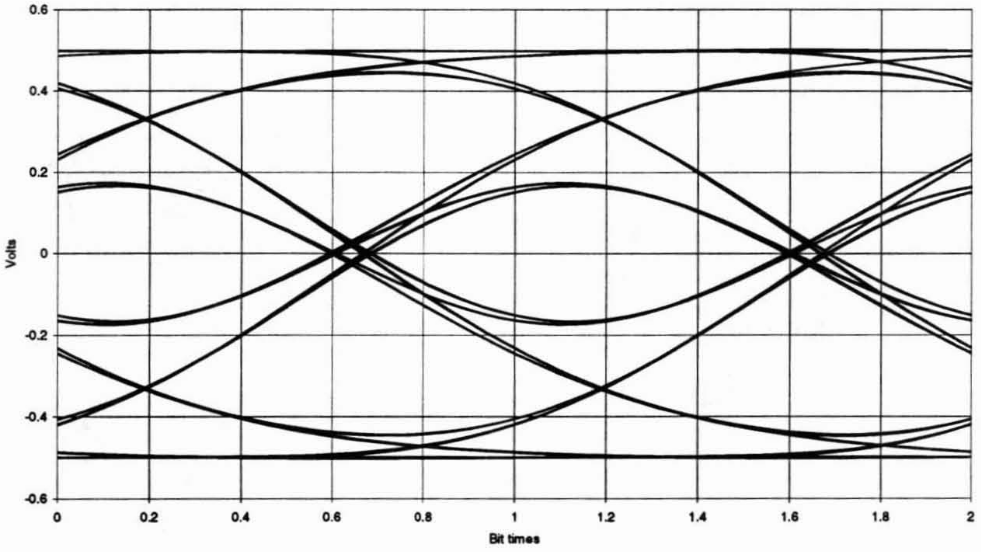


Figure 13: Effect of Slight High Frequency Attenuation (BT = 0.3)
6dB/octave low pass filtering, -3dB at 0.5 x bitrate

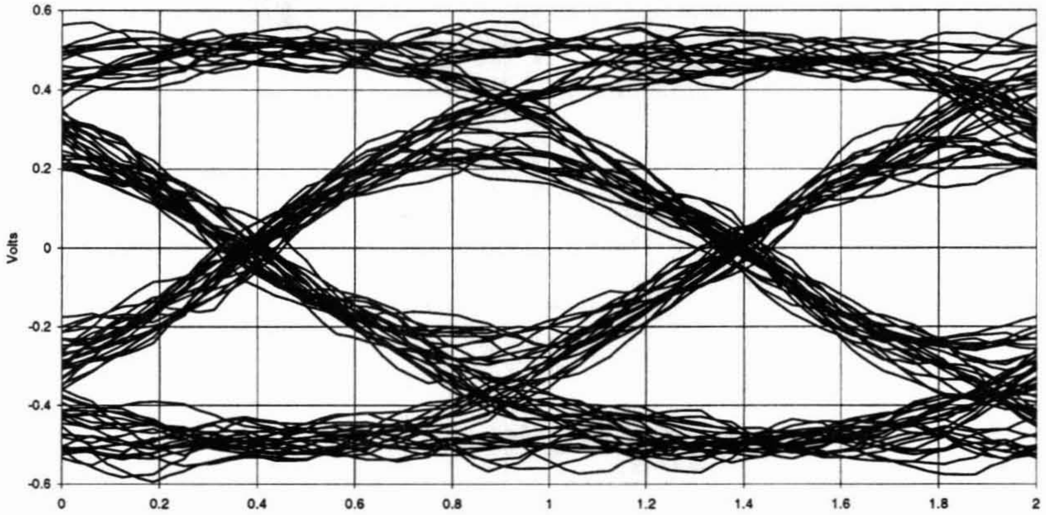


Figure 14: Effect of Noise (BT = 0.3)
Noise Bandwidth = 2 x bitrate; S/N = 25dB

7. Data Sequencing

To ensure that the MX589 Rx clock recovery and Rx level circuits are given the best opportunity to operate correctly the receive section works best with data which has a reasonably 'random' structure. The data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided. For this reason, it is recommended that data be scrambled in some manner before transmission.

A string of logic 1's will be modulated as a single frequency shift at the beginning of the string and a single frequency shift at the end; no frequency changes will occur. This will appear at the Rx modem as near DC and can result in the receiver not being able to track the incoming signal correctly. Both bit timing and level information can be lost.

Particularly when a BT value of 0.3 is being used problems also occur when single bits bounded by their complement are being sent repeatedly ('0 0 0 0 0 1 0 0 0 0' or '1 1 1 1 0 1 1 1 1' note however, that these are not the only patterns to give problems); these sequences sent many times over can cause the GMSK demodulator to give out bits in error.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should be avoided, particularly when BT = 0.3.

Many FSK and FFSK data systems use a '1 0 1 0 1 0 1 0 . . .' pattern as a synchronizing preamble, Figure 15A shows the resultant output from a system using BT values of both 0.5 and 0.3.

In this case the output of a BT = 0.3 system does not provide true level information for the level measuring circuits to lock on to. When the BT is 0.5 the output does not display the problem to the same degree.

Figure 15B, Figure 15C, and Figure 15D show outputs from inputs of '1 1 0 0 1 1 0 0 ....', '1 1 1 1 0 0 0 0 1 1 1 1 ...' and '0 1 0 0 0 0 1 0 0 ...' respectively. Where it is impossible for data to be provided to the modem within the above guidelines, it is recommended that external sequencing is used; i.e. scrambling or data coding.

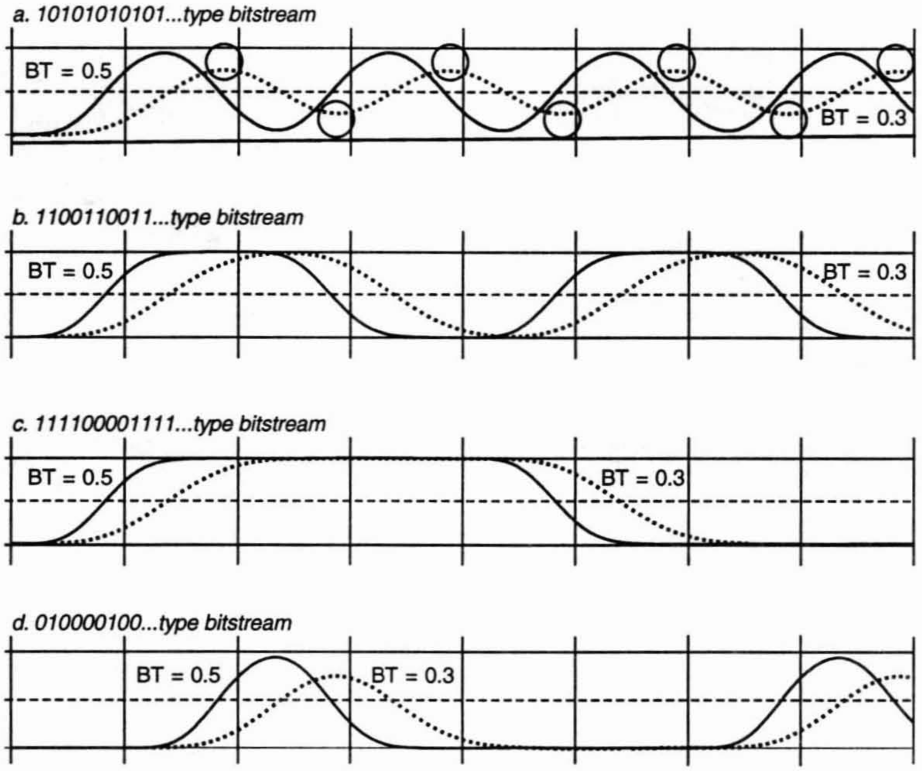


Figure 15: GMSK Output Levels for Various Input Bit Configurations

7.1 Data Randomizing (Scrambling)

As previously discussed, the receive section of the MX589 prefers data which has a reasonably 'random' structure.

Whether the applied data (digital bits) originate from a computer type system or by voice digitization, it is not always possible to ensure that streams of constant-'sense' Rx data are avoided.

Illustrated below are two simple ways to randomize data:

1. Exclusive-OR the input binary data with a pseudo-random binary stream. This method will require both Rx and Tx pseudo-random codes to be in sync.
2. Exclusive-OR the input binary data with a shifted input data stream. A self-synchronizing method which exclusive-OR's the Rx input data with a time-shifted version of itself. This method of randomizing will propagate bit errors as any Rx bit in error will be duplicated with each EX-OR function in the loop. This method is in accordance with CCITT recommendations (V.26 ter)

Preamble bits and/or SYNC words should not, of course, be randomized.

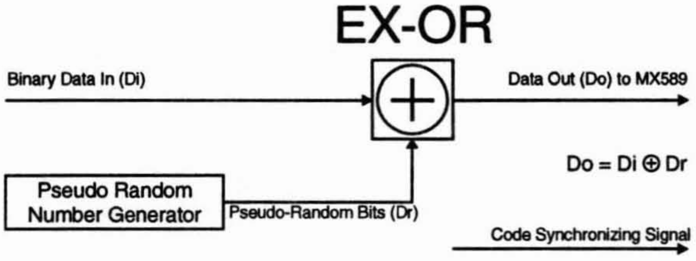


Figure 16: Exclusive-OR the Input with a Pseudo-Random Data Stream

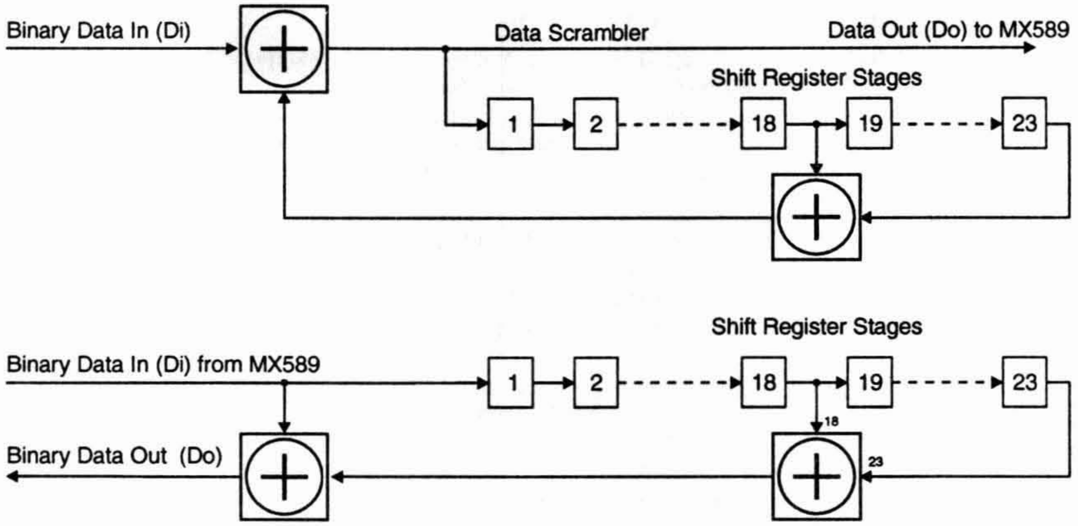


Figure 17: Exclusive-OR the Input with a Shifted Input Data Stream

7.2 Data Coding

If it is important, for hardware or system interface considerations, that the lower frequency limit of a GMSK signal is kept above a specific frequency it is possible to deliberately encode the data prior to modulation; for instance where AC coupling is employed or there are PLL control limits.

This entails ensuring that sequences (blocks) of bits that contain low –frequency components are altered to produce the required overall output. This coding can be carried out in software or hardware, as appropriate. It should be noted that if coding that results in an increase in the number of bits is used this will reduce the actual system 'data rate' unless the bit rate is increased, which in turn may take the system outside the bandwidth specification.

8. Rx 'Acquisition' and 'Hold' Modes

The MX589 may be expected to receive data efficiently under several different signal and configuration conditions depending upon the system formatting and the device coupling methods.

Conditions identified so far are:

Rx with Carrier Detect Indication

Rx with No Carrier Detect Indication

The upper and lower voltage levels of the input signal, after internal filtering, are stored on external capacitors connected to the Doc1 and Doc2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data.

As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay very slowly towards V_{BIAS}.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note however, that these pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

8.1 Rx Acquisition with Carrier Detect Indication

The MX589 can tolerate DC offsets in the received signal of at least +/- 10%V_{DD} with respect to V_{BIAS}, however to ensure that the DC offset compensation circuit operates correctly and with minimum delay, 'Low' to 'High' transitions of the 'RxDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value (Note that this can place restrictions on the value of any series signal coupling capacitor).

1. MX589 connected as Figure 2 in the current Data Sheet; inputs RxDCacq and PLLacq 'Low';
2. At the receipt of an RF carrier detect indication to the µC: wait two bit periods; place RxDCacq and PLLacq 'High' ('clamp' - Doc1 and Doc2 capacitors are rapidly charged towards a voltage midway between the Rx signal level and V_{BIAS}). The 'RxDCacq' and 'PLLacq' inputs must be placed 'High' for a minimum of 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock on to the received signal correctly. To confirm that 'lock' has been achieved it may be necessary to employ additional methods of sync detect; such as a frame detection or MX589 S/N output monitoring.
3. To give the MX589 a satisfactory reference level to 'clamp' to, it is recommended that the transmitting station is configured to provide a short period of blank carrier before the data starts.
   To calculate this period the following system parameters should be considered: Tx power-up time + Rx demodulator settling time + Rx AC coupling values [+ 2 bit times].
4. When lock is confirmed the above inputs should be taken 'Low' again and the acquisition circuits operated as described in the Data Sheet.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on. Every time a channel change occurs, the preamble/acquire sequence (steps 1 - 4) should be performed.

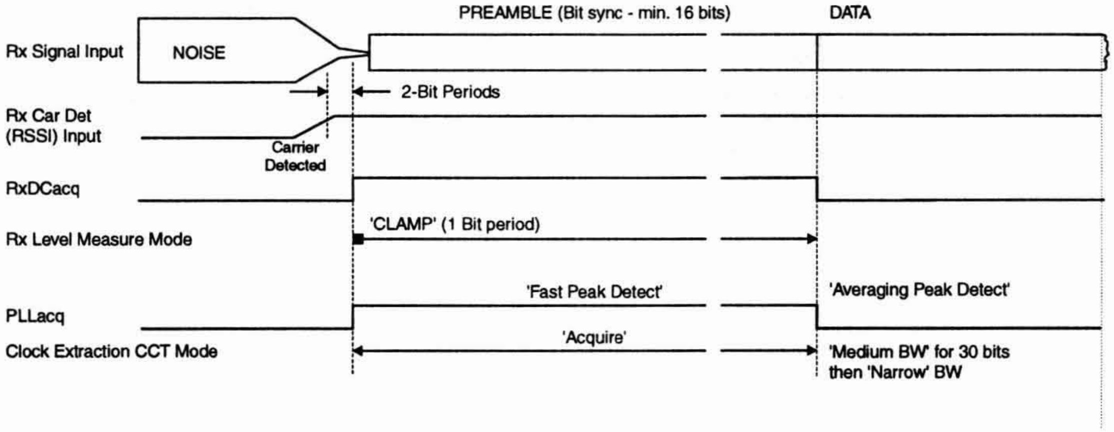
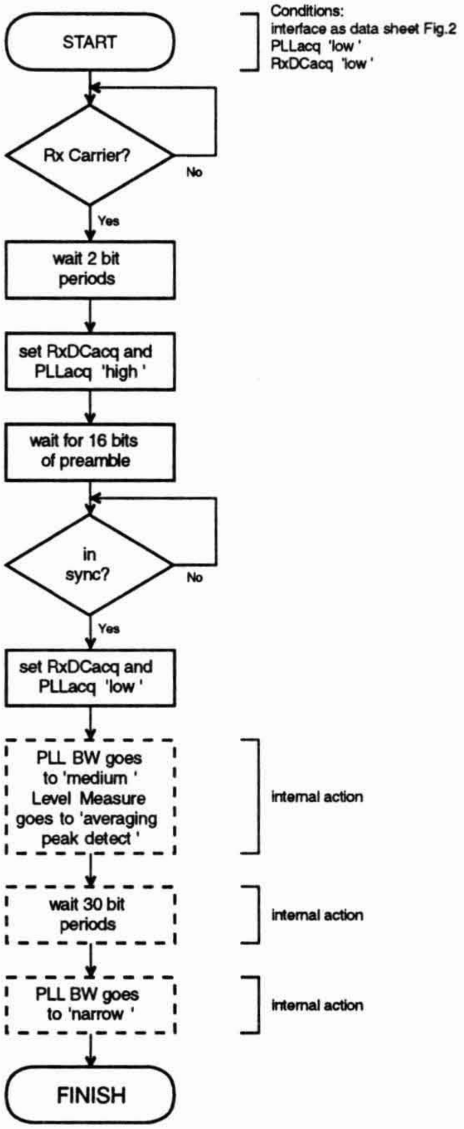

PREAMBLE (Bit sync - min. 16 bits)
DATA
Rx Signal Input
NOISE
2-Bit Periods
Rx Car Det (RSSI) Input
Carrier Detected
RxDCacq
Rx Level Measure Mode
'CLAMP' (1 Bit period)
'Fast Peak Detect'
'Averaging Peak Detect'
PLLacq
Clock Extraction CCT Mode
'Acquire'
'Medium BW' for 30 bits then 'Narrow' BW

Figure 18: Rx Acquisition with Carrier Detect Available

8.2 Rx Acquire Sequences


Conditions:
interface as data sheet Fig.2
PLLacq 'low'
RxDCacq 'low'
START
Rx Carrier?
No
Yes
wait 2 bit periods
set RxDCacq and PLLacq 'high'
wait for 16 bits of preamble
in sync?
No
Yes
set RxDCacq and PLLacq 'low'
PLL BW goes to 'medium' Level Measure goes to 'averaging peak detect'
internal action
wait 30 bit periods
internal action
PLL BW goes to 'narrow'
internal action
FINISH

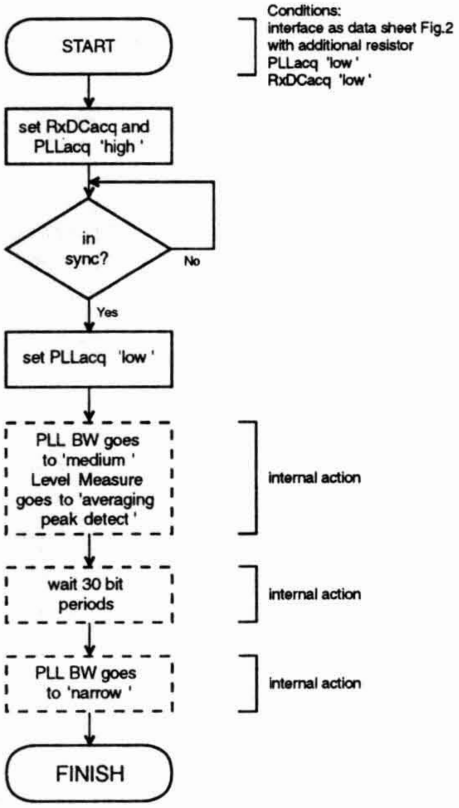

Conditions:
interface as data sheet Fig.2
with additional resistor
PLLacq 'low'
RxDCacq 'low'
START
set RxDCacq and PLLacq 'high'
in sync?
No
Yes
set PLLacq 'low'
PLL BW goes to 'medium' Level Measure goes to 'averaging peak detect'
internal action
wait 30 bit periods
internal action
PLL BW goes to 'narrow'
internal action
FINISH

Figure 19: Rx/Data Carrier Indication Available

Figure 20: No Rx/Data Carrier Indication Available

8.3 'RxHold' Input

'RxHold' Input

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more than about 0.1 bit time from the actual received data timing during the time that the 'RxHold' input is 'Low'.

The 'RxDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

8.4 Rx Acquisition with No Carrier Detect Indications

If the receive system has no method of indicating when the RF carrier or signal preamble will start it is recommended that:

1. With reference to the current MX589 Data Sheet, Figure 2, a new component, resistor R, of value between 1.0MΩ and 2.0MΩ, should be connected across output pins Doc1 and Doc2.
2. RxDCacq and PLLacq inputs set 'Low'.
3. Before or when the required signal is expected to appear: Set RxDCacq and PLLacq 'High'; the modem acquisition circuits will clamp and then lock and track the data. The RxDCacq pin setting may remain in this position for the duration of operation.
4. The PLLacq pin should be taken 'Low' when lock has been confirmed to improve the signal-to-noise performance by reducing the PLL bandwidth. With the additional resistor, R, connected, there is no advantage in taking the RXDCacq input 'Low' again to attain the Averaging Peak Detect mode.
5. If the received signal has a long preamble sequence, e.g. 100bits, RxDCacq and PLLacq settings may remain low; the circuitry will eventually attain lock.

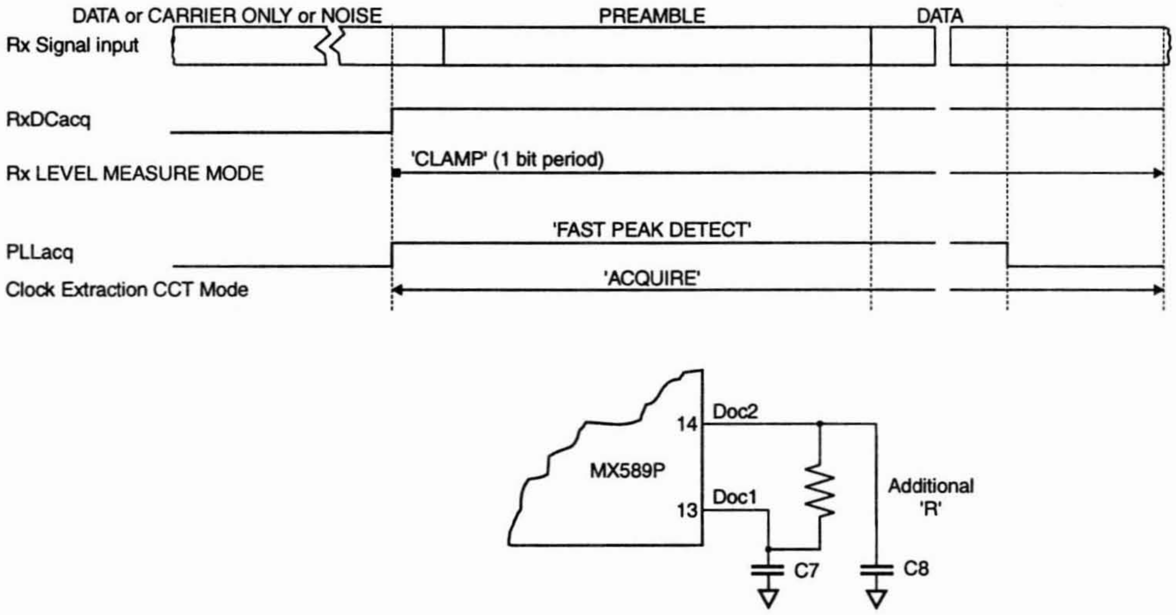

DATA or CARRIER ONLY or NOISE
PREAMBLE
DATA
Rx Signal input
RxDCacq
Rx LEVEL MEASURE MODE
'CLAMP' (1 bit period)
'FAST PEAK DETECT'
PLLacq
Clock Extraction CCT Mode
'ACQUIRE'
MX589P
14
Doc2
13
Doc1
Additional 'R'
C7
C8

Figure 21: Rx Acquisition with No Carrier Detect Available

9. Interleaving on Systems with Forward Error Correction (FEC)

Data for transmission, with its FEC overhead, is loaded to the MX589 serially.

If, during transmission, a section of data bits (block) is corrupted by some external disturbance (ignition interference etc.) there is a possibility that a whole block (or blocks) of data will be damaged making large amounts of data at the Rx uncorrectable and therefore unreadable. This will result in a request for a re-transmission and reduction in the overall data rate.

If however, prior to loading to the modem, the data bits within blocks are interchanged between blocks (interleaved), then if external disturbance is experienced and a section is damaged, when the blocks are rebuilt (de-interleaved) at the receiver only one or two of the bits in each original block of data will be in error therefore allowing the FEC system a better chance of correction.

With reference to the example in Figure 22, interleaving is carried out externally, prior to loading the modem. Data is supplied to the interleaving process in the following sequence (real data):

A1, A2, A3, A4, ...H9, H10

and read-out from the process in the following sequence (interleaved data):

H1, G1, F1, E1, ...H2, G2, ... B10, A10.

De-interleaving is the reverse process.

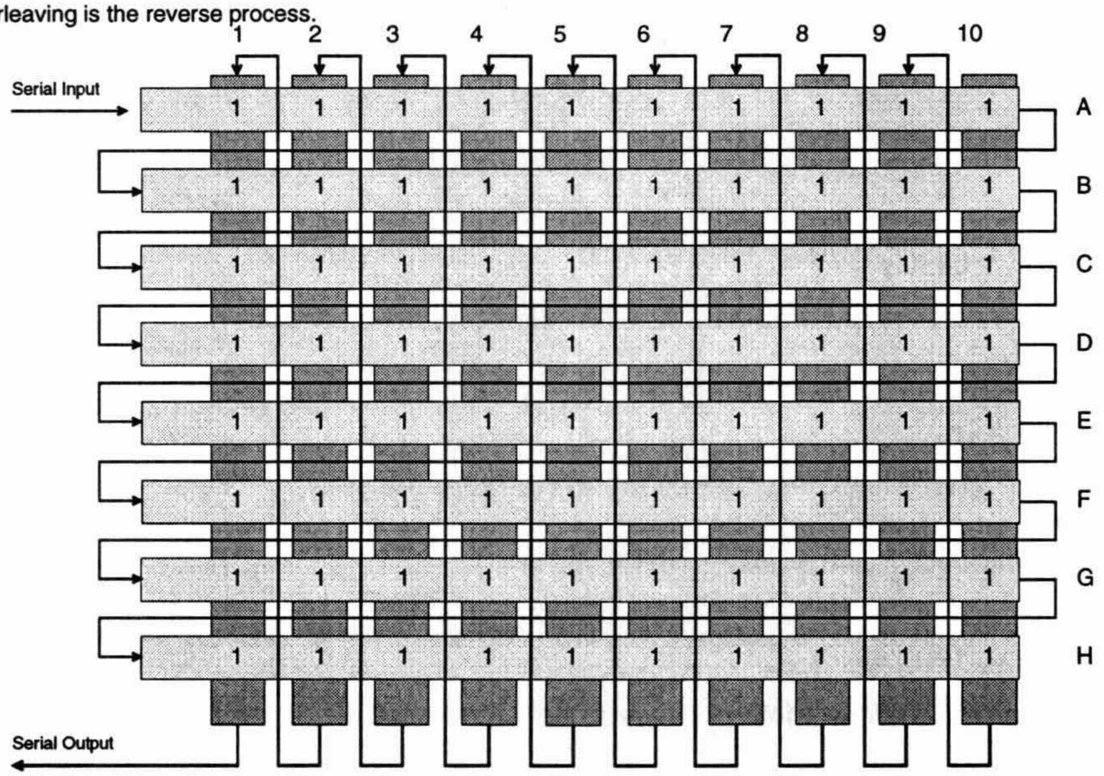


Figure 22: Interleave Example

10. Alternative Data Rates

The current MX589 Data Sheet specifies device operation at data rates of between 4kbps and 64kbps at 5.0 volts and Xtal/clock frequencies of between 1.0MHz and 10.4MHz.

To enable this device to be used, efficiently, in the maximum number of data transfer applications, this Application Note details tables that are intended to provide more information to operate at data rates other than those illustrated in the data sheet.

With due regard to the operating V_{DD} values recommended in the Data Sheet, the following parameters control/affect the data rate operation of this device:

Clock Oscillators and Dividers.

Tx OUT output external component (R1 and C1) values.

The values of Doc1 and Doc2 capacitors (C7 and C8). Note that peripheral components to the Rx Level

Measurement circuitry, should also be considered.

10.1 Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz (V_{DD} = 3.0V) or 1.0MHz to 6.5MHz (V_{DD} = 5.0V) may be employed, depending upon the desired data rate.

A division ratio to facilitate data-rate setting is controlled by the logic level inputs on the ClkDivA/B pins. The formula below is employed to calculate the data rate:

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (ClkDivA/B)}}$$

10.2 Tx OUT Output Components R1 and C1

The RC network formed by R1 and C1 is required between the Tx OUT pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator. The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

For a BT of 0.3	R1C1 = 0.34/bit rate (bps)
For a BT of 0.5	R1C1 = 0.22/bit rate (bps)

10.3 Doc1 and Doc2 Capacitor (C7 and C8) Values

Note the Data Sheet recommendations with regard to these two components:

C7 and C8 should both be 0.015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 0.03µF at 4kbps, 3000pF at 40kbps.

10.4 Alternative Data Rate Tables

10.4.1 3.6864MHz

For a Xtal/Clock value of 3.6864MHz					
Data Rate (bps)	**ClkDiv A**	**ClkDiv B**	**BT**	**R1 (kΩ)**	**C1 (pF)**
7200	1	0	0.3	100	470
7200	1	0	0.5	62	470
14400	0	1	0.3	130	180
14400	0	1	0.5	130	120
28800	0	0	0.3	62	180
28800	0	0	0.5	62	120

Table 2: Data Rate for 3.6864MHz Xtal/Clock

10.4.2 4.096MHz

For a Xtal/Clock value of 4.096MHz					
Data Rate (bps)	**ClkDiv A**	**ClkDiv B**	**BT**	**R1 (kΩ)**	**C1 (pF)**
4000	1	1	0.3	120	680
4000	1	1	0.5	120	470
8000	1	0	0.3	91	470
8000	1	0	0.5	120	220
16000	0	1	0.3	47	470
16000	0	1	0.5	91	150
32000	0	0	0.3	47	220
32000	0	0	0.5	47	150

Table 3: Data Rate for 4.096MHz Xtal/Clock

10.4.3 4.9152MHz

For a Xtal/Clock value of 4.9152MHz					
Data Rate (bps)	**ClkDiv A**	**ClkDiv B**	**BT**	**R1 (kΩ)**	**C1 (pF)**
4800	1	1	0.3	100	680
4800	1	1	0.5	100	470
9600	1	0	0.3	91	390
9600	1	0	0.5	47	470
19200	0	1	0.3	100	180
19200	0	1	0.5	91	120
38400	0	0	0.3	47	180
38400	0	0	0.5	47	120

Table 4: Data Rate for 4.9152MHz Xtal/Clock

10.4.4 8.192MHz

For a Xtal/Clock value of 8.192MHz					
Data Rate (bps)	**ClkDiv A**	**ClkDiv B**	**BT**	**R1 (kΩ)**	**C2 (pF)**
64000	0	0	0.5	47	82

Table 5: Data Rate for 8.192MHz Xtal/Clock

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX909A Signal Acquisition Principles

Introduction

This Application Information publication provides guidance on the correct way of using the automatic level and timing extraction sequences of the MX909A as triggered by the AQLEV and AQBC bits of the Command Register.

The techniques detailed should work in most radio systems but slightly different operation could lead to worthwhile improvements for specific cases. Experimentation will be necessary to evaluate the performance of the procedures in comparison with system requirements.

Bit Clock Extraction and Receive Level Measurement Principles

The clock extraction circuits operate by storing on-chip a current best estimate of the bit timing of the received signal. These clock extraction circuits track the timing of the input signal by monitoring the data zero-crossings. They will eventually lose track of the timing if these do not occur for extended periods.

As data is received the device continually updates the current best estimate, unless the 'Hold' setting is selected in which case the estimate is frozen. The input signal can change the internal estimate at a speed related to the bandwidth set (PLLBW).

During acquisition the PLLBW is initially set to 'Wide' and the input signal can then rapidly alter the internal estimate. As the clock extraction circuits home-in on the received data timing the bandwidth is automatically switched to 'Medium' for 30 bits to reduce the amount of jitter and hence improve the BER performance; the setting is then changed to the residual value (as set by the Control Register, PLLBW bits).

The 'Hold' setting is intended to enable clock retention during short fades.

The upper and lower voltages of the input signal, after internal filtering, are stored on external capacitors connected to the DOC1 and DOC2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data. As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay slowly towards VBIAS.

During acquisition the two capacitors are rapidly charged toward the input voltage over 1-bit period (Clamp), the capacitor voltages then follow the input signal using Lossy Peak Detect to quickly establish the upper and lower levels. As the signal is acquired the mode automatically changes to the residual setting (as set by the Control Register, LEVRES bits). The 'Hold' setting is intended to enable level retention during short fades.

Note that to operate correctly in the 'Peak Averaging' mode it is required that bit timing has already been established.

The level extraction circuits require the voltages present during pairs of '1's' and '0's', i.e. the upper and lower values. If '00' and '11' sequences do not occur for periods greater than approximately 100 bits the levels stored will not accurately reflect those of the input wave.:

Acquisition Operation

The acquisition sequences available to the user of the MX909A are intended for 2 types of system:

1. 'Mobitex' type systems with some form of carrier or signal detect facility.
2. Systems with no carrier or signal detect indication.

In both cases it is assumed that the incoming signal to be detected consists of a bit sync pattern (..11001100..) followed by a system synchronization pattern and that the device is set to raise an interrupt when this occurs (an SFS or SFH task has been set). The following techniques should lead to reliable detection and acquisition of the start of isolated data for most radio systems. (See note on ac coupling).

'Mobitex-Type' - Carrier Detect Indication Available

The device must lock-on to the incoming signal within the 16 bits of bit sync; to achieve this it is necessary to activate both AQBC and AQLEV acquisition sequences at or before the start of the bit sync, typically during a period of unmodulated carrier which precedes messages. In this case the AQBC and AQLEV automatic sequences can be used with the residual settings for the PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Peak Averaging'. The BER will improve toward its steady value over a period of approximately 30 bits from the start of the bit-sync.

It is important that when the AQLEV acquisition sequence is started the voltage level of the input wave is within, or at worst just outside, the extremes of a '11110000' data pattern.

No 'Carrier Detect' Available

Where no carrier or signal detect circuitry is available the device has to lock onto the incoming signal with little or no cue from the controlling device, this will of course mean that acquisition will take longer and that decoding errors are more likely.

The MX909A must track the incoming signal continuously for a data signal and the best settings to achieve this will be PLLBW = 'Wide' and LEVRES = 'Lossy Peak Detect'. To initiate this the AQBC and AQLEV bits would need to be set with the residual PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Lossy Peak Detect' or 'Peak Averaging'.

When the synchronization pattern is successfully detected the PLLBW and LEVRES functions will automatically sequence to the residual setting.

Where the device is required to detect a signal in this way it is recommended that the bit sync sequence of repetitive '..0011..' bits is extended from 16 (Mobitex spec.) to ≥64 or that the pre-message unmodulated carrier period is extended. Also it may be found advantageous to lengthen the frame sync sequence to reduce the possibility of frame sync falsing.

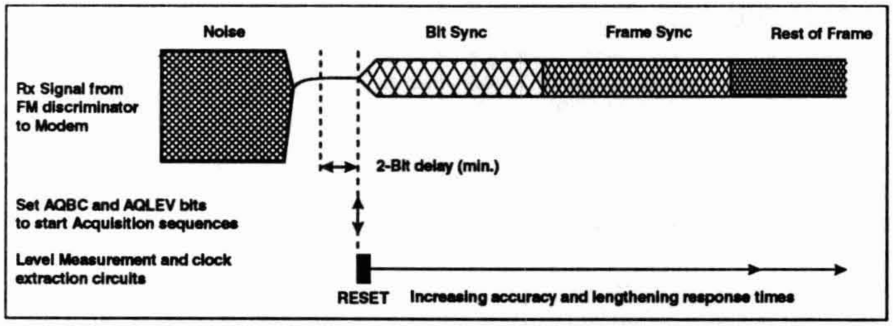

Noise
Bit Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
2-Bit delay (min.)
Set AQBC and AQLEV bits to start Acquisition sequences
Level Measurement and clock extraction circuits
RESET
Increasing accuracy and lengthening response times

Figure 1: Bit Clock and Level Acquisition Example

Acquisition Notes

Frame Sync Falsing

When noise or an unmodulated carrier is fed into the device the output of the internal bit decode circuits will effectively be random data. This will have the effect of triggering the frame-sync detect circuit whenever this random data matches the frame-sync bytes programmed. There is little possibility of this happening if a Search for Frame Head or Search for Frame Sync task is set just before the beginning of the frame-sync bytes.

However if the device is set to detect a message a long time before it appears, and no carrier detect is available, the possibility of falsing is increased. This problem is aggravated in the case of the Mobitex system which specifies that the frame sync must be detected with up to any one bit in error; this raises the probability of falsing, due to random data, from 1 in 2^{16} bits to 17 in 2^{16} bits.

The user can significantly reduce the chances of falsing by providing extra frame sync bits after those programmed in the MX909A. For example, when receiving a signal with 4 bytes of frame sync the receiving device is programmed with the first two bytes (LFSB), when these are detected using the SFS task, two RSB tasks are issued.

Decoding of the signal only continues if these next 2 bytes match the last two bytes of the 4 byte frame sync otherwise the search would be restarted.

Short Unmodulated Carrier and Bit Sync Sequences

The most critical case to be met is to use the MX909A in a system where no carrier detect or signal presence indicator is available, the frame-sync is short and the unmodulated carrier is present for a short period.

The device is required to lock-on to the incoming signal within 16 bits whilst also dealing with the potentially large dc and level changes that can occur just before the message is received.

Operating to such a system may result in some proportion of received messages being missed due to frame sync falsing and missing the frame sync bytes due to decoding errors. It is therefore recommended that the MX909A is used in systems with a short unmodulated carrier and bit sync sequences, only if a carrier detect or similar indication is available.

AC Coupling

The effect of ac coupling is to reduce the static BER performance for a given S/N ratio as it causes low frequencies to be attenuated and cause dc changes to appear as a decaying voltage superimposed upon the signal. A carrier, giving a dc shift, coming on near the start of a message will have the effect of confusing the level detection circuitry and hence cause errors in extracting data. It would be better to delay the message appearing until any dc shift had decayed thus improving the likelihood of correct acquisition. In either case the automatic acquisition sequences can be used.

Automatic Acquisition Sequences

Sequences of operation for automatic acquisition. For situations when a bit sync pattern is not being searched for (SFS or SFH is not set) the MX909A uses a fixed number of bits delay in switching between the modes:

AQLEV

SFH or SFS is set within 28 bits of AQLEV being set:

1 bit of clamp
Lossy peak detect until frame sync is detected
Residual setting

SFH or SFS is not set: 1 bit of clamp

30 bits of Lossy peak detect
Residual setting

AQBC

SFH or SFS is set within 14 bits of AQBC being set:

'Wide setting' until frame sync detected
30 bits of 'Medium setting'
Residual setting

SFH or SFS is not set: 16 bits of 'Wide setting'

30 bits of 'Medium setting'
Residual setting

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APPLICATION NOTE

MX909A Fade Management, Data Detection, and Carrier Drift Management

1. Introduction

The MX909A is a full function baseband GMSK modem suitable for use in MOBITEX[1] and general purpose wireless packet data applications. It provides several automated functions to support robust, high performance, wireless data links. This document describes issues and strategies relating to fading applications, data detection in continuous carrier systems, and transmit/receive r.f. carrier drift. It also describes pertinent MX909A features and controls which may be used in an MX909A based system.

2. Fade Management

2.1 Synchronous Decoding & Receiver Training

In order to accurately decode a received data stream, a synchronous modem must properly recover its clock and signal components which are then interpreted to reconstruct the transmitted data. Because transmit and receive modems are independent circuits (having separate and different local clock frequencies and signal levels) a receiving modem must be trained or synchronized, immediately prior to each data transfer, to establish a common and coordinated sense of bit timing. In addition, the receiver must also be trained to establish a sense of nominal signal amplitude against which the received data signal is compared to properly interpret its data bit values.

Training is performed by transmitting a specific data stream, the preamble, which provides evident and consistent timing (zero crossing) and amplitude (maximum peak-to-peak range) characteristics. During the training period, a receiving modem adjusts its local clock and level circuits until the known preamble data stream is accurately reconstructed. Once this adjustment is complete, the transmit and receive modems are synchronized and user data can be reliably transferred. (Note that data transfer must immediately follow the preamble or synchronization could be lost due to relative clock and level drift between transmit and receive modems.)

In mobile wireless applications, dynamic changes in the radio channel alter the frequency, phase, and amplitude of transmitted signals. In order to maintain its synchronization through these changes, a receiving synchronous modem may use feedback techniques to dynamically revise its local clock and level circuits according to the changing nature of the received signal.

2.2 The Fading Problem

A particularly challenging situation occurs when multipath interference[2] and receiver shadowing dramatically reduce received signal strength, resulting in a loss of input signal required to drive the synchronization feedback system. This can cause a loss of synchronization as the feedback system blindly hunts. Once synchronization is lost, the receiving modem cannot accurately interpret the signal even after sufficient signal strength returns upon exiting from a fade. Through this mechanism, the loss of synchronization can cause the loss of a significant portion (or all) of the 'post-fade' section of a transmission.

2.3 Fade Management Strategies

Fades occur in virtually all mobile wireless systems. This has given rise to countless fade management strategies. Three different fade management strategies which may be used individually or in combination are described below.

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[1] MOBITEX is a trademark of the Telia Corporation.

[2] Multipath interference is the result of a radio signal propagating via multiple paths to reach the same receiver. The multiple paths can be created by reflecting objects which produce an indirect path from transmitter to receiver. Because the multiple paths may be of different lengths the multipath signals, originating from the same source, will likely be out of phase at the receiver's location. At the extreme, the phases of the multiple paths cancel to produce an effective blanking of the received signal.

2.3.1 Receiver Diversity

Diversity uses multiple receive paths (antennae, etc.) to ensure that at least one of the paths receives a strong signal at all times. Because of its high cost, diversity is usually reserved for special, high availability wireless links.

2.3.2 Limit or Lock Tracking Systems During Fades

Another strategy attempts to maintain synchronization through a fade by constantly or momentarily disabling or limiting the dynamic response of synchronization tracking circuits. If an impending fade can be detected before it becomes too severe, locking or holding the receiver tracking circuits may sustain synchronization until the fade passes. If the hunt rate of the tracking circuits is continuously limited, the total tracking error which accumulates during a fade may be insufficient to cause a loss of synchronization. This approach eliminates the need to anticipate a severe fade.

2.3.3 Tolerate Synch Loss During Fades But Quickly Resynchronize Thereafter

A third strategy uses rapid tracking response to quickly resynchronize after a fade. The rapid response can be applied only upon detecting a fade or it may be constantly used at the expense of a reduced BER[3] in the presence of noise during non-fade periods.

2.3.4 Strategy Selection

Optimum strategies can be based on a combination of the strategies described and can vary widely depending upon the dynamics of the entire system. Fade probability, depth, frequency, and attack/decay rates along with the dynamic response of the complete receiver system (including radio circuits) all influence a wireless link's performance. Aside from diversity techniques, fade management generally involves tuning selected dynamics in the receiver system to best balance performance tradeoffs.

2.4 Using the MX909A

The MX909A provides direct program control of the dynamics of its clock and level synchronization and tracking circuits. In addition, it provides automatic macro sequencing of clock and level modes to support a typical frame start synchronization process without the need for low level program supervision. While the automatic operation of synchronization functions is usually preferred, the MX909A provides users the flexibility to implement custom fade management strategies.

2.4.1 Receiver Clock PLL Controls for Acquisition/Tracking

The MX909A uses a phase locked loop (PLL) to adjust and maintain its receiver clock. To most rapidly lock onto a received signal, the PLL dynamic response would be very fast. This can be achieved by using a wide bandwidth feedback system in the PLL. To sustain PLL lock and lowest BER, however, the optimal PLL dynamic response would usually be slower in order to be more stable in the presence of noise. The latter can be achieved by using a relatively narrow bandwidth feedback system in the PLL.

To support optimum system performance, the MX909A PLL provides four dynamic response modes which can be selected at any time under software control. The modes are: Wide Bandwidth, Medium Bandwidth, Narrow Bandwidth, and Hold. The Hold mode stops all PLL tracking adjustments while the others provide varying response.[4] The automatic clock acquisition (synchronization) process first operates the PLL in the Wide Bandwidth mode in order to most quickly lock onto the receive clock signal. At specific times[5], the mode is automatically changed to the next slower bandwidth until the user's previously configured 'normal' (slowest allowed) mode is reached.

---

[3] Bit Error Rate: That proportion of total transmitted bits which are received in error.

[4] It should be noted that differences between transmit and receive clock frequencies will cause a receiver to eventually lose synchronization if the PLL is kept in Hold mode.

[5] Refer to the MX909A data bulletin for a more detailed description of mode shift timing.

2.4.2 Level Acquisition and Tracking

The MX909A uses two capacitors, Doc1 and Doc2, on which the peak maximum and minimum ('peak' and 'valley') received signal voltages are integrated and held. These voltages, taken together, establish a sense of nominal peak-to-peak signal amplitude and d.c. level by which to interpret received signals. Each of the peak and valley integration circuits uses a 'leaky' RC filter, comprising one of the 'Doc' capacitors in series with an internal resistor as shown in Figure 1. This method allows the reference levels on the Doc capacitors to adapt as the received signal's amplitude and d.c. bias change.

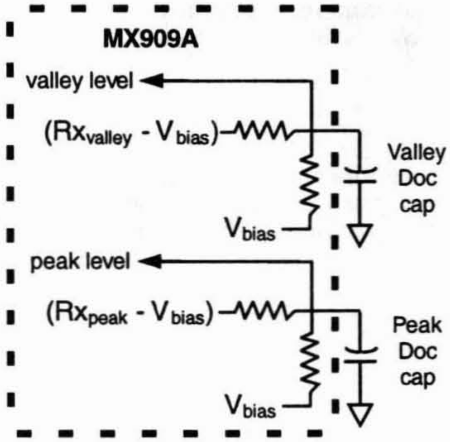

Figure 1, Simplified Schematic of Level Circuit

The MX909A provides four level circuit modes of successively slower response: Lossy Peak Detect, Peak Detect, Peak Averaging, and Hold. Hold disables any capacitor voltage level updates and the capacitor level decays toward V_{BIAS} at the slowest available rate. These modes provide a range of responses which can be used to both rapidly acquire and subsequently sustain receive signal levels. While an automatic sequence of modes is usually preferred to acquire level voltages, program control can be used to dynamically select different modes to achieve special tuning requirements.

3. Data Detection

The automatic level tracking functions of the MX909A adapt to receive signal level variations to maintain good BER performance under realistic wireless link conditions. These level tracking and other modem functions are typically activated when link activity is indicated by radio frequency carrier detect circuits. Other systems, however, transmit a continuous carrier which is intermittently modulated with a data stream. In such systems, the automatic level detect functions of the MX909A can adapt to the low receive input signals produced by the discriminator and cause the MX909A to demodulate the quiet channel's noise. Because of the random nature of this noise, occasional frame synchronization patterns may occur and be detected. Such continuous carrier systems require a baseband data detect function to qualify whether frame synchronization search functions should be initiated.

A simple data envelope detect circuit can be constructed using the voltages produced by the level acquisition and tracking circuits inherent in the MX909A (see Section 2.4.2, Level Acquisition and Tracking). Such a circuit observes the Doc1 and Doc2 voltages with a high impedance circuit to ensure that the received signal envelope, indicated by those voltages, is sufficiently high to warrant a frame synchronization search.

4. Extreme Carrier Drift

Although the MX909A tolerates significant transmit carrier/receiver local oscillator frequency differences, a system may desire additional tolerance to compensate for excessive receive local oscillator frequency shifts which can be caused by extreme environmental factors. Such a system requires a signal to indicate the relative error between transmit and receive oscillators. This 'oscillator error' signal can then be used in a local oscillator adjustment circuit to track the transmit carrier frequency.

Relative oscillator error is indicated by a d.c. level shift, relative to V_{bias}, in discriminator output (the MX909A's receive signal input). A simple high input impedance opamp circuit can be constructed to produce such a 'clock error' output signal from the Doc1 and Doc2 voltage levels (see Section 2.4.2, Level Acquisition and Tracking).

5. Conclusion

The MX909A provides a rich combination of features to support high performance wireless data modem designs. Using the methods described above, a choice of automatic or user defined strategies can be implemented to optimize designs and meet the needs of realistic, high performance, wireless data systems.

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APPLICATION NOTE

Increasing Data Throughput in Radio Telemetry Systems

Increasing Data Throughput in Radio Telemetry Systems

Introduction

In any data network attention must be given to the control protocol and signaling methods used in order to maximize its operational effectiveness. These issues are at least as important in radio based networks as in systems based on other transmission methods. As the use of radio-based solutions and applications increases, the pressures on the radio spectrum will become greater. High speed effective protocols and systems design will be essential features of radio data systems.

This application note will discuss factors affecting radio data network performance and present solutions based on integrated circuit technology to many of these issues. In general, it assumes the use of some form of packet data transmission rather than circuit switched data.

Increasing Data Speed

The most obvious method of increasing a network's efficiency is to maximize the data signaling speed. In nearly all types of radio-based data system, the transmission bandwidth of the data needs to be limited to fit into a licensable channel. Although some short-range systems do not suffer from extreme bandwidth limitations, this is not the case with wide-area data systems. If one assumes a working channel bandwidth of 12.5kHz at UHF, care is required to maximize the data that can be passed through this radio channel.

Two examples of appropriate methods are: Gaussian Filtered Minimum Shift Keying (GMSK) and Four Level Frequency Shift Keying (4L-FSK). As both can be implemented using traditional frequency modulation techniques, these methods are chosen as examples. While other signaling methods can provide faster transfer in a limited channel bandwidth, GMSK and 4L-FSK are effective and economic to implement in both the Baseband and RF sections of an equipment design. This is true as both modulation types can be dealt with using normal FM transmitter techniques and a traditional FM discriminator based receiver. This avoids the use of other more complex and expensive techniques such as I & Q or linear de/modulation.

i) Gaussian Filtered Minimum Shift Keying

In a GMSK system, the digital bit stream to be transmitted is passed through a Gaussian low pass filter. A Gaussian filter is a filter which when excited by an impulse outputs a Gaussian shaped output pulse. This is illustrated in Figure 1.

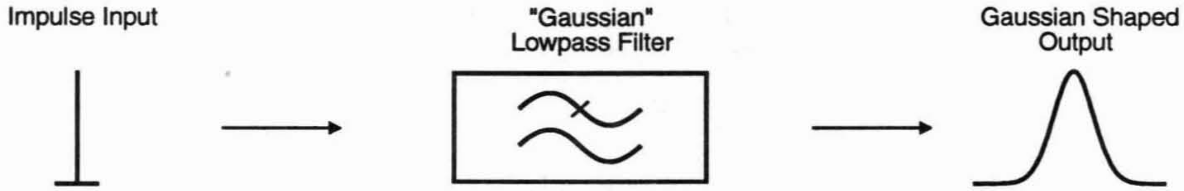

Figure 1: Gaussian Filtered Minimum Shift Keying

When a digital bit stream is passed through such a filter, a marked reduction in transmission bandwidth occurs. In an optimum GMSK system, 8000b/s should pass through a 12.5kHz FM radio channel. For a further more detailed description of GMSK, readers are referred to Reference 1. The FM deviation should also be set to be equal to one-half of the data rate. For example, an 8000b/s GMSK data signal should be transmitted with a peak deviation of 4kHz or +/- 2kHz. Within the design of a GMSK system the maximum data rate, the bandwidth employed and the bit error rate can be traded against one another. The method described here provides an approximation to true GMSK. While not in-line with the textbook definition of GMSK, it still provides a simple and effective implementation of a GMSK system.

ii) Four Level Frequency Shift Keying

In a 4L-FSK system, the digital bit stream is split into a series of bit-pairs. Each bit-pair is then coded as one of four voltage levels and passed through a low pass filter section. It has been shown that the optimum channel shape for the passing of bandwidth limited digital data is that of a Raised Cosine. Filtering should b provided at the transmitter for the purpose of transmission bandwidth reduction and at the receiver for the limitation of noise bandwidth to the data detector. This filtering optimally should have an overall Raised Cosine response. The raised cosine is normally split equally in the transmitter and receiver as two Root-Raised Cosine low pass filters. As with GMSK the precise details of the bandwidth used, the maximum speed, and the bit error rate can be offset one against the other. A simplified representation of this process shown in Figure 2.

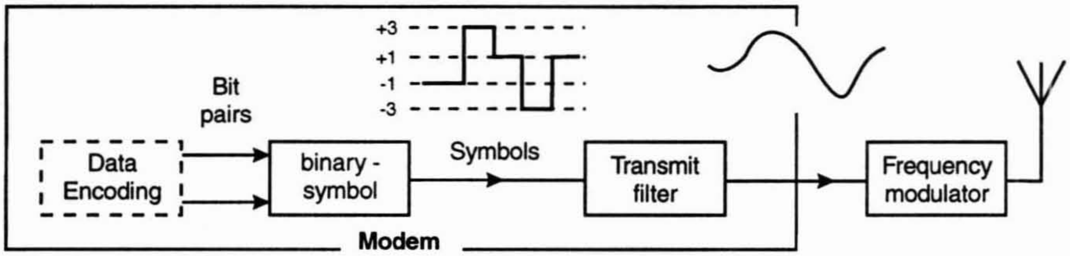

Figure 2: Four Level Frequency Shift Keying

Using 4L-FSK 9600b/s can be achieved in 12.5kHz FM channels or 19200b/s in a 25kHz channel.

Either of the two modulation methods previously described can help to maximize data throughput by allowin fast data transfer at good bit error rates while using traditional FM techniques.

Data Coding to Reduce Retries and Collision Effects

A common source of problems in a radio data network is the data unfriendly environment offered by radio transmission. Systems that detect errors during transmission and simply ask for data to be resent can suffe from excessive numbers of retries and collisions. The more retries which occur, the more likely it is that further collisions and retries will occur. This situation will become progressively worse until the throughput o the system will reduce to nearly zero. In computer networks, a TCP/IP based LAN carried over Ethernet is a example system which works on the simple retry principle. In Ethernet every station can clearly 'hear' when any other station within the LAN is transmitting; this is not the case with radio based networks. Even so, a common benchmark for indicating that a network is reaching its maximum comfortable load is 40% packet time occupancy or put another way 0.4 Erlangs traffic loading. In radio the need to reduce to a minimum packet retries is therefore imperative. Without these methods, the traffic handling capacity of a radio-based system could reduce to well below this 40% figure.

The reduction in retries can be achieved using two distinct methods: The first procedure is to reduce the number of retries, which occur due to noise and interference. The second procedure is to use a suitable channel access method such that two active stations do not corrupt each others packets by transmitting simultaneously when their coverage areas overlap.

i) Forward Error Correction

In most packet data systems, error detection is performed by the use of Cyclic Redundancy Checking (CRC However, to avoid retries the use of Forward Error Correction (FEC) is also required. In an FEC system, additional information is sent along with the data bytes to be transmitted. This additional information allows the receiving device to not only detect that errors have occurred but also to try and attempt to correct for son or all of these errors. As an example, a byte of 8-bits may be sent along with a further 4-bits of FEC information.

For example:

Bit position	0	1	2	3	4	5	6	7	8	9	10	11
Bit Description	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11

Should an error occur in either information bits b0 to b7 or FEC bits f0 to f3, the FEC system will attempt to correct for these errors. In radio systems, most bit errors will occur due to a burst of noise or interference. This will have the effect of corrupting not just one or 2 bits per byte dotted along a frame but perhaps 20 bits all together while leaving the rest of the frame intact and without errors. An FEC system such as the one shown above will not be able to cope with such a situation since all the bits in a byte and the FEC information bits may all have been corrupted thus leaving no good information to work with. The use of a technique known as interleaving overcomes this problem.

Bit interleaving works by taking a number of data bytes and their associated FEC 'nibbles' and reading them into a table. As an example, if 10 bytes were used, this would be 80 information bits plus a further 40 FEC bits, making a total of 120 bits. This 120-bit, bit stream could be read into a table of 12 rows by 10 columns row by row.

→ 000 001 002 003 004 005 006 007 008 009
010 011 012 013 014 015 016 017 018 019
020 021 022 023 024 025 026 027 028 029
030 031 032 033 034 035 036 037 038 039
040 041 042 043 044 045 046 047 048 049
050 051 052 053 054 055 056 057 058 059
060 061 ... ...
... ... 118 119

The bits are then read out of this table for transmission column by column thus in the above example the order of actual bit transmission is:

000 010 020 030 040 050 060 070 080 090 100 110 001 011 021 .... and so on.

This process is reversed in the receiving station to reconstruct the wanted data frame. The effect of this operation is that when a burst error occurs in the radio channel, it corrupts single bits spaced throughout the frame rather than blocks of bits in a single byte. Thus, the FEC process still has a good chance of being able to correct errors.

The MX-COM, Inc MX919 is an integrated circuit radio modem that includes FEC processing and bit-interleaving. The bit error rate (BER) curve in Figure 3 indicates that at S/N ratios of about 10dB a 3dB improvement in bit error rate can be achieved by additionally using FEC.

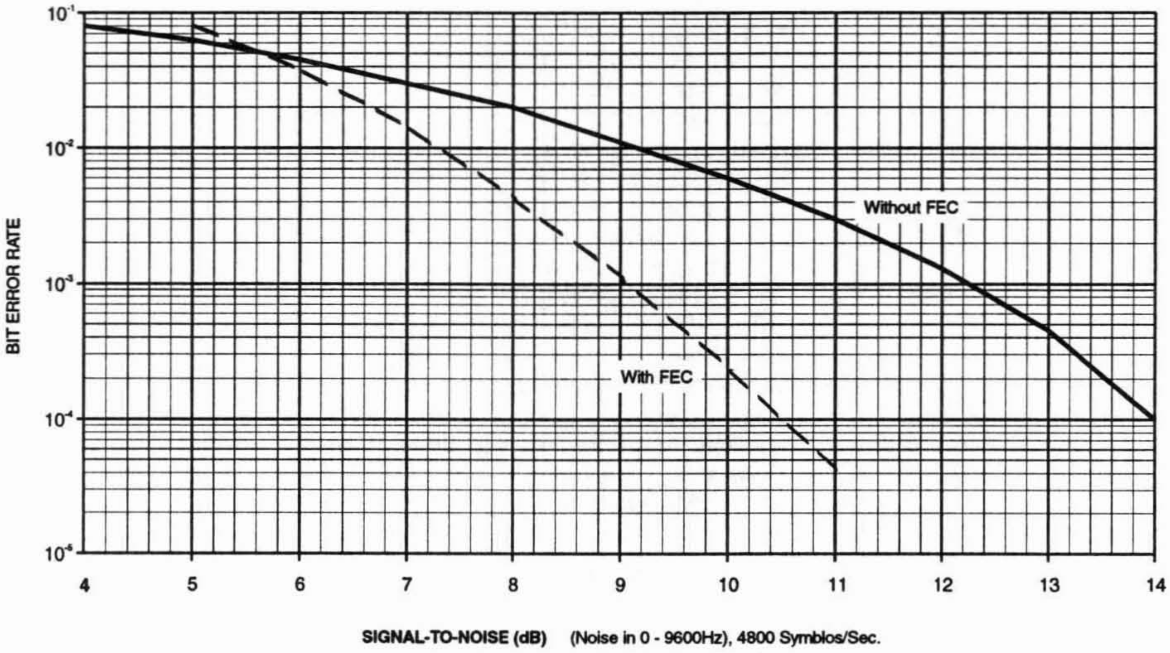

Figure 3: Bit Error Rate

It will be noted that at a S/N ratio of 5.5dB, the FEC system breaks down and the BER is worse than not using FEC.

Once a system has FEC implemented, the number of retry attempts should be limited to a small number before the station concludes that transmission is not possible. This avoids stations generating lots of retries which have no hope of success and merely serve to increase the probability of collisions and band occupancy.

ii) The effect of FEC on the frequency reuse pattern

In addition to reducing, the number of retries which occur by providing an improvement in bit error rate; FEC also has an additional benefit. To achieve a certain bit error rate at the receiver, the transmitter power may be reduced by the S/N gain provided by the FEC. In the example of the MX919, this gain is around 3dB. The transmitter power could, therefore, be reduced by 3dB to achieve an equivalent coverage area. Since the interference distance of a transmitter increases by the square of its transmitter power, this gives coverage cells with much reduced interference overlap areas. Thought of another way this can be viewed as coverage areas with much more sharply defined cell boundaries. These sharp edges to cells allow a smaller reuse distance to be used to cover a specific area and thus increase the data traffic, which can be handled by a limited number of channels over a wide area. An illustration of this effect is shown in Figure 4.

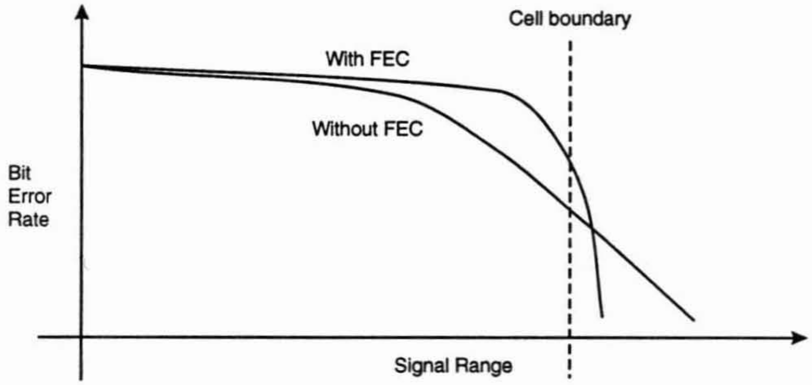

Figure 4: Bit Error Rate Effect

The use of Slotted-Digital Sense Multiple Access to avoid data collisions

As previously described, in computer networks Ethernet is widely used to interconnect computers and to provide the data transport medium. Ethernet works by each station listening to the link and not transmitting data while another station is heard to be occupying the channel. When a station does transmit data, it also listens to its own signal and attempts to determine that its signal was not corrupted by another station during its transmission. It can do this because it assumes that if it decoded its own signals OK then so must all the other stations on its LAN. This is a valid assumption when the transmission medium is a coaxial cable! This channel access method is known as Carrier Sense Multiple Access/Collision Detection or CSMA/CD. The success of CSMA/CD in avoiding collisions is very dependent on a good Data Carrier Detect (DCD) system and on being able to detect collisions effectively. In radio systems, it can never be assumed that every station can hear every other station in fact the reverse is normally the case. No station can hear every other and what is heard and what is not is subject to many different effects from propagation, noise and interference. It has been shown by the designers of the ETSI specified ‘HIPERLAN’ system, a radio-based LAN, that in a radio-based system the DCD circuit has to be sensitive to 20dB below the point where data cannot be received successfully. In the case of most systems, this would need to be around the -15dB S/N point. Such a DCD is not a practical solution. In a half or full duplex radio system, collision detection while transmitting is not possible either because the Rx is not active during Tx or because if it is it suffers extreme de-sense problems. This analysis should demonstrate that a CSMA system or a CSMA/CD system cannot be used in a radio-based data network

Various approaches to channel access can be proposed to avoid the problems discussed above. These can involve a system in which a control station polls outstations for data thus ensuring only one station is active at anytime. This will avoid collisions but may also waste airtime polling stations that have no data to send or are not able to reply for some reason. A further alternative is the system known as DAMA or Demand Allocated Multiple Access in which stations indicate to a control station that they now wish to be considered active and the control station allocates a time-slot to each active station. As the number of active stations increases, the data bandwidth allocated to each station in a set period reduces. This system is certainly much more effective than CSMA/CD and is widely used in satellite access systems where again no outstation can hear the other and there is a high risk of data collisions. However, some 'dead-time' will still occur and the efficiency will not be as high as a form of random-access or 'bandwidth-on-demand' system.

The particular method favored by the author is the so-called Slotted-Digital Sense Multiple Access S-DSMA algorithm. In S-DSMA, again a control station is used and this is assumed to be a duplex device. S-DSMA is a random access method similar to CSMA and thus avoids the 'dead-time' of polled or DAMA systems. It does also not introduce a significant amount of extra packet traffic to control its operation.

The operation is as follows:

> When the control station is transmitting data to an outstation, in addition to the information itself, it interleaves bits at regular intervals which indicate if the control stations receiver is busy or not. The control station is placed at a point in the system such that it can hear all the outstations in its cell and they only send data to it and receive data from it. The outstations are split frequency half duplex and do not transmit directly to each other. By monitoring the control stations 'receiver status bits', the outstation can determine if it is safe to transmit or not. If the control station states that its receiver is free the outstation is able to be sure that transmission can occur with a low risk of collision. In order to avoid two outstations both transmitting together when they both see the control station receiver is free, a random time delay is introduced at each outstation before transmission occurs. The delay allows one station to grab the channel before the other and the control station will then indicate that its receiver is no longer free. Thus, the second outstation must once again hold-off transmission.

By reducing the likelihood of collisions to a minimum and ensuring that only a good radio path is used for transferring data (to control station and back never from peer to peer) very high traffic loading of the channel can be achieved of the order of 75% or 0.75 Erlangs.

This effective system put together with the benefits of FEC and sharply defined cell boundaries can prove extremely effective. The Motorola mobile data system known as DataTAC^{TM}, which employs these techniques, can support around 1500 outstations per control station.

This is highlighted in Reference 2.

Simple implementation of these complex solutions

Consumer Microcircuits Limited have launched a range of integrated circuits which remove from the design of radio data networks many of the problems discussed in this paper. Known as the MX9x9 series of devices each product comes in a 24-pin Shrunk Small Outline Package and operates from a minimum supply voltage of 3.0 volts. The current consumption is of the order of 2.5mA at 3.3 volts.

Each device provides a microprocessor interface and analogue input/outputs suitable for connection to a typical FM transceiver implementation. In addition, each circuit includes packet framing, bit sync and frame sync recovery, Forward Error Correction calculation and checking, a bit de-/interleaver and Cyclic Redundancy Check calculation and checking. A data quality register is provided to enable each host microprocessor to assess the signal quality of an incoming data signal.

The devices in the MX-COM MX9x9 series have the following device specific features.

The MX909A provides a GMSK based data signaling modem in addition to the features discussed above it also includes a data randomizer to improve the performance of the GMSK system.

The MX919B provides a 4L-FSK based modem in addition to the common features of the MX9x9 range of ICs.

The MX929B provides a 4L-FSK modem and automatic handling of interleaved S-DSMA status bits in addition to the common features outlined previously.

These integrated circuits make the design of fast effective radio data networks much more easily achieved.

Conclusion

This paper has shown how the use of effective data modulation methods, forward error correction and the S-DSMA channel access technique can maximize the effectiveness of a radio data system. This allows optimum spectrum use and provides a good quality service for the users of such a system. The importance of these features can only increase as the use of radio based data systems also increases. The paper has also indicated that off-the-shelf solutions exist in the form of integrated circuits to help a system designer make full use of the methods discussed.

References:

1: MX589 GMSK Modem Application Note
(MX-COM, Inc Publication Doc. # 20830074.002)

2: The RD-LAP Air Interface Protocol
(Ronald Gerhards and Pierre Dupont, INTERCOMM 93)

MX•COM, INC. MiXed Signal ICs

APPLICATION

MSK and its Application to Wireless Data Transmission

1. Introduction

Bandwidth Efficient methods for transmission of data have been and continue to be of great importance to the data dependent community. A community that is experiencing exponential growth. Minimum Shift Keying (MSK) is a continuous phase modulation (CPM) technique that offers advantages in performance and ease of implementation. This paper will provide some insight as to how a simplified MSK modem can be implemented and modeled. The model presented is suitable for a system simulator such as *Ptolemy* from UC Berkeley.

1.1 Background

The academic field of "Data Transmission" is loaded with modulation schemes. Most involve translation of data bits or patterns into a unique combination of phase, frequency or amplitude. Some of the more notable techniques are listed in Table 1.

MODULATION TECHNIQUE	COMMON ACRONYM
Frequency Shift Keying	***FSK***
Multi-level Frequency Shift Keying	***MFSK***
Continuous Phase Frequency Shift Keying	***CPFSK***
Minimum Shift Keying	***MSK***
Gaussian Minimum Shift Keying	***GMSK***
Tamed Frequency Modulation	***TFM***
Phase Shift Keying	***PSK***
Quadrature Phase Shift Keying	***QPSK***
Differential Quadrature Phase Shift Keying	***DQPSK***
$\pi/4$ Differential Quadrature Phase Shift Keying	***$\pi/4$ DQPSK***
Quadrature Amplitude Modulation	***QAM***

Table 1: Modulation formats [6].

Each of the modulation formats listed in Table 1 is suited to a specific application. In general, schemes where two or more bits are represented by a symbol (e.g. QAM, QPSK) require better signal to noise ratios (SNR) than two-level (binary) schemes for similar bit error rate (BER) performance. Additionally, in a wireless system, schemes that have more than two levels (m-ary) generally require greater power amplifier linearity.

Most implementations of the modulation formats listed in Table 1 are synchronous. When data rates exceed 1200 bits/second or when the transmission medium is subject to non-ideal affects (e.g. fading or SNR < 25 dB) synchronous data transmission is preferred over asynchronous. Synchronous data transmission is characterized by the presence of a clock which is synchronous to the data. The clock is embedded in, and therefore recoverable from, the modulated signal. MSK is a synchronous modulation format.

Another important consideration in data transmission is bandwidth. Digitally modulated data, composed of sharp "one to zero" and "zero to one" transitions, results in a spectrum rich in harmonic content that is not well suited to RF transmission. Hence, digital modulation formats that minimize bandwidth (BW) consumption are in vogue. As implied earlier, digital modulation involves the mapping of changes in data states to changes in amplitude, frequency, phase, or some combination of the three. After smoothing the transitions (discontinuities) in phase, frequency or amplitude, we can see, through Fourier analysis, BW consumption is reduced. An entire family of modulation formats, categorized as continuous phase modulation (CPM) minimize BW consumption by eliminating phase discontinuities. CPM state changes are represented by non-abrupt changes in phase and frequency while the amplitude of the carrier envelope remains constant (i.e. phase modulation or frequency modulation).

1.2 Theory of Continuous Phase Modulation

The simplest form of constant envelope modulation is binary FSK. This type of modulation is composed of two sinusoids

$$s_1(t) = \cos \omega_1 t \tag{1}$$

and

$$s_2(t) = \cos \omega_2 t . \tag{2}$$

Where $s_1(t)$ is selected for a logic zero and $s_2(t)$ is selected for a logic one. An implementation of the this type of FSK system would appear as shown in Figure 1.

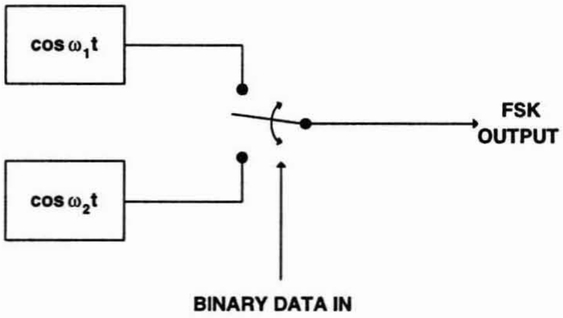

Figure 1:Discontinuous phase FSK modulator.

This type of FSK is referred to as "discontinuous phase" or "non-coherent" FSK because there is no coherence between the phase of ω_1, ω_2 and the modulating signal (BINARY DATA IN). CCITT standard V.21 (300 baud) is an example of non-coherent FSK ($f_1 = 1080$ Hz and $f_2 = 1750$ Hz) it has also been applied to other low data rate systems where bandwidth efficiency is not an issue.

An alternative method, to that depicted in Figure 1, for generating FSK is to use a voltage controlled oscillator (VCO) or frequency modulator. The key aspect of the VCO is, for instantaneous frequency deviation proportional to the modulating signal *m(t)*, the phase must be proportional to the integral of the modulating signal. In mathematical terms

$$e(t) = \mathrm{Re}\{A_C \exp[j\phi(t)]\} \tag{3}$$

where, $\phi(t) = \omega_C t + \phi_C + \psi(t)$

$e(t)$ = modulated carrier (FM is a type of angle modulation)

A_C = amplitude of unmodulated carrier

ω_C = angular frequency of unmodulated carrier

ϕ_C = initial carrier phase angle

$\psi(t)$ = instantaneous phase angle due to the modulating signal $m(t)$.

Rewriting equation (3) applying Euler's equation for exponential relations,

$$e(t) = A_C \cos[\omega_C t + \phi_C + \psi(t)] \tag{4}$$

where,

$$\psi(t) = K \int_{-\infty}^{t} m(\tau) d\tau . \tag{5}$$

Here, *m(t)* is the modulating signal and *K* is a constant of proportionality. Substituting (5) into (4) yields the equation for continuous phase FSK (CPFSK).

$$e(t) = A_C \cos[\omega_C t + \phi_C + K \int_{-\infty}^{t} m(\tau) d\tau]. \tag{6}$$

In the case where *m(t)* is bipolar (logic 1 = +1, logic 0 = -1) the integration in equation (5) can be carried out as follows. First we must have an expression which represents the bipolar data signal as shown below.

$$m(t) = \sum_{n=-\infty}^{+\infty} S_n r(t - nT) \tag{7}$$

where, $S_n = \pm 1$, according to bipolar data polarity

r(t) = rectangular pulse with amplitude *1/(2T)* and duration *T*.

Substituting (7) into (5) yields

$$\psi(t) = K \int_{-\infty}^{t} \sum_{n=-\infty}^{+\infty} S_n r(\tau - nT) d\tau \tag{8}$$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \int_{-\infty}^{t} r(\tau - nT) d\tau . \tag{9}$$

For the interval $0 \le t < T$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \int_{0}^{t} \frac{1}{2T} d\tau \tag{10}$$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \frac{1}{2T} t . \tag{11}$$

Using the result from equation (11), equation (6) can be written as

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[\omega_C t + K S_n \frac{1}{2T} t + \phi_n]. \tag{12}$$

Where, $nT \leq t < (n+1)T$ and ϕ_n is adjusted according to the phase of the previous symbol ϕ_{n-1}. As a result, if the modulating signal (NRZ binary data) has no impulses, the modulated carrier *e(t)* will not have phase discontinuities. A general representation for CPFSK modulator is shown in Figure 2.

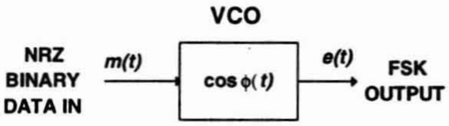

Figure 2:CPFSK generation.

Looking at the term *K* in equation (12)—referred to as a constant of proportionality earlier—for constant envelope modulation systems (e.g. FM) *K* is proportional to the peak frequency deviation of the VCO. For CPFSK, the modulation *m(t)* is NRZ data and

$$K = 2\pi f_d T \,. \tag{13}$$

Where, $f_d = |f_2 - f_1|$

T = symbol or bit period

f_1 = logic zero (S_n=-1)

f_2 = logic one (S_n=+1).

The term $f_d T$ is commonly known as the modulation index *h*. Substituting $2\pi h$ for *K* in (12) yields

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[2\pi f_C t + \frac{\pi h S_n}{T} t + \phi_n] \tag{14}$$

for, $nT \leq t < (n+1)T$.

For MSK, $h = 0.5$ so (14) can be written as

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[2\pi\left(f_C t + \frac{S_n}{4T}\right)t + \phi_n] \tag{15}$$

for, $nT \leq t < (n+1)T$.

Consequently, if S_n is *+1*, the frequency of the carrier is shifted higher to

$$f_2 = f_C + \frac{1}{4T} \,. \tag{16}$$

When S_n is *-1*, the frequency of the carrier is shifted lower to

$$f_1 = f_C - \frac{1}{4T} \,. \tag{17}$$

Subtracting (17) from (16) yields,

$$f_2 - f_1 = \frac{1}{2T} \tag{18}$$

Equation (18) states, for $h = 0.5$, the frequency separation between f_1 and f_2 is equal to half the bit rate. Figure 3illustrates a set of four waveforms for a typical MSK modulator.

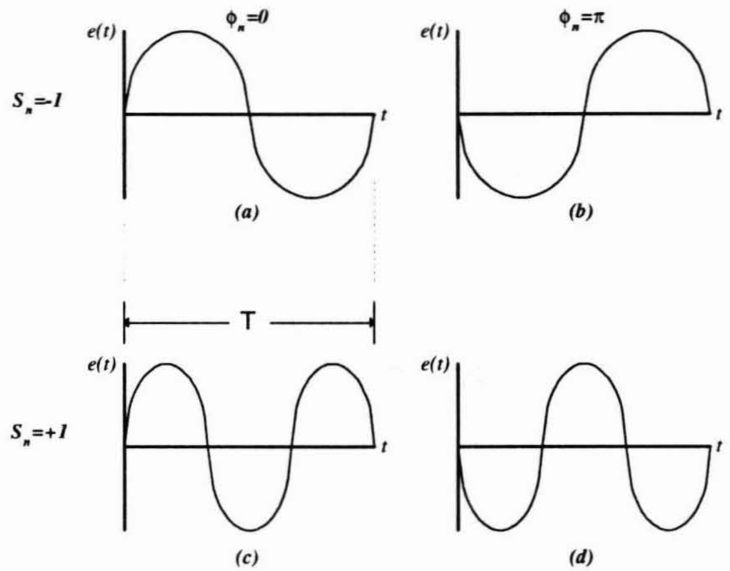

Figure 3: Typical MSK modulator outputs for (a) logic 0 and ϕ_n=0, (b) logic 0 and ϕ_n=π, (c) logic 1 and ϕ_n=0, and (b) logic 1 and ϕ_n=π.

In Figure 3 it should be noted that $e(t)$ for a logic 1 ($S_n = +1$) has only one more zero crossing than a logic 0 ($S_n = -1$). In other words, zero crossing detector must discriminate down to the occurrence of a single zero crossing in order to accurately demodulate the data signal. According to [7], a non-coherent zero crossing detection scheme will perform nearly as well as a coherent detector if the FSK signals are orthogonal. For two signals to be orthogonal over an interval T, their inner product must be zero,

$$\int_0^T x(t)y^*(t)dt = 0 \tag{19}$$

where, $y(t) \neq x(t)$ and $y^*(t)$ is the complex conjugate of $y(t)$. If $x(t)$ and $y(t)$ are real then (19) becomes

$$\int_0^T x(t)y(t)dt = 0. \tag{20}$$

For any FSK system where $\omega_1=2\pi f_1$ and $\omega_2=2\pi f_2$, equation (20) can be written as

$$\int_0^T \cos(\omega_1 t)\cos(\omega_2 t)dt = 0\,. \tag{21}$$

Performing the integration in (21) yields

$$\frac{\sin(\omega_1-\omega_2)T}{2(\omega_1-\omega_2)}+\frac{\sin(\omega_1+\omega_2)T}{2(\omega_1+\omega_2)}=0\,. \tag{22}$$

For MSK equation (18) can be rewritten in terms of radian frequency

$$\omega_1-\omega_2=\frac{\pi}{T}\,. \tag{23}$$

And the radian carrier frequency is

$$\omega_C=\frac{\omega_1+\omega_2}{2}\,. \tag{24}$$

Substituting (23) and (24) into (22) yields

$$\sin(2\omega_C T)=0\,. \tag{25}$$

Which has the solution

$$\omega_C=\frac{k\pi}{2T}\,. \tag{26}$$

Where k is an integer.

As a result, if equation (26) is satisfied, f_1 and f_2 will be orthogonal. In fact, equation (23) represents the "minimum" separation between f_1 and f_2. Hence, the name Minimum Shift Keying. This modulation scheme was first proposed by Doelz and Heald [3] which resulted in a US Patent, assigned to the Collins Radio Company. Figure 4 is a simplified block diagram for a MSK modulation system.

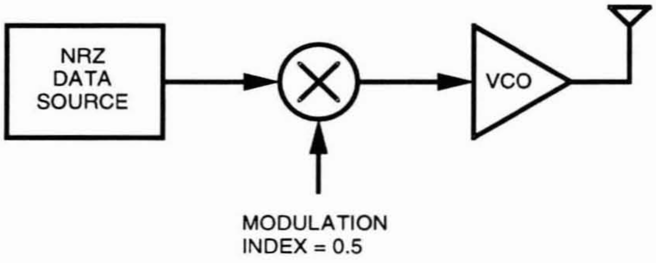

Figure 4: MSK modulator.

A modulation scheme is of little practical value if it can not be demodulated in an efficient manner. The definition of efficiency is somewhat application dependent—in general cost, size, and power consumption must be minimized while performance must be maximized. The performance of a MSK demodulator can be quantified by measurement of the signal-to-noise ratio (SNR) versus BER. SNR is considered by some as an inaccurate method for comparison of performance because of its dependence on noise BW. In other words, the SNR can be significantly altered by varying the system BW. Unless all systems have identical BW it is difficult to make comparisons. A more accepted measure of performance is E_b/N_0 versus BER. E_b/N_0 is related to SNR as shown below,

$$\frac{E_b}{N_0} = \frac{S}{RN_0} = \left(\frac{S}{N}\right)\left(\frac{B_n}{R}\right). \qquad (27)$$

Where, S = signal power

R = data rate in bits per second

N_0 = noise power spectral density (watts/Hz)

E_b = energy per bit

$B_nN_0 = N$ = noise power

B_n = noise BW of IF filter.

Figure 5 is a plot of typical performance characteristics for ideal coherent and non-coherent MSK detectors.

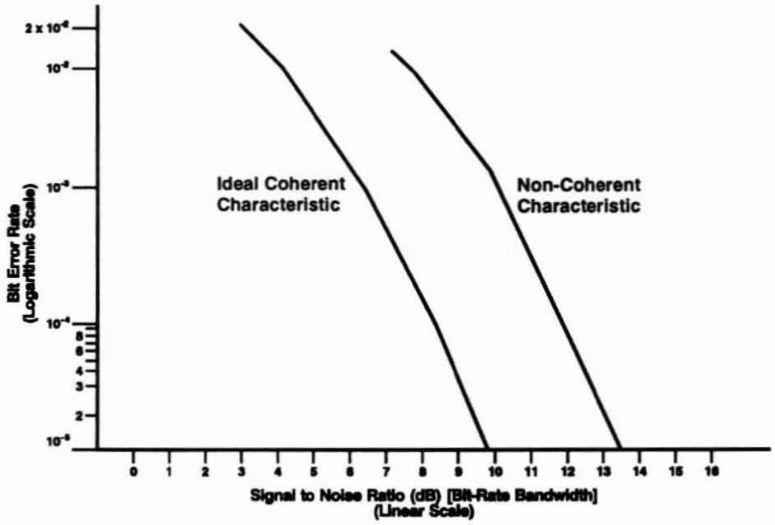

Figure 5: BER versus SNR where noise BW equals the bit rate.

2. Implementation

In this section we describe the implementation of a 1200/2400 bit/second MSK modem. That is, a MSK modulator and demodulator including carrier detection and data synchronization.

2.1 MSK modulator

Depending on selected bit rate and digital data input, the modulator generates one of the 1200 Hz, 1800 Hz, or 2400 Hz frequencies. The frequencies for different data rates and bit polarity (logic one or zero) are given in Table 2.

Baud rate (BPS)	TX data in	MSK tone frequency
1200	1	1200 Hz
1200	0	1800 Hz
2400	1	2400 Hz
2400	0	1200 HZ

Table 2: Tone frequencies for 1200/2400 bps MSK modem.

The modulator generates tones that are phase continuous and change frequency at the zero crossings as shown in Figure 6.

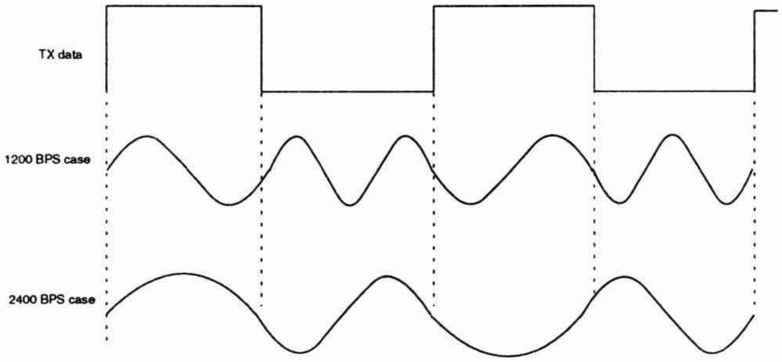

Figure 6: MSK modulator output waveforms.

The modulator block diagram is shown in Figure 7. Primarily, the modulator consists of a digitally controlled oscillator and a low pass filter. The modulation index is 0.5 and the carrier frequency is 1500Hz for 1200 baud and 1800Hz for 2400 baud case. This way of implementing the modulator is sometimes referred to as serial modulation.

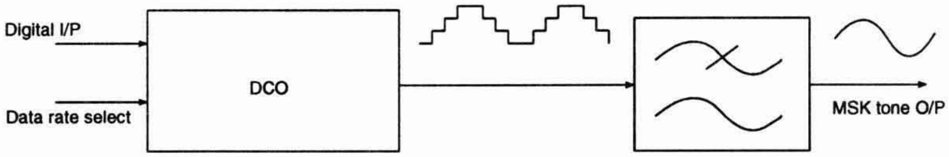

Figure 7: MSK modulator block diagram.

2.2 MSK demodulator

Demodulation is the process of converting the MSK sinusoidal signals to digital ones and zeros. Figure 8 below shows the block diagram of a non-coherent detector. The front end of this detector consists of a band pass filter whose frequency response plot looks similar to Figure 15 for 1200 bps and Figure 16 for 2400 bps. The filter output is sliced to produce a digitized form of the MSK signal, with positive half of the sine wave transformed into high going pulse and the negative half into low going pulse. The monostable is a zero crossing indicator, it produces a pulse every time the input signal changes polarity. The frequency discriminator then differentiates between the two MSK tones based on the zero crossing signal frequency. This detection scheme is non-coherent because the receiver is neither phase nor time synchronized to the transmitter.

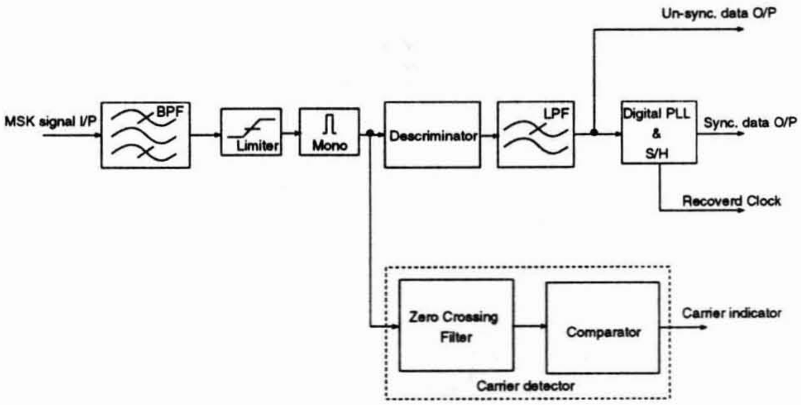
Un-sync. data O/P
MSK signal I/P
BPF
Limiter
Mono
Descriminator
LPF
Digital PLL & S/H
Sync. data O/P
Recoverd Clock
Zero Crossing Filter
Comparator
Carrier indicator
Carrier detector

Figure 8: Non-coherent MSK demodulator.

The carrier detector output indicates if MSK signal is being received. The carrier detector works off of the zero crossing indicating signal. The zero crossing filter discriminates between good and bad occurrences of the zero crossings and counts the bad zero crossing occurrences over a pre-defined period. The comparator compares the bad zero crossing count with a pre-set limit to make a decision on the carrier detector output.

The phase locked loop generates a reference clock running at the selected baud rate. The unclocked data output is sampled on the rising edge of this clock to provide synchronized data output. The period of this synchronous clock is adjusted every once per cycle if required to line up the rising edge of the clock with the middle of the unclocked data output.

2.3 Transmit and Receive Synchronization

The modulator provides a transmit reference clock to the user, this clock needs to be used to feed the digital input data to the device.

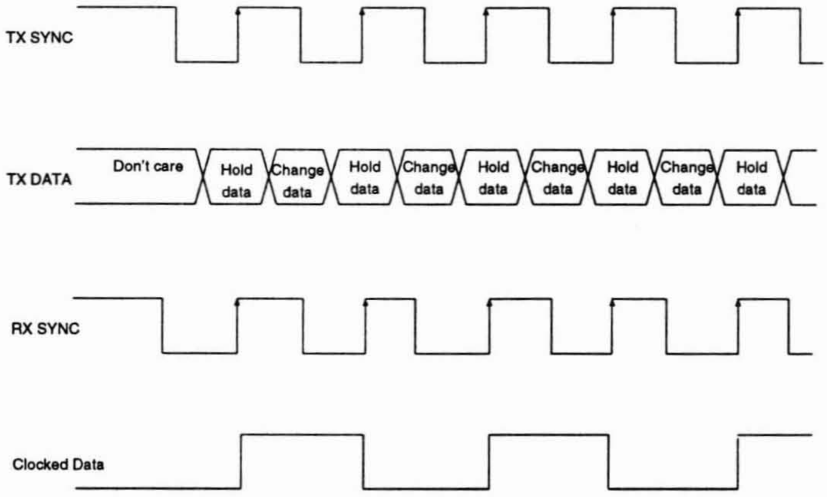
TX SYNC
TX DATA
Don't care
Hold data
Change data
Hold data
Change data
Hold data
Change data
Hold data
Change data
Hold data
RX SYNC
Clocked Data

Figure 9: Transmit and receive timing diagrams.

The de-modulator provides the recovered clock and data in reference to this clock. The timing diagrams of the TX and RX sync clocks are shown above. These two clocks can be used to enable synchronous communication between the modem and data terminal equipment.

Figure 10below illustrates an example of how the modem can communicate synchronously with any instrument that has synchronous RS-232C interface.

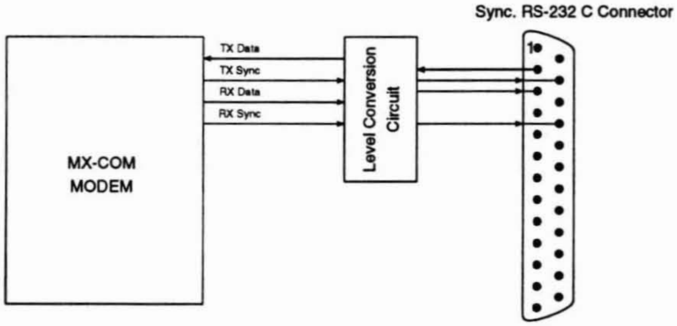
Sync. RS-232 C Connector
TX Data
TX Sync
RX Data
RX Sync
MX-COM
MODEM
Level Conversion
Circuit
1

Figure 10: Synchronous RS-232C interface.

2.4 Carrier Detector

The carrier detector is an important feature of the de-modulator. The carrier detect indicator may be used to wake-up or shut down some circuitry in the system to reduce the power consumption.

The carrier detector response time is user controllable via an external input. By altering the state of the external input the user is able to trade sensitivity for response time. In other words, the faster the response the more likely the carrier detect will false on noise and if falsing must be minimized then response time must be compromised.

3. Modeling

With increasing demand to move products quickly to market and to keep costs down, verifying a design through simulation before building a breadboard saves time and money. The rapid growth of PC based simulation tools brings modeling capability to a larger number of design engineers. The verification process can be broken down into three steps:

1. **Creating a model of the design** - Software modeling is a process of emulating hardware blocks of a design. Models can be designed on a hierarchical building block approach. The lowest level models may emulate simple hardware functions such as filters, amplifiers, or digital gates. Several lower level models can be joined together to create more complex models such as modulators or demodulators. These higher level models can be joined together to create even higher level models such as a complete communication system.
2. **Simulating the function of the model** - Simulation is the process of stimulating a model with various inputs and observing the models response. The response of the model can be recorded in plots and data files for analysis.
3. **Analyzing the plots and data collected from the simulation** - Analysis is the process of verifying the plots and data against design goals. This process helps the designer ensure correctness of or see how changes may improve the design.

The models, simulation, plots and pseudo code included in this section were derived using a modeling tool called Ptolemy. Ptolemy is a UNIX based modeling tool that has been ported to run on a PC based UNIX system called Linux. Linux and Ptolemy are freeware software packages and are available to be downloaded from several sites on the internet. One such site is *sunsite.unc.edu.* The Ptolemy home page is http://ptolemy.eecs.berkeley.edu. Other archives sites can be found using a web browser search engine. There are several other PC based modeling tools available from various software companies.

The scope of this document is to model an MSK communications scheme. Each topics will be broken up by function. The topics will include modeling MSK generation and detection (including a description of bit synchronization and carrier detection) and modeling MSK at the system level. The conclusion will review the topics and results presented in this document.

Discrete Time Models

All the models presented below are in the discrete time domain with successive samples uniformly spaced in time. The complete transmitter->channel->receiver model is a multirate system, meaning that different sampling rates are used at various stages in the model. For example the input data bits to be transmitted are sampled at the baud rate either 1200 or 2400 samples per second. The transmitter model's output sample rate is N times the baud rate. The majority of the receiver also runs at this N times rate. We typically used N=60 for the simulation results presented below. The emphasis of this section is on modeling the basic functions included in a typical serial MSK modem offered by MX-COM. RF interfaces and channel models are discussed to aid the reader in developing a complete system model however they are not fully developed. In order to simulate frequency offsets between the transmitter and receiver an interpolating/decimating block that changes the sample rate by M/N can be inserted between the transmitter and receiver. For a 0.1% frequency offset let M=1000 and N=999. For in-depth coverage of multirate processing see [2].

In the following sections, pseudo-code is provided to show the algorithm or function performed by each of the blocks in the model. The authors hope the pseudo-code will aid the readers in modeling and performing simulations of their system designs. The pseudo-code is presented in a simple manner ignoring certain programming considerations such as memory allocation, minimal buffering, type declaration, and scheduling of execution sequence. The models below focus on the core algorithm not the implementation details. Various system simulation environments such as Ptolemy have their own unique ways of dealing with these considerations which are beyond the scope of this paper.

The following conventions are used in the pseudo-code.

// starts a comment which ends at the end of the line

= assignment or comparison depending on context

+ , - , ×, / all have their normal meaning. Division is also shown as $\frac{x}{y}$ and multiplication as $x \cdot y$

Y[x] x is the index of array Y, x and Y are used here as an example - they may have any name. Inputs and outputs of each model are treated as an arrays. When referring to an input or output, increasing values of x progress forward in time. Thus Input[x-1] would refer to the previous input to the model at sample x. If a block is multirate, then it consumes more or fewer input samples than it creates output samples. For example the MSK modulator model creates N output samples for every input bit. That is upon processing Input[i], it will create Output$[N \cdot i]$, Output$[N \cdot i+1]$, Output$[N \cdot i+2]$, up to Output$[N \cdot (i+1)-1]$

F(x) function F( ) evaluated with parameter x. For example:

sin(x) is the sinusoidal function of trigonometry

cos(x) is sin(x + π/2)

sinc(x) is sin(x)/x and has the value 1 at x equal 0

sign(x) returns 1 for 0 and positive x and -1 for negative x

for i=0 to N-1 { command sequence } iterates command sequence N times with i increasing by 1 each iteration.

while (expression) { command sequence } repeats command sequence as long as expression remains true.

if (expression) { seq. 1 } else {seq. 2} executes seq. 1 if expression is true otherwise executes seq. 2.

3.1 MSK Modulation

MSK modulation is the process of converting digital data to sinusoids that represent digital data values. In MSK modulation digital data must be converted to a bipolar representation of the data. The bipolar data is then modulated with a modulation index of 0.5. The resulting frequencies are equal to the carrier frequency plus and minus one forth of the baud rate. The initial phase constant of the VCO determines whether data transitions occur at the signal peak (i.e. cos MSK) or the zero crossing (i.e. sin MSK).

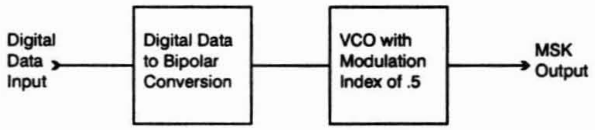
Digital Data Input
Digital Data to Bipolar Conversion
VCO with Modulation Index of .5
MSK Output

Figure 11: Typical MSK Modulator.

3.1.1 1200 Baud MSK Signals

Figure 12 shows 1200 baud MSK data modulated with a 1500 hertz carrier. MSK sine waves are continuous phase and can only start at zero for a phase constant of zero and pi radians. The first four traces show the sin MSK symbol shapes for data 1 and 0, while the fifth one shows the eye diagram. See Figure 19 for a sequence of bits at 1200 baud.

3.1.2 2400 Baud MSK Signals

Figure 13 shows 2400 baud MSK data modulated with a 1800 hertz carrier. All four symbol shapes are shown followed by the corresponding eye diagram. See Figure 20 for a sequence of bits at 2400 baud.

Pseudo-Code Listing 1 **MSK Modulation Model**

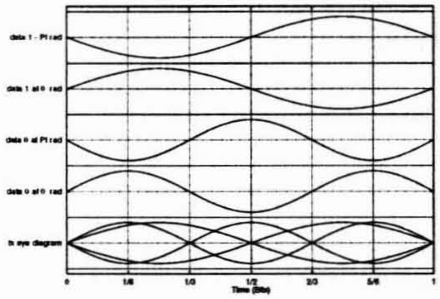

Figure 12: 1200 Baud sin MSK.

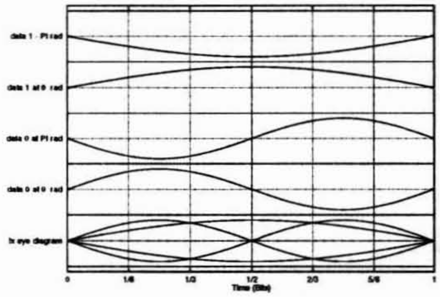

Figure 13: 2400 Baud sin MSK

I/O, Variables, and Constants

```
input[ ]       // transmit data bit array
output[ ]      // output array
N              // interpolation rate -> output sample rate = N x baud rate
2πp[i]         // phase constant in radians   0,π for sin MSK   π/2, 3π/2 for cos MSK
p[i]           // phase constant at sample i has value of  0 or  0.5
Map[0] = 1     // input data 0 mapped to bipolar data 1
Map[1] = -1    // input data 1 mapped to bipolar data -1
c              // carrier normalized to the baud rate
               // 1200 Baud Value = 1.25 = 1500(Carrier)/1200(Baud Rate)
               // 2400 Baud Value = 0.75 = 1800(Carrier)/2400(Baud Rate)
```

Pseudo-Code for MSK modulator

```
dk = Map[input(i]];                         // Map input data value (dk) for this symbol.
for n=0 to N-1 {                            // Generate N output samples per input bit
```

```
        $\text{output}[N \cdot i + n] = \sin\left(2\pi\left[\left(c + \frac{dk}{4.0}\right)\cdot\frac{n}{N} + p[i]\right]\right)$;
    }
    $p[i+1]$ = fractional remainder of $\left(p[i] + c + \frac{dk}{4.0}\right)$;        // calculate phase constant for next input bit
```

3.2 MSK Demodulation

MSK Demodulation is the process of converting Sinusoids to digital data. MSK demodulation looks for specific frequencies that represent digital data. Shown in Figure 14is a block diagram for a typical MSK demodulator. MSK demodulation can be broken down in to three sections, signal demodulation, bit synchronization and MSK carrier detection.

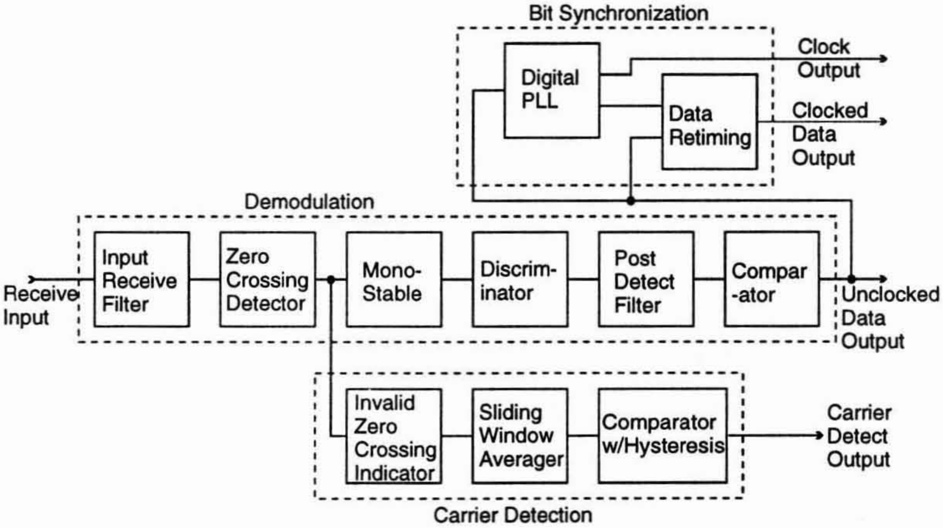
Bit Synchronization
Digital PLL
Data Retiming
Clock Output
Clocked Data Output
Demodulation
Receive Input
Input Receive Filter
Zero Crossing Detector
Mono-Stable
Discrim-inator
Post Detect Filter
Compar -ator
Unclocked Data Output
Invalid Zero Crossing Indicator
Sliding Window Averager
Comparator w/Hysteresis
Carrier Detect Output
Carrier Detection

Figure 14: MSK Demodulation Block Diagram.

3.2.1 Demodulator

The MSK detector demodulates the digital information from the received analog signal. There are six blocks that make up the detector. Each block processes the output of the previous block. The output of the sixth block is recovered digital data. The blocks are listed below and will be discussed in order of signal progression.

(a) Input Receive Filter
(b) Zero Crossing Detector
(c) Monostable
(d) Discriminator
(e) Post Discriminator Low Pass Filter
(f) Data Slicer/Comparator

3.2.1.1 RX Filter

The receiver's input filter is a band pass filter centered around the main lobe of the MSK spectrum. It is designed to have a passband width equal to the bit rate (i.e. 2100-900 = 1200Hz and 3000 - 600 = 2400Hz). The frequency domain impulse responses for both baud rates are shown below in Figure 15 and Figure 16. These graphs show the magnitude responses of linear phase finite impulse response (FIR) filters. The filter weights are based on a windowed difference of sinc( ) functions such as:

$$\left[\operatorname{sinc}\left(\frac{2\pi \cdot f_H \cdot t}{f_S}\right) - \operatorname{sinc}\left(\frac{2\pi \cdot f_L \cdot t}{f_S}\right)\right] \cdot \text{window\_ function}(t) \qquad (28)$$

where:

f_H is the upper cutoff frequency of the bandpass filter

f_L is the lower cutoff frequency of the bandpass filter

f_S is the sampling frequency of the bandpass filter

Most system simulation packages include tools for generating filter coefficients based on spectral templates, thus coefficients are not tabulated. If an infinite impulse response (IIR) filter is used then it should be group delay equalized over the passband. See section 3.4 for a simple model of an FIR filter.

For thorough coverage of digital filters refer to a digital signal processing text book such as [2],[5] or [8].

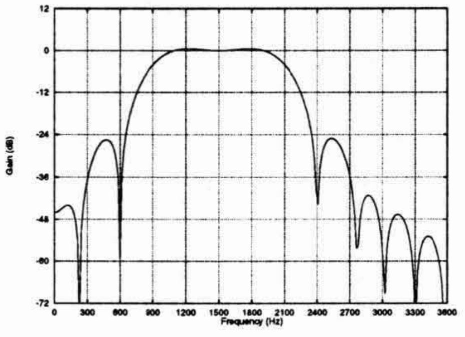

Figure 15: Rx 1200 Baud Filter.

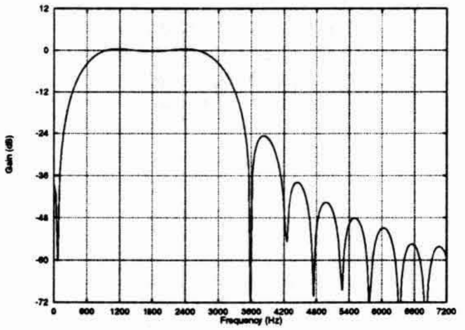

Figure 16: Rx 2400 Baud Filter.

3.2.1.2 Zero Crossing Detector

The zero crossing detector monitors the incoming sinusoid signal from the RX input filter at a rate of N samples per symbol. When the signal passes through zero the output is pulsed high for one sample period. The zero crossing detector then monitors for the next zero crossing.

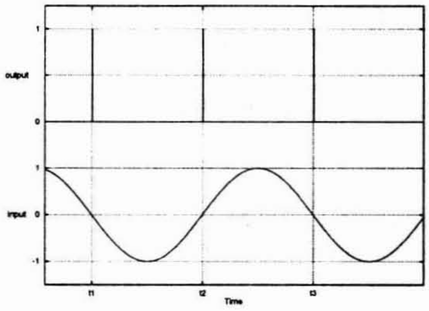

Figure 17:Plot of Zero Crossing Function.

Pseudo-Code Listing 2 **Zero Crossing Detector**

I/O

input[i] = current input sample

output[i] = current output sample

Pseudo Code

```
if sign(input[i]) != sign(input[i-1])
    output[i] = 1;
else
    output[i] = 0;
```

3.2.1.3 Monostable

The monostable monitors the pulsed output signal from the zero crossing detector. When a pulse is detected the output of the monostable is set high and the timer is restarted. The value of the timer is set to 1/3 a symbol time for 1200 baud and 1/2 symbol for 2400 baud. When the time-out period of the monostable expires the output is set low. If a new pulse is detected on the input before the timer has expired, the timer is restarted and the output remains high. Figure 18 shows the function of the monostable.

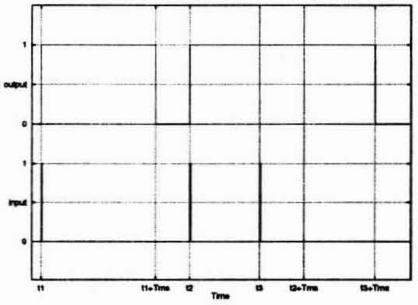

Figure 18: Plot of Monostable Function.

Pseudo-Code Listing 3 Monostable Model

```
I/O, Variables, and Constants

    input[i]            // Current input sample
    output[i]           // Current output sample
    $T_{ms}$ = N/3      // 1/3 Bit time @ 1200 Baud
    $T_{ms}$ = N/2      // 1/2 Bit time @ 2400 Baud
    timer = 0           // initialize timer first time
```

```
Pseudo Code for Monostable

    if input[i] = 1     then    timer = $T_{ms}$;
    if  timer > 0       then    output[i] = 1;
                        else    output[i] = 0;
    if timer > 0        then    decrement timer;
```

3.2.1.4 Discriminator

The discriminator uses the output signal of the monostable to reconstruct the digital information. In Figure 19 and Figure 20, the operation of the discriminator is displayed. The signals in these figures are under perfect conditions without passing through the receive filter. Under more realistic conditions the output the discriminator looks much less perfect and hence needs to pass through the Post Discriminator Filter to look more like the transmitted bits. See the discriminator output trace in Figure 31 to understand the need for the low pass filter.

3.2.1.4.1 1200 Baud Case

In Figure 19, the TX data in signal is included as a reference to the digital data being decoded. The TX MSK out signal is the modulated signal that is applied to the zero crossing detector. As seen in this signal, a data bit one has 2 zero crossings while a data bit zero has 3 zero crossings per bit time. The monostable output signal is the input to the discriminator. (Refer to the monostable for an explanation of it's output signal). The input signal to the discriminator is time shifted to create two additional signals. The first is shifted by one sixth of a bit time and the second is shifted by one third. These three signal are logically NANDed together to produce the discriminator's output signal. For a logic one the zero crossings are spaced such that the output of the monostable is low for one sixth of a bit time before the middle of the bit and again before the end of the bit. The logical NANDing of the three signals creates a pulse width equal to one half of the bit period for each of the two zero crossings in a logic one. This creates a digital one with the appropriate bit timing. For the zero bit, the zero crossings keep the monostable output high so the NAND output stays low.

3.2.1.4.2 2400 Baud Case

In Figure 20, the TX data in signal is included as a reference to the digital data being decoded. The TX MSK out signal is the transmitted signal for which the discriminator is decoding. As seen in this signal, a data bit with the value of one has 1 zero crossings and a data bit with the value of zero has 2 zero crossings per bit time. The monostable output signal is the input to the discriminator. The input signal to the discriminator is time shifted by one half of a bit period and is logically NANDed with the input. The logical NANDing of the two signals creates the proper bit period. For a zero, the zero crossings keep the monostable output high so the output of the NAND stays low.

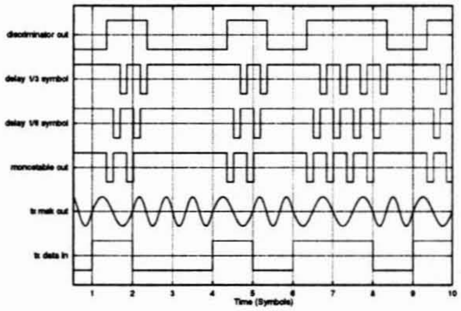

Figure 19:1200 Baud Discriminator Signals.

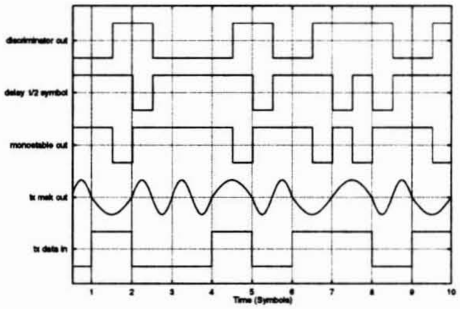

Figure 20: 2400 Baud Discriminator Signals.

Pseudo-Code Listing 4 Discriminator Model

```
I/O, Variables and Constants

    input[i]                         // current input sample
    output[i]                        // current output sample
    Taps[]       = {0, N/6, N/3}     //1200 Baud
                 = {0, N/2}          // 2400 Baud
    state                            // variable used to compute logical And of delayed inputs
```

```
Pseudo Code for Discriminator        // runs at N x baud rate

    state = 1                        // initialize to true for each input sample.
    for x = 0 to size of Taps-1
        state = state & input[i - Taps[x]]          // compute logical And of each delayed input

    output[0] = complemented value of state         // logical Invert
```

3.2.1.5 Discriminator Low Pass Filter

The discriminator low pass filter is designed to pass frequencies up to half the bit rate. This corresponds to the highest frequency needed to pass an NRZ data sequence 101010... As seen in spectral plots in Figure 21 and Figure 22, the discriminator low pass filter rolls off sharply beyond its cutoff to remove high frequency noise out of the discriminator. These plots depict a finite impulse response filter with weights of a windowed sinc( ) function. See section 3.4 for a finite impulse response filter model.

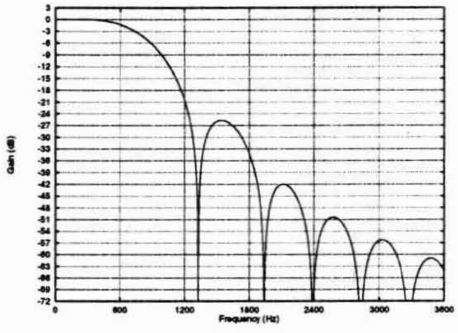

Figure 21: 1200 Baud LPF.

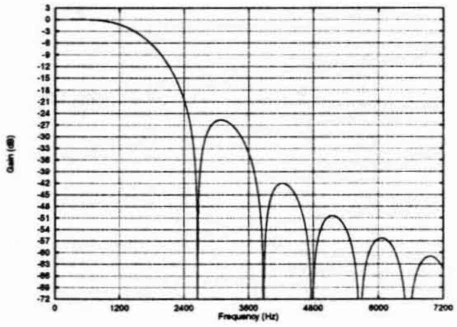

Figure 22: 2400 Baud LPF.

3.2.1.6 Bit Slicer

The bit slicer is simply a comparator with a threshold half way between a one and a zero. That is it outputs 1 for inputs greater than 0.5 and output 0 for inputs less than 0.5. Section 3.4 shows pseudo-code for a comparator. That model provides for hysterisis; however for use as a bit slicer both the upper and lower threshold can be set to 0.5 to essentially eliminate the hysterisis.

3.2.2 MSK Carrier Detection

The carrier detector is made up of three blocks, the bad zero crossing detector, sliding window filter and Comparator with hysterisis. The carrier detect section monitors the information out of the zero crossing detector to determine whether the zero crossing are timed properly for a 1200 or 2400 baud MSK signal. If the zero crossings are properly spaced a logic level is output to indicate that a valid MSK signal is being received.

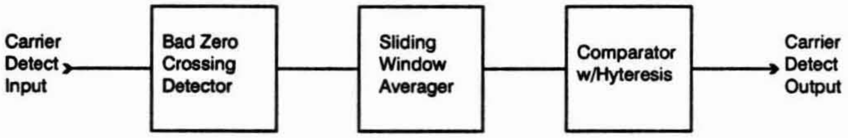

Figure 23: Carrier Detect Block Diagram.

3.2.2.1 Bad Zero Crossing Detector

The Bad Zero Crossing Detector monitors the zero crossings of the filtered input signal. The time between zero crossings is compared against a referenced. If the Bad Zero Crossing Detector determines that a zero crossing is not properly time spaced the output pulses high, otherwise the output remains low. Figure 24 and Figure 26 show the timing windows used for 1200 and 2400 baud. Figure 25 and Figure 27 show that with a properly timed input signal (i.e. zero crossings within the window) the output is low. With an improperly timed input (i.e. zero crossing outside the window or end of window reached) the output pulses high. The windows are based on the ideal zero crossing spacings +/- 5% of the bit time. Thus each baud rate would have two valid windows, however the receive input filter introduces a slight intersymbol interference at symbol boundaries and thus the windows need to widen towards each other to account for this. Since the windows of the 1200 Baud case become very close, a single window is used.

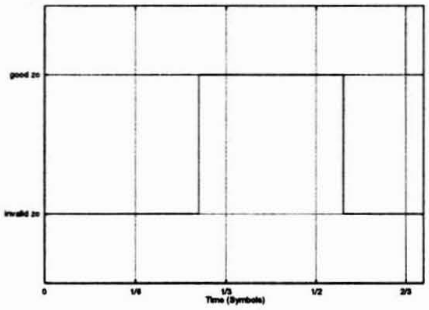

Figure 24: 1200 Baud Valid Zero Crossing Window

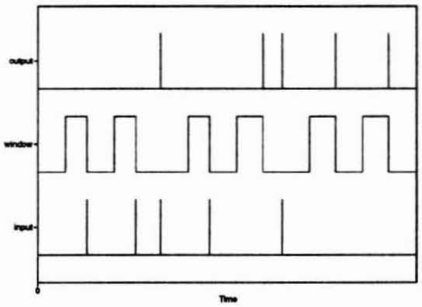

Figure 25: 1200 Baud Bad Zero Crossing Detector.

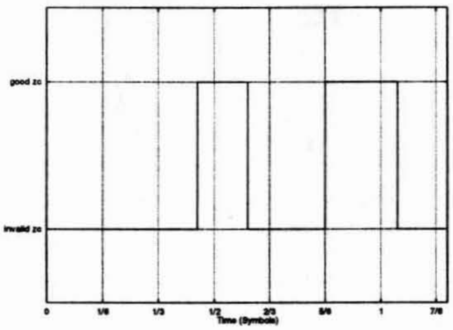

Figure 26: 2400 Baud Valid Zero Crossing Window.

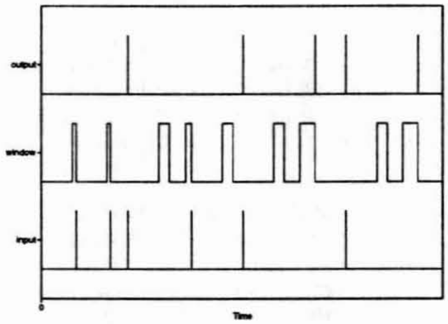

Figure 27: 2400 Baud Bad Zero Crossing Detector.

Pseudo-Code Listing 5 Bad Zero Crossing Detector

```
I/O, Variables and Constants
    input[i]                // current input sample
    output[i]               // current output sample
    START                   // Array of valid-window START times
        {Nx0.2833}                  // 1200 baud - one window
        {Nx0.45, Nx0.8}             // 2400 baud - two windows
    STOP                    // Array of valid-window STOP times
        {Nx0.55}                    // 1200 baud - one window
        {Nx0.6, Nx1.05}             // 2400 baud - two windows
    counter                 // used to keep track of time since last zero crossing occurred
    OK                      // flag used to indicate properly timed zero crossing
```

Pseudo-Code for Bad Zero Crossing Detector

```
OK = TRUE;                                   // flag defaults TRUE for no zero crossing input
if (input[i] = 1) {                          // if zero crossing occurs this sample
    OK = FALSE;                              // then flag defaults FALSE and window is checked
    for j=0 to size of STOP and START arrays                  // loop over all valid-windows
            if ((counter >= START[i]) & (counter <= STOP[i])) // check if counter is in window
                    then  OK = TRUE;                          // set flag TRUE if in window
    reset counter;                           // counter is reset at every zero crossing
    }
if (counter > max. value in STOP array)
    then    { OK = FALSE; reset counter; }   // window expired -> spacing is too large for MSK
    else    increment counter;
output[i] =  logic inverse of  OK;           // output pulses high for bad zero crossings
```

3.2.2.2 Carrier Detect Sliding Window Filter

The sliding window filter maintains a count of the number of bad zero crossings within the last L samples. It can be modeled as a finite impulse response filter of length L with all coefficients set to 1. See section 3.4 for pseudo-code of a finite impulse response filter. To mimic response time of MX-COM's serial MSK modems the length of the window should be eight symbols so L=N x 8 where N is the number of samples per symbol.

3.2.2.3 Carrier Detect Comparator

The carrier detect comparator monitors the output of the sliding window filter to determine if the zero crossing spacings are consistent enough to look like MSK. It has hysterisis to prevent chattering in noisy conditions. The comparator's upper threshold is set to five while its lower threshold is set to one. Thus, it trips to the detect state when there are no bad zero crossings in the last L samples and trips to the non-detect state when there are more than five. Section 3.4 shows pseudo-code for a comparator with hysterisis. That models output should be inverted to have an active high MSK carrier detect.

3.2.3 Bit Synchronization

The Bit Synchronization section re-times the data from the demodulation section. There are two blocks in this section, the Phase Lock Loop block (PLL) and the re-timing block. The PLL creates the clock that is used to re-time the data.

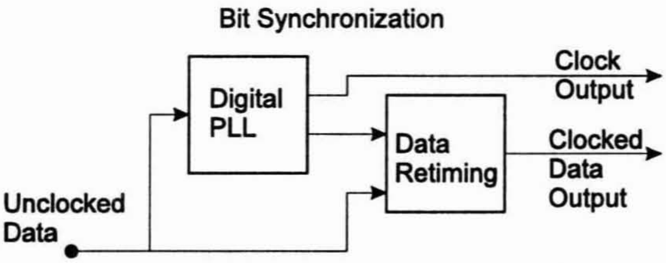

Figure 28: Bit Synchronization Block Diagram.

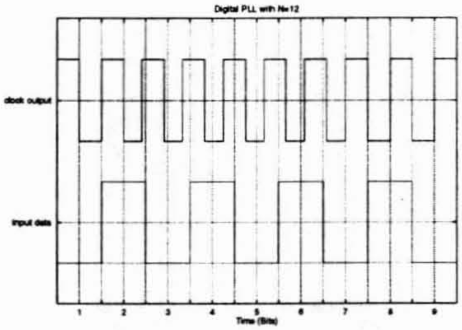

Figure 29: Bit Synchronization Plot.

3.2.3.1 Digital Phase Lock Loop

The PLL aligns the output clock rising edge to the middle of the input NRZ data bit. When the PLL is not aligned with the incoming data a correction factor is applied to the PLL clock period until it becomes synchronized with the incoming data. As seen in Figure 29 the output clock starts out of phase with the data and it becomes synchronized by the end of the plot. In Figure 29 the correction factor used is one 12th of a bit period to more clearly show the locking process

Pseudo-Code Listing 6 Digital PLL

I/O, Variables and Constants

input[i]	// current input sample; input is NRZ data
output[i]	// current output sample; output is clock which locks to NRZ data changes
X	// the correction factor (Note: for MX-COM MSK modems X = 5% bit time)
N	// number of samples per symbol
early	// flag set TRUE if data transition is early
late	// flag set TRUE is data transition is late
counter	// a general counter
reset	// flag set TRUE when algorithm determines it is time to reset counter

---

Pseudo Code for First Order Digital PLL

```
reset = 0;
if  counter<N/2-(0.5X) and input[0] not equal to input[1]        // set early flag
    then    early = 1;
if counter>N/2+(0.5X ) and input[0] not equal to input[1]        // set late flag
    then    late = 1;
if counter is equal to N - 1 - X and early and NOT late          // apply correction factor
    then    reset = 1;                                           //        by resetting early
if counter is N-1 and NOT early and NOT late                     // apply no correction
    then    reset = 1;                                           //        by resetting on time
if counter is N-1 and early and late                             // reset on time since flags conflict
    then    reset = 1;
if counter is equal to N - 1+ X                                  // apply correction factor
    then    reset = 1;                                           //        by resetting late
if counter > N/2                      // set output clock phase based on counter state
    then    output = 0;
```

```
        else     output = 1;
    if reset is equal to 1 then {              // reset flag is true then reset counter and early and late flags
        counter = 0;
        late = 0;
        early = 0;
        }
        else increment counter;
```

3.2.3.2 Data Re-timing

The date re-timing block aligns the data to the clock recovered by the PLL. The most common solution is a D flip-flop. The data is applied to the D input of the flip-flop and the PLL output clocks the data through the flip-flop. A model of a D flip-flop is shown in section 3.4.

3.3 System Simulations

Figure 30 shows an MSK system consisting of a transmitter, noisy channel, and a receiver. By simulating a complete system with the models defined above, various signals are plotted in Figure 31. The transmit data bits have a 16 bit preamble for bit synchronization. The receive filter output shows how noise degrades the band limited MSK signal. This degradation is more clearly seen in the receive filter eye diagrams, Figure 32 and Figure 33. The discriminator output clearly shows the need for the post discriminator low pass filter. The unclocked output exhibits jitter (i.e. variable length bit duration) and shows the need for sampling it in the middle of the bit to reliably recover it. The clocked data output shows relatively little jitter in the re-timed data. Additionally the carrier detect output and internal signals are shown to help the reader understand their function. While the transmitter is not enabled many bad zero crossings are indicated. These keep the sliding window filter output from going below the carrier detect threshold. After the start of transmission few bad zero crossings are seen and the carrier detect output trips high when the sliding window filter output goes below the threshold.

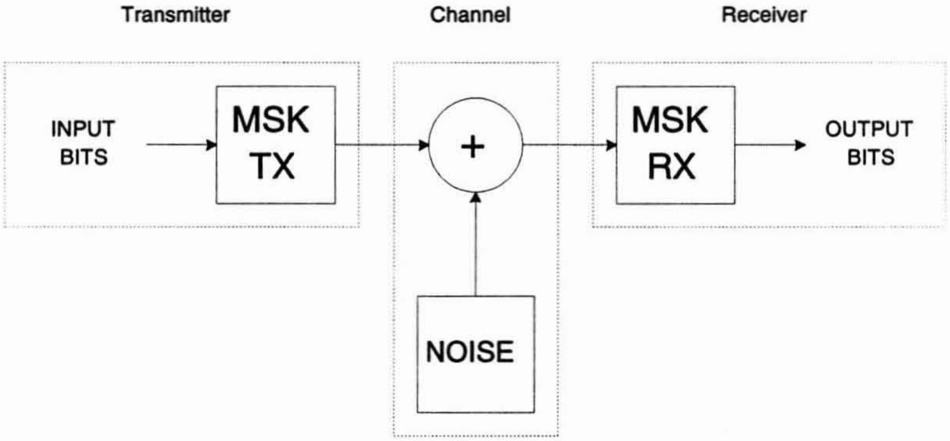

Figure 30: MSK Communications System with Noisy Channel.

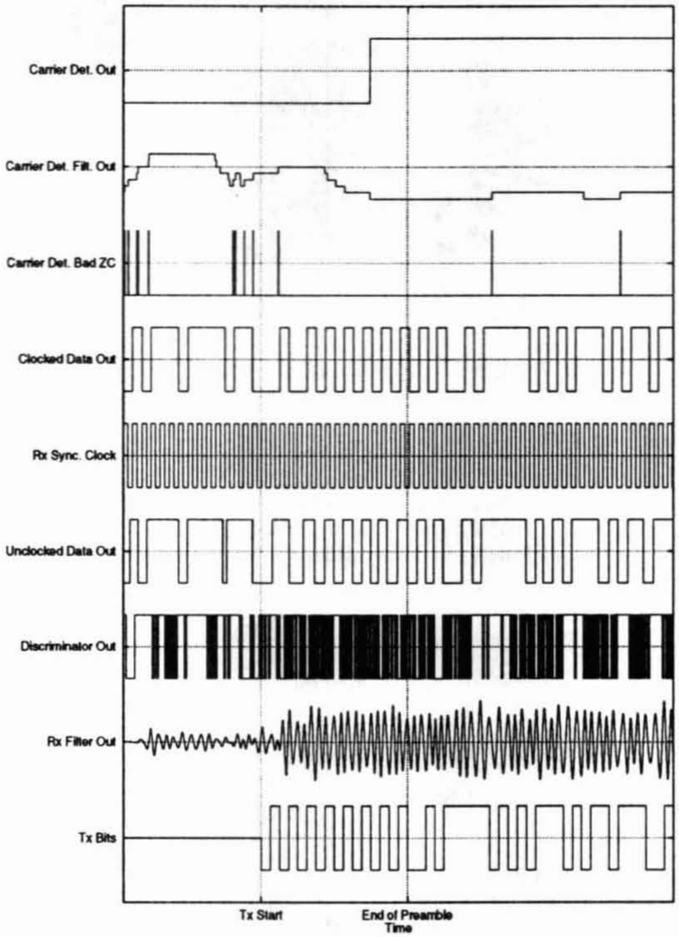

Figure 31: System Simulation Signals for 1200 baud at 12dB SNR

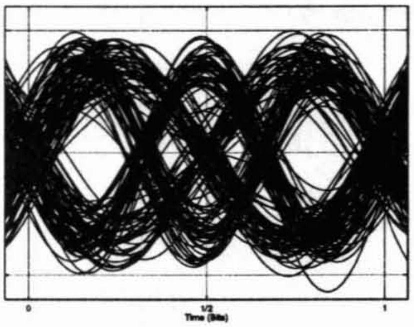

Figure 32: RX Eye Diagram for 1200 Baud at 12dB SNR.

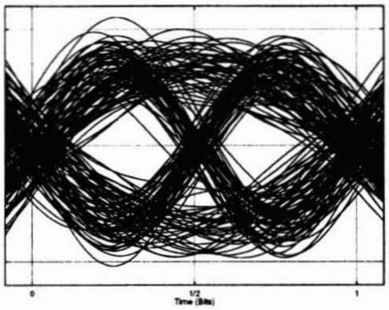

Figure 33: RX Eye Diagram for 2400 Baud at 12dB SNR.

3.3.1 MSK Simulations with various SNR

Figure 34 shows the simulated bit error rate performance of the system depicted in Figure 30. The channel is assumed to be additive white gaussian noise (AWGN). In the simulations the noise source produces white noise from DC to half the sampling rate. Thus the total noise power is much higher than the noise in the bit rate bandwidth. Equation (29) computes an effective SNR from a measured SNR assuming white noise over the measurement bandwidth.

$$\mathrm{SNR}_{\mathrm{Eff}} = \mathrm{SNR}_{\mathrm{Meas}} + 10\log\frac{\mathrm{BW}_{\mathrm{Meas}}}{\mathrm{BW}_{\mathrm{BitRate}}} \tag{29}$$

which can be rearranged as:

$$\mathrm{SNR}_{\mathrm{Meas}} = \mathrm{SNR}_{\mathrm{Eff}} - 10\log\frac{\mathrm{BW}_{\mathrm{Meas}}}{\mathrm{BW}_{\mathrm{BitRate}}} \tag{30}$$

To adjust the effective SNR to 12dB assuming:

AWGN source is a random variable with zero mean and variance = $\sigma^2 = 1$ i.e. dB power = 0dB.

MSK peak signal level = 1 i.e. signal power = 20log(RMS voltage level) = $20\log\left(\frac{1}{\sqrt{2}}\right)$ = -3dB

and a sampling rate 60 times the baud rate i.e. $\mathrm{BW}_{\mathrm{Meas}}$ = 30 times the baud rate

$$\text{Correction Factor} = 10\log\frac{\mathrm{BW}_{\mathrm{Meas}}}{\mathrm{BW}_{\mathrm{BitRate}}} = 10\log\frac{30}{1} = 14.77\mathrm{dB}$$

thus $\mathrm{SNR}_{\mathrm{Meas}}$ = 12dB - 14.77dB = -2.77dB

The SNR without adjusting noise power level is:

$$\mathrm{SNR}_{\mathrm{Meas}} = 10\log\frac{\text{Signal Power}}{\text{Noise Power}} = -3\mathrm{dB}$$

so it is necessary to decrease the noise power by 0.23 dB so:

$$\text{noise variance} = 10^{\frac{-0.23}{10}} = 0.9484$$

to arrive at other effective SNR we can simply adjust the noise variance by a scale factor:

$$\text{scale factor} = 10^{\frac{12-SNR}{10}}$$

The table below shows the required noise variance for SNR near 12dB with the system sampling rate equal to 60 x baud rate.

Effective SNR (dB)	Noise Variance	Scale factor from reference .
13	0.753	0.794 = 1/1.259
12	0.948	1 i.e. 12dB is reference
11	1.194	1.259
10	1.503	$1.585 = (1.259)^2$

Table 3: Noise variance for various effective SNR.

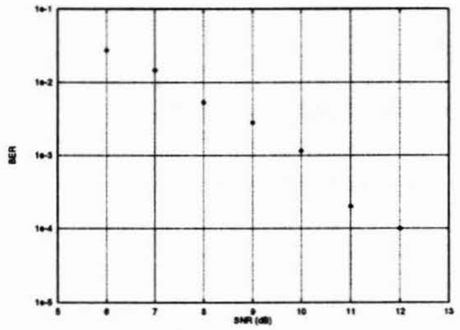

Figure 34: Simulated Bit Error Rate Performance.

3.3.2 FM System

Because of the relatively narrow bandwidth required by MSK, it can often be transmitted over existing analog radio links with little or no modification. Figure 35 is a block diagram of FM transmission of MSK. Pseudo-code models for the key blocks of this system are shown below.

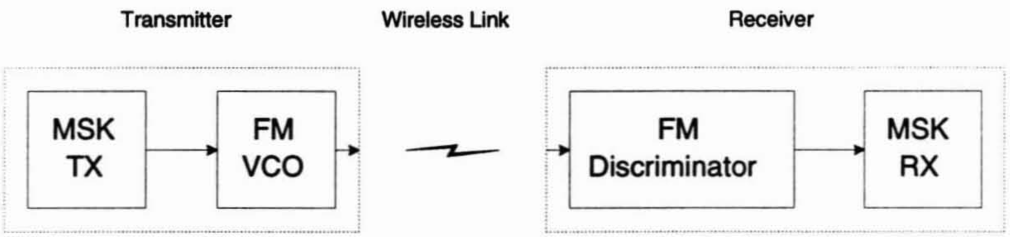

Figure 35: FM Block Diagram.

3.3.2.1 FM modulation model

Pseudo-Code Listing 7 VCO based FM modulator model

```
I/O, Variables and Constants
    input[ ]       // input sequence
    output[ ]      // output sequence
    IntIn = 0      // variable used to store integral of input[] sequence up to current time.
    step           // difference between consecutive input samples normalized to interpolation rate M.
    carrier        // FM carrier frequency normalized to interpolation rate M
    deviation      // FM deviation frequency normalized to carrier frequency.
    $\omega_c = \frac{2\pi \cdot \text{carrier}}{M}$                          // carrier frequency constant
    $\omega_d = \frac{2\pi \cdot \text{carrier} \cdot \text{deviation}}{M}$   // deviation frequency constant

PSEUDO-CODE        // run for each sample, output sample rate is
                   // M times input sample rate
                   // use linear interpolation between input samples

    $\text{step} = \frac{\text{input[i]} - \text{input[i - 1]}}{M}$;
    for j=0 to M-1 {
        IntIn = IntIn + input[i-1] + $\text{step} \cdot j$;          // simple integrator
        output[M · i + j] = $\sin(\omega_c \cdot (i \cdot M + j) + \omega_d \cdot \text{IntIn})$;
        }
```

3.3.2.2 FM Discriminator Model

A simple heterodyne discriminator model based on Figure 35 can be built with multipliers, delays and filters. Pseudo-code is shown for the mixer and the discriminator.

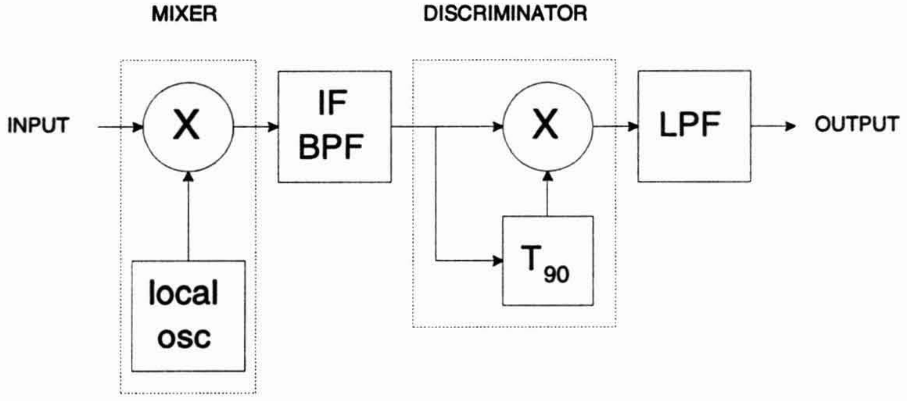

Figure 36: Heterodyne Discriminator Block Diagram.

Pseudo-Code Listing 8 Mixer

I/O, VARIABLES and CONSTANTS

```
RFinput[i]          // RF input
IFoutput[i]         // IF output
                    // local oscillator frequency normalized to sampling rate of block
$\omega_c = \frac{2\pi \cdot f_c}{f_s}$   // note $f_c$ is offset from the RF carrier by the IF frequency.
```

PSEUDO-CODE   for MIXER

```
IFoutput[i] = RFinput[i] × sin($\omega_c$ × i);
```

Pseudo-Code Listing 9 FM Discriminator

I/O, VARIABLES and CONSTANTS

```
IFinput[i]          // input to discriminator
DSoutput[i]         // discriminator output
$T_{90}$                 // Delay equal to one quarter of the IF center frequency
```

PSEUDO-CODE   for DISCRIMINATOR

```
DSoutput[i] = IFinput[i] × IFinput[i - $T_{90}$];
```

3.4 General Purpose Models

This section list various general purpose models which the authors hope are self explanatory.

Pseudo-Code Listing 10 Finite Impulse Response Filter Model

I/O, VARIABLES and CONSTANTS

```
input[i]            // current input sample
output[i]           // current output sample
L                   // FIR filter order
j                   // index to previous samples
sum                 // used to accumulate tap x weight products
weights[0..L-1]     // array of filter coefficients
```

PSEUDO-CODE // run for each sample, input and output sample rates are equal

```
sum = 0
j = 0
while j<L {
    sum = sum + (input[i-j] x weights[j]);
    increment j;
    }
output[i] = sum;
```

Pseudo-Code Listing 11 Comparator with Hysterisis

I/O, VARIABLES and CONSTANTS

```
input[i]        // current input sample
output[i]       // current output sample
Hth             // upper threshold
Lth             // lower threshold
```

PSEUDO-CODE // run for each sample, input and output sample rates are equal

```
if (input[i] > Hth)                    // output trips high
    then output[i] = 1
    else if (input[i] < Lth)           // output trips low
            then output[i] = 0
            else output[i] = output[i-1]// output stays same as last output
```

Pseudo-Code Listing 12 D type flip-flop

I/O, Variables, and Constants

```
D[i]      // current input sample
C[i]      //  clock input
Q[i]      // current output sample
state     // used to store sampled
```

Pseudo-Code

```
if (C[i] = 1) & (C[i-1] = 0)       // rising edge of clock input
    then state = D[i];             // sample input
```

```
Q[i] = state;                    // output state
```

3.5 References

[1] J.B. Anderson, T. Aulin and Carl-Erik Sundberg, *Digital Phase Modulation*, Plenum Press, New York, NY, 1986.

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MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Using an MX469 MSK SynchronousModem with an Asynchronous Data I/O

1. Asynchronous Modem Circuitry

This application note, used with current MX469 product information, outlines the construction of a low-cost asynchronous modem for the transmission of RS-232 data in the form of Minimum Shift Keying (MSK), between terminals by a radio or line medium.

The modem circuitry shown in Figure 1 accepts asynchronous data while transmitting synchronous data using the MX469 series modem. The MX469 may be used to transmit data at either 1200 or 2400bps, depending on the setting of Switch 1 shown in Figure 1. The chart below details the devices used in this application.

Performance Requirement	Associated Circuitry
RS-232 Driver/Receiver Level Translator	Maxim MAX-232
Async to Sync	Sipex MAS7838
Sync to Async Conversion	
Data Carrier Detection	MX-COM MX469
Controlled RTS/CTS Delay	74HC04 Delay Element
Generation of MSK Signals	MX-COM MX469
Reception of MSK Signals	MX-COM MX469
Interface into Radio System	MX-COM MX469
RS-232 Handshake	Misc. Circuitry

The signals required for an RS-232 handshake for asynchronous data are as follows. A complete definition of each is given at the end of this application note.

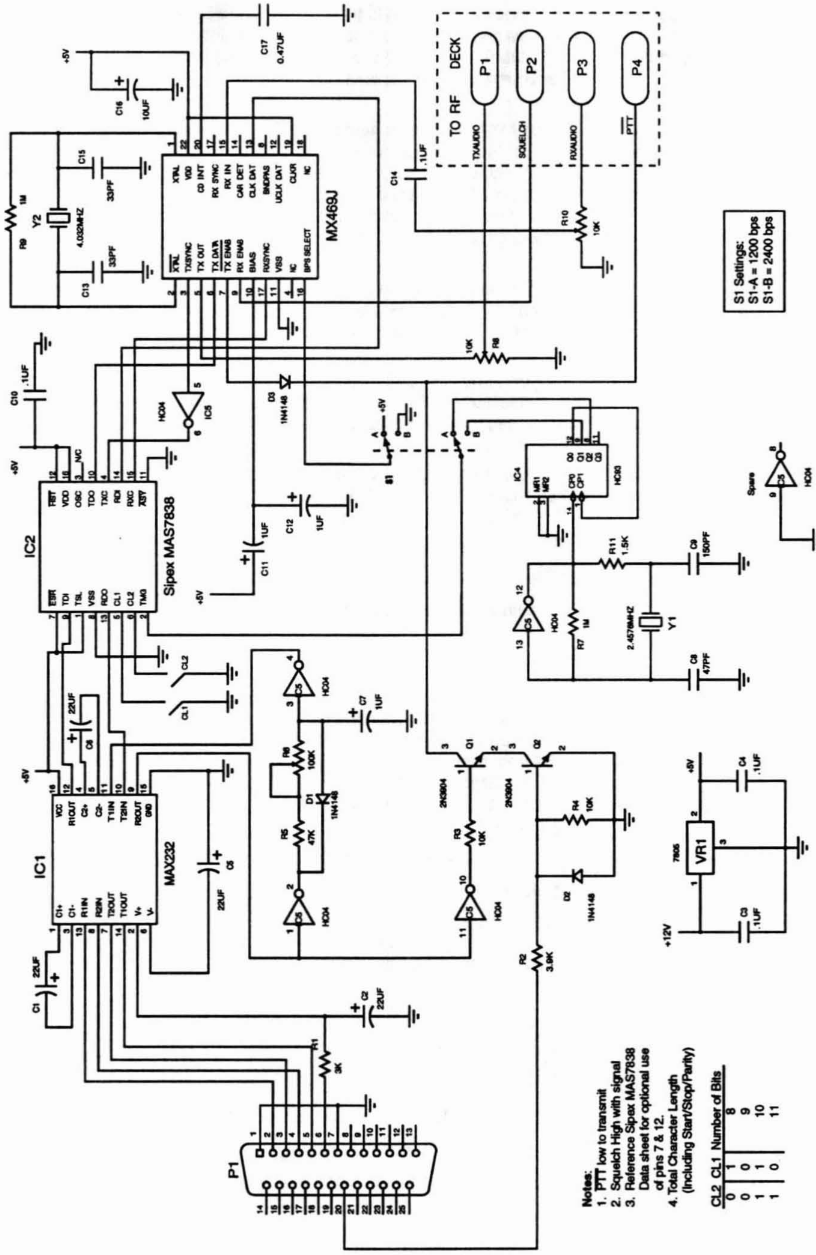
DTR = Data Terminal Ready
DSR = Data Set Ready
RTS = Request to Send
CTS = Clear to Send
TXD = Transmit Data
RXD = Receive Data
DCD = Data Carrier Detect

The Maxim MAX-232 converts the TTL/CMOS input/output levels to ±10V RS-232 input/output levels. On power-up, the data set ready (DSR) signal is set by the MAX-232's DC to DC converter. The incoming data terminal ready (DTR) signal enables the transmitter keying signal.

The request to send (RTS) and clear to send (CTS) signals are level shifted from the RS-232 interface to TTL/CMOS signal levels. When the modem receives an RTS, the RF transmitter and the MSK tone are keyed immediately and a 30 ms to 100 ms timer is started. At the completion of the timing, a CTS signal is generated for the data terminal to allow serial data flow.

The transmit data (TXD) signal is level shifted to the TTL/CMOS levels, and applied to the Sipex MAS7838 sync to async converter circuit. The random timed asynchronous input from the data terminal is synchronized with the transmit clock pulses of the MX469. If a timing error builds up due to the difference of the external asynchronous clock and the synchronous internal timing on the modem, the Sipex MAS7838 will skip a stop pulse to allow an adjustment to occur. The receiving end Sipex MAS7838 will generate a stop pulse and add it into the data flow so that no information is lost.

Using and MX469 MSK Sync. Modem with an Async. Data I/O


IC1
MAX232
IC2
Sipex MAS7838
MX469J
IC4
HC93
VR1
7805
P1
Y1
2.4576MHZ
Y2
4.032MHZ
Q1
Q2
2N3904
HC04
TO RF DECK
P1
P2
P3
P4
TXAUDIO
SQUELCH
RXAUDIO
PTT
S1
+5V
+12V
Spare
CL1
CL2

Notes:
1. PTT low to transmit
2. Squelch High with signal
3. Reference Sipex MAS7838 Data sheet for optional use of pins 7 & 12.
4. Total Character Length (Including Start/Stop/Parity)

CL2	CL1	Number of Bits
0	1	8
0	0	9
1	1	10
1	0	11

S1 Settings:
S1-A = 1200 bps
S1-B = 2400 bps

Figure 1: Schematic diagram of an MX469 in a typical application.

From the sync to async converter, synchronous information is then sent into the MX469, which converts the digital '1' into one cycle of 1200 Hz sinewave and a digital '0' into one and a half cycles of 1800 Hz sinewave for 1200bps and 1200 and 2400 Hz for 2400bps. This sinewave is then sent on the transmitter through a level adjustment. The signal is sufficiently band limited and level controlled to pass FCC type acceptance testing without any additional in-band filtering.

The incoming receiver signal is fed into the MX469 which is held in a power down mode until an RF carrier is detected by the receiver squelch circuitry. This minimizes power drain and also prohibits false information from being sent to the data terminal. If the receiver does not have a noise squelch signal, the chip's carrier detect must be used. It will detect within 12 ms the presence of the data modulation tone. This event is output on the carrier detect pin which should be used to disable the data output to minimize random data at the terminal. The use of the Schmidt trigger circuitry would minimize the 'clatter' at the beginning of the detection signal.

The tones are translated into logic levels and a digital phase lock loop is locked onto the incoming data steam within 16 bit reversals. The detected synchronous data and the recovered receive clock are sent into the Sipex MAS7838 for conversion back into asynchronous data. This information is then sent out to the data terminal through the Maxim MAX-232.

Operation in either a synchronous or asynchronous mode is achieved with a jumper. If additional RS-232 level shifting is needed for transmit and receive clocks and TX and RX enable, pins on the Sipex MAS7838 are brought low. Bringing these pins low bypasses the conversion process and allows synchronous data to pass directly through the device.

Proper clock frequency for the MX469 device is provided by a 4.032 MHz crystal. Clock frequency for the Sipex MAS7838 must be provided at 256 times the bit rate. This is accomplished by using a 2.4576 MHz crystal and dividing down by eight to 301.2 kHz (1200bps) or by four to 602.4 kHz (2400bps). Power is derived from a single 7805 voltage regulator. DC current measured on the first model is 12.75mA.

2. Software Considerations

As with many data systems, there are certain items that should be addressed within software for proper operation.

2.1 Bit sync pattern

The MX469 is a simple data pump that can be used with any protocol by adding the preamble to the start of the protocol. The ability of the MX469 to send and receive data, in a low signal to noise environment, lie in the ability of the receiving modem's phase lock loop to predictively determine the zero crossing of each successive data bit. A preamble must be sent prior to sending meaningful data (such as sync word or data) for the phase lock loop to acquire bit synchronization. A minimum of 16 successive alternating ones and zeros must be transmitted as a preamble to train the receiving MX469's phase lock loop.

This preamble pattern may be accomplished by appending two bytes of $55 or $AA onto the message. Make sure you take into account the stop, start, and parity bits to achieve a minimum of 16 one to zero transitions.

2.2 Stop, Start, and Length of Data

Once an RF signal ends, high level noise will be emitted from the receiver's discriminator. Even with data carrier detect or noise squelch circuits to gate the MX469's receiver off, there will be a period of noise (or false data out of the MX469) while muting circuits make a decision. This type of random data often creates problems down stream when applied to the logic controller or point of sale terminal. Having a message bracketed and only dealing with the information between start and stop characters is one method of prohibiting random data from entering the actual message. One should consider methods (or protocol) to distinguish start, stop, and length of data string to discern data burst from random noise.

2.3 Microprocessor Interface:

Although this application note depicts using the MX469 without the need of a microprocessor, interface to a microprocessor may also be considered by the circuit designer. Additional flexibility can be added so the microprocessor adds or strips off unnecessary RS-232 bits and adds the required preamble and bit timing to data sent to and from an asynchronous RS-232 port. The microprocessor interface is simple.

The MX469 internally generates a Tx and Rx SYNC clock for the microprocessor to use to synchronize each transmitted or received data bit. This allows the microprocessor to slave its timing to the zero crossings of the MSK modulation method used to conserve bandwidth. Each successive data bit sent from the microprocessor to the TX data input pin must be present and stable while the TX SYNC clock is transitioning from a low to a high. The next bit to be transmitted is sent, on the clock's falling edge. In a similar manner data is read from the Rx CLOCKED DATA output pin on the falling edge of the Rx SYNC clock output pin.

Data on the CLOCKED DATA output pin should be ignored while the Rx SYNC clock output pin is transitioning from a logic low to a logic high.

The Carrier Detect output can be used as an additional logic level to indicate an RF carrier is or is not present during data reception.

3. Operation with CTCSS or DCS Sub-Carriers

Because the MX469 modems contain a bandpass filter on the input, CTCSS/DCS sub-carriers are filtered out without extra circuitry.

It is important that no energy from the tone section appears within the transmitted data signal passband of 900 to 2100 Hz for 1200bps or 600 to 3000 Hz for 2400bps. It is equally important that the tone and data signals are not summed together and sent into the limiter section of the transmitter. The limiter represents a nonlinearity and would generate intermodulation products within the data bandpass which when received generate errors in the decoding of the data. Tone is normally summed into an FM transmitter after the limiting.

Radios designed only for data do not require a speech limiter, allowing tone and data to be summed directly.

4. RS-232 Handshake

The RS-232 handshake for asynchronous data requires the following signals:

Data Terminal Ready (DTR) is a signal from the terminal or computer that indicates to the modem that the unit is powered and active. An RF transmission should not be enabled if the Data Terminal is not active.

Data Set Ready (DSR) is a signal from the modem that indicates to the terminal that the unit is powered and active. Many terminals or computers will not allow data to flow without this condition being true.

Request to Send (RTS) emanates from the terminal or computer. The software or user has decided that transmission should begin and requests that the RF carrier be turned on.

Clear to Send (CTS) is a signal that originates from the modem. It is sent in response to a RTS, the request to send signal from the terminal or computer after certain criteria have been met. It is not sent until sufficient time has expired after the transmitter keyed to allow adequate settling time for both the RF transmitter and receiver. It would not be sent if there is an RF carrier on the channel indicating another user. Finally, it would not be sent if a high VSWR (Voltage Standing Wave Ratio) were detected on the transmitter when it was keyed. (Not all transmitters are provided with a VSWR detector.)

Transmit Data (TXD) and Receive Data (RXD) is the actual asynchronous data flow. Transmit data is data coming from the terminal and Receive data is data flowing into the terminal.

Data Carrier Detect (DCD) is often connected to DSR in a modem, if it is required to function as a Carrier Detect pin. However in this application DSR is permanently wired high.

MX·COM, INC. MiXed Signal ICs
APPLICATION NOTE
MPT1327 **Error Detection & Correction of MPT1327 Formatted Messages**

Error Detection & Correction of MPT1327 Formatted Messages using MX429A or MX809 devices

1.1 Background

MPT1327 messages are transmitted as 64-bit 'codewords', where each codeword contains 48 information bits followed by 16 check bits:

Bit No:	1 48	49 64
	information field	check bits

(Bit number 1 is transmitted first.)

These check bits allow the receive terminal to detect all odd numbers of errors, any 2 or 4 errors, and any error-burst up to length 16 in a codeword, and also to correct errors in the received codeword, although it should be noted that the higher the degree of error correction applied, the more likely is false decoding.

This document gives algorithms for:

Generation of the check bits of a transmitted codeword.
Received codeword error detection.
Limited error correction of a received codeword.

These algorithms may be used with any bit or byte oriented modem, such as the **MX429A** or MX809, although the **MX429A** and MX809 devices can perform check bit generation and error detection automatically and the **MX429A** also provides a 16-bit 'Syndrome' output which may be used to aid error correction.

1.2 Generation of Transmit Codeword Check Bits

1.2.1 Theory

The first 15 check bits are derived from a (63,48) cyclic code by using codeword bits 1 to 48 as the coefficients X62 to X15 (in that order) of a 63 bit polynomial, which is then divided modulo-2 by the generating polynomial;

X15 + X14 + X13 + X11 + X4 + X2 + X0 (11101000 00010101 binary)

On completion of the division, the 15 coefficients X14 to X0 of the remainder are used as the first 15 check bits (codeword bits 49 to 63), with the X0 coefficient (bit 63 of the complete codeword) inverted.

Finally, bit 64 of the codeword is added to provide an even parity check of the whole 64-bit codeword.

1.2.2 Example of Transmit Codeword Generation

Information field; 6 data bytes

89	AB	CD	EF	12	34	Hex
10001001	10101011	11001101	11101111	00010010	00110100	Binary

Polynomial division

x^{62}..x^{0}

```
10001001 10101011 11001101 11101111 00010010 00110100 00000000 0000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                     10010 10110010 001
                     11101 00000010 101
                      1111 10110000 1001
                      1110 10000001 0101
                         1 00110001 1100010
                         1 11010000 0010101
                           11100001 11101110
                           11101000 00010101
                               1001 11111011 0000
                               1110 10000001 0101
                                111 01111010 01010
                                111 01000000 10101
                                    111010 11111000 00
                                    111010 00000101 01
                                             11111101 0100000
```

Remainder with last bit inverted:

```
                                             11111101 0100001
```

Complete codeword, including parity bit:

```
Bit; 1                                                               64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
        89       AB       CD       EF       12       34       FD       42
```

1.2.3 'C' Language Algorithm

```
/*****************************************************************************/
/*   Function gen_ckbits() returns the first 15 check bits of a transmit     */
/*   codeword (codeword bits 49 to 63). Bit 15 of the returned value will    */
/*   be codeword bit 49, bit 1 of the returned value will be codeword bit    */
/*   63, and the lsb (bit 0) should be ignored.                              */
/*   The last bit (64) of the codeword must be derived separately, to        */
/*   give even parity of the whole 64-bit codeword.                          */

gen_ckbits()
  {
  int n,bit;
  unsigned int ckbits = 0;              /* Clear check bits          */
  for(n=1;n <= 48;n++)                  /* 48 information bits       */
    {                                   /*                           */
    bit = getbit_tx(n);                 /* Get each bit in turn      */
    if( 1 & (bit ^ (ckbits >> 15)))     /*    XOR tx bit with MSB    */
                                        /*    of checkbits and if    */
                                        /*    the result == 1        */
      ckbits ^= 0x6815;                 /*    then XOR checkbits     */
                                        /*    with 6815 Hex          */
    ckbits <<= 1;                       /* ... Shift check bit word  */
                                        /*      one bit left,        */
    }
  return(ckbits ^ 0x0002);              /* Return checkbits with     */
                                        /* codeword bit 63 inverted */
  }

/*   Function getbit_tx(n) should return bit 'n' (1 to 48) of the transmit*/
/*   codeword information field.                             */

getbit_tx(n)
  {
  return(/* 1 or 0 */);
  }
```

1.3 Receive Codeword Checking & Error Correction

1.3.1 Theory

The parity of the received 64-bit codeword is checked, then bit 63 of the codeword is inverted. The first 63 bits of the resulting codeword are then used as the coefficients X77 to X15 of a 77 bit polynomial, which is then divided modulo-2 by the 'generating polynomial'. If the remainder is zero, and the parity check is met, then no errors have been detected.

The 15-bit remainder of this division is used as the least significant 15 bits of the 16-bit 'Syndrome' word generated by the MX429 (and by the algorithm of section 3.4), while the msb of the Syndrome word is set to '1' if the parity of the received codeword is incorrect. The resulting Syndrome word value can give an indication of which bit(s) of the codeword have been received incorrectly; see section 3.4.

1.3.2 Example of Receive Codeword Checking: No Errors

Received codeword: 6 bytes:

```
          89        AB        CD        EF        12        34        FD        42
       10001001  10101011  11001101  11101111  00010010  00110100  11111101  01000010
Bit;   1...........................................................................64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

```
x77..............................................................................x0
10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
               1 00100101 0010111
               1 11010000 0010101
                 11110101 00000101
                 11101000 00010101
                    11101 00010000 000
                    11101 00000010 101
                            10010 10110010 001
                            11101 00000010 101
                             1111 10110000 1001
                             1110 10000001 0101
                                1 00110001 1100010
                                1 11010000 0010101
                                  11100001 11101110
                                  11101000 00010101
                                      1001 11111011 1111
                                      1110 10000001 0101
                                       111 01111010 10101
                                       111 01000000 10101
                                            111010 00000101 01
                                            111010 00000101 01

                                            000000 00000000 00000000 00000000 000000
Remainder = zero
MX429 'Syndrome' word:                      00000000 00000000
No errors detected
```

1.3.3 Example of Receive Codeword Checking: 2 Errors

Received codeword: 6 bytes: bits 9 & 10 in error

```
             89        6B        CD        EF        12        34        FD        42
          10001001  01101011  11001101  11101111  00010010  00110100  11111101  01000010
            errors;    xx
  Bit;    1                                                                           64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

```
x^77 ............................................................ ..............................x^0
10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 01111110 1
 1110100 00001010 1
   10101 01110100 010
   11101 00000010 101
    1000 01110110 1110
    1110 10000001 0101
     110 11110111 10111
     111 01000000 10101
       1 10110111 0001010
       1 11010000 0010101
          1100111 00111111 1
          1110100 00001010 1
            10011 00110101 011
            11101 00000010 101
             1110 00110111 1100
             1110 10000001 0101
                  10110110 10011111
                  11101000 00010101
                   1011110 10001010 0
                   1110100 00001010 1
                    101010 10000000 10
                    111010 00000101 01
                     10000 10000101 110
                     11101 00000010 101
                      1101 10000111 0111
                      1110 10000001 0101
                        11 00000110 001000
                        11 10100000 010101
                           10100110 01110110
                           11101000 00010101
                            1001110 01100011 0
                            1110100 00001010 1
                             111010 01101001 10
                             111010 00000101 01
                                    1101100 11110100 1
                                    1110100 00001010 1
                                       11000 11111110 011
                                       11101 00000010 101
                                        101 11111100 11011
                                        111 01000000 10101
                                          10 10111100 011101
                                          11 10100000 010101
                                           1 00011100 0010000
                                           1 11010000 0010101
                                            11001100 00001011
                                            11101000 00010101
                                              100100 00011110 01
                                              111010 00000101 01
                                               11110 00011011 000
                                               11101 00000010 101
                                                  11 00011001 101000
                                                  11 10100000 010101
                                                     10111001 11110100
```

MX·COM, INC. MiXed Signal ICs

APPLICATION NOTE

CMX602A **Using the CMX602A in place of the MX602**

Using the CMX602A in place of the MX602

Introduction

The CMX602A and the MX602 are pin compatible, use the same external components, draw the same current and the Zero Power and FSK Receive modes are unchanged. However, there are a few differences in operation that the user should be aware of.

1. In a British Telecom (BT) On-hook application, the controlling software should wait for the DET output to go high and then low again to indicate the presence of a Tone Alert signal.
2. For the Off-hook case, the $\overline{\text{IRQ}}$ output going low (when in Tone Alert Detect mode) indicates that a CAS has been detected. The local handset and keypad should then be muted as required by the Bellcore specification and the CMX602A switched to FSK Receive mode to be ready to receive the FSK data. Doing this will also clear the $\overline{\text{IRQ}}$ output.
3. If it is possible to mute the local speech from the microphone rapidly (within 0.5ms) without introducing noise (i.e. where the CIDCW equipment is built into the telephone set) then this should be done whenever the CMX602A is in Tone Alert Detect mode and the DET output is high. Doing this will markedly reduce the number of false responses generated by local (near end) speech. Note that the DET output is not used for any other purpose in an off-hook application when the CMX602A is set to Tone Alert Detect mode.

MX602 Algorithms with the CMX602A

The DET output high time for the CMX602A is 17ms less than the MX602, i.e. under average speech and CAS signal levels the DET output lengths from a MX602 are mostly in the range 35 to 50ms. For a CMX602A this reduces to 18 to 33ms. This may cause problems depending on the algorithm used.

The MX602 Data Sheet (Doc. # 20480136.004) describes two algorithms:

1. Algorithm (a) is for use when local speech muting can be effected without injecting noise, and says that the minimum DET high time should be 15ms. This algorithm will work with the CMX602A at the cost of a very slight loss in CAS detection performance.
2. Algorithm (b) is not recommended for use with the CMX602A.

For the optimum CMX602A algorithms, please refer to the latest CMX602A data sheet.

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APPLICATION NOTE

Recommendations for V.23 1200/75bps Full-Duplex Call Set-Up

Recommendations for V.23 1200/75bps Full-Duplex Call Set-Up

V.23 recommendations do not describe how a connection is established. The following information and figure describes how the connection should be established.

Note: One should not rely on other modems to follow this particular flow and the 1200/1200bps half-duplex connections are not covered by this application note.

1. The calling (originating) modem should connect to the line by operating the off-hook relay.
2. Having seized the line the dial tone should be detected. The dial tone will typically appear approximately 1/3 seconds after going off-hook. If the dial tone does not appear after 5 seconds return to the on-hook state. If dial tone monitoring is not to be performed (blind dialing) a pause of several seconds is necessary after line seizure and before dialing begins, typically 2 seconds.
3. Send DTMF digit sequence, tones should have ON and OFF periods of typically 100ms.

Reference Point A.

4. Calling modem remains silent after dialing until it receives a response from the answering modem. The first response may be the V.25 answering procedure, this should be ignored until the signal returns after 75ms ± 20ms energy drop, Reference Point B.
   Without V.25 answering procedure reference, point B will be the end of the 2 seconds answering modem's billing delay.
5. When binary '1's (high band marks) have been detected from the answering modem for 155ms ± 50ms the calling modem can be configured ready to receive data, Reference Point C.
   Start timers for 456ms ± 10ms and 765ms ± 10ms.
6. When the 456ms ± 10ms timer expires start transmitting binary '1's (low band marks) to the answering modem, Reference Point D.
7. When the 765ms ± 10ms timer expires the calling modem can change to data transmission mode and assert the CTS handshaking line. The binary '1's (low band marks) at the transmitter should now be replaced by data, Reference Point E.

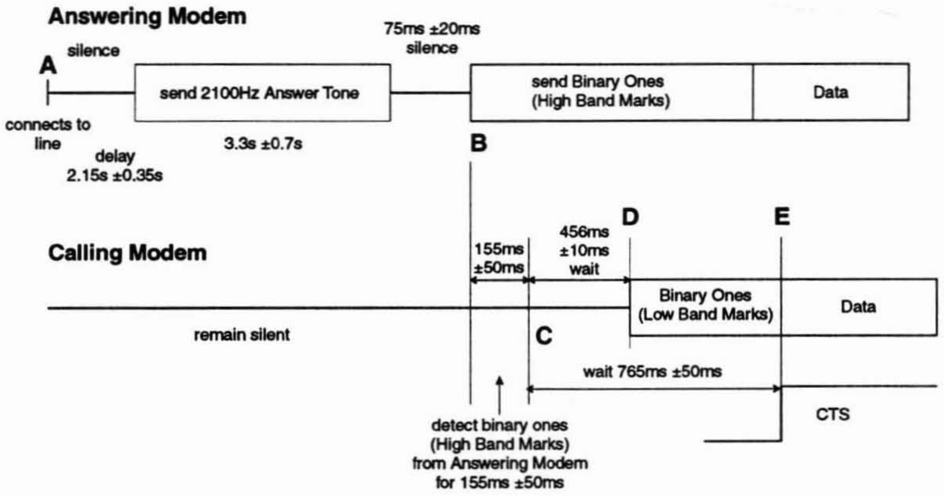

Answering Modem
silence
A
send 2100Hz Answer Tone
75ms ±20ms
silence
send Binary Ones
(High Band Marks)
Data
connects to
line
delay
2.15s ±0.35s
3.3s ±0.7s
B
Calling Modem
155ms
±50ms
456ms
±10ms
wait
D
E
Binary Ones
(Low Band Marks)
Data
remain silent
C
wait 765ms ±50ms
CTS
detect binary ones
(High Band Marks)
from Answering Modem
for 155ms ±50ms

Figure 1: Timing Diagram

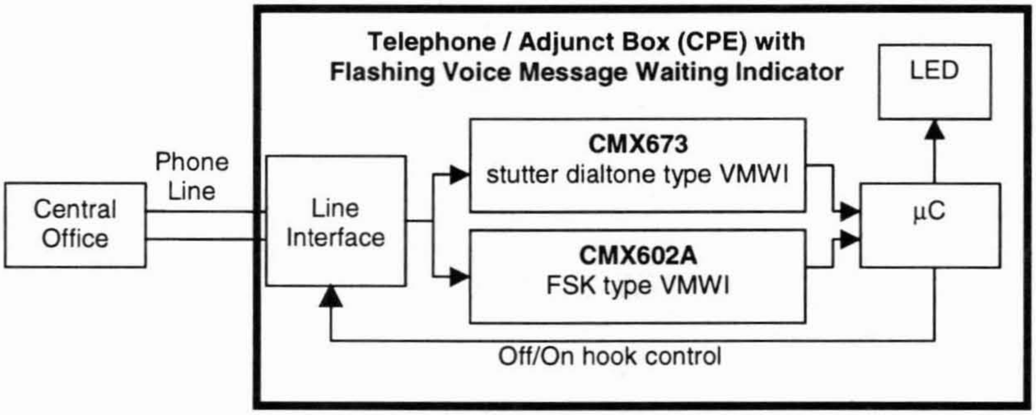
MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

CMX673 Suggested Applications

The CMX673 is a signal detector that operates on energy in the frequency band of about 300 to 650Hz. It's primary use is in the detection of status tones encountered in a telephone system. These tones include dial tone, circuits busy, ring tone, station busy, and others. Identification of specific status tones is derived by examining the specific on/off cadence of the CMX673's tone detector output. Featuring both high accuracy and rapid response time makes the CMX673 well suited for the rapid/short cadences used for services such as voice message waiting indication (VMWI).

This application note shows some typical applications (Figures 1, 2, 3, and 4), a simple scheme for connecting the CMX673 to a balanced telephone line (Figure 5), and some common call progress tone cadences and frequencies (Tables 1 and 2) and an illustrative cadence timing diagram (Figure 6).


Telephone / Adjunct Box (CPE) with
Flashing Voice Message Waiting Indicator
LED
CMX673
stutter dialtone type VMWI
CMX602A
FSK type VMWI
Phone Line
Central Office
Line Interface
µC
Off/On hook control

Using the output signals of the CMX673 and CMX602A, the µC identifies both the stutter dial tone and FSK types of voice message waiting indication signals that are popular in the U.S. The Central Office generates the stutter dial tone for a short period each time the CPE is taken off hook.

If voice messages are waiting, the µC flashes the LED to notify users without the user having to operate the phone or lift its handset.

Figure 1: Low Cost Dual Type U.S. Voice Message Waiting Indication

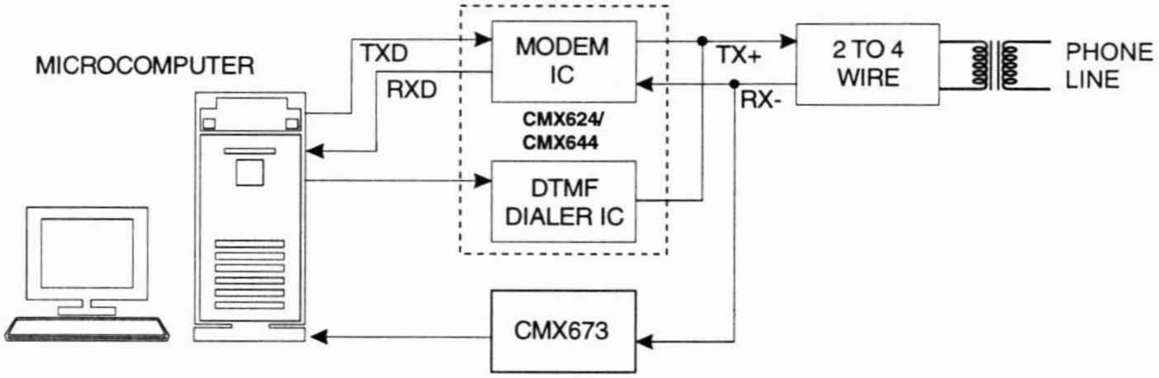

MICROCOMPUTER
TXD
RXD
MODEM IC
CMX624/
CMX644
DTMF DIALER IC
CMX673
TX+
RX-
2 TO 4 WIRE
PHONE LINE

Figure 2: Detecting Dial Tone and Secondary Dial Tones in an Automatic Dialing Data Modem

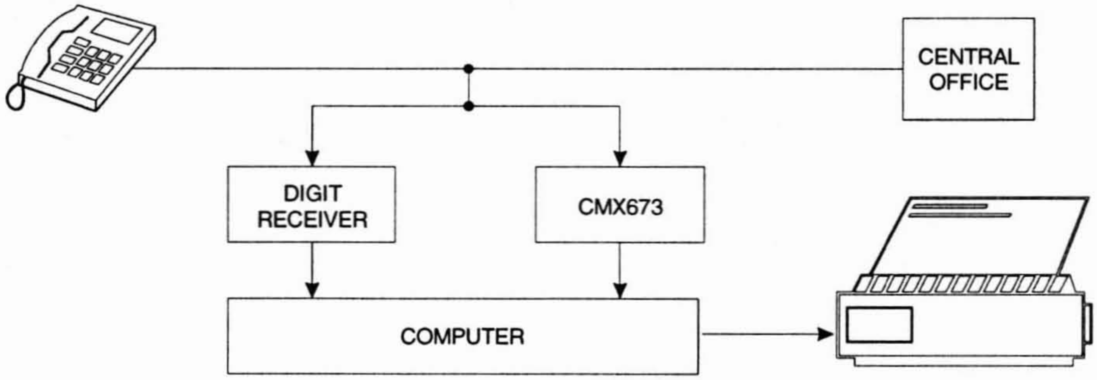

CENTRAL OFFICE
DIGIT RECEIVER
CMX673
COMPUTER

Figure 3: Call Detail and Completion Monitor in a Billing System

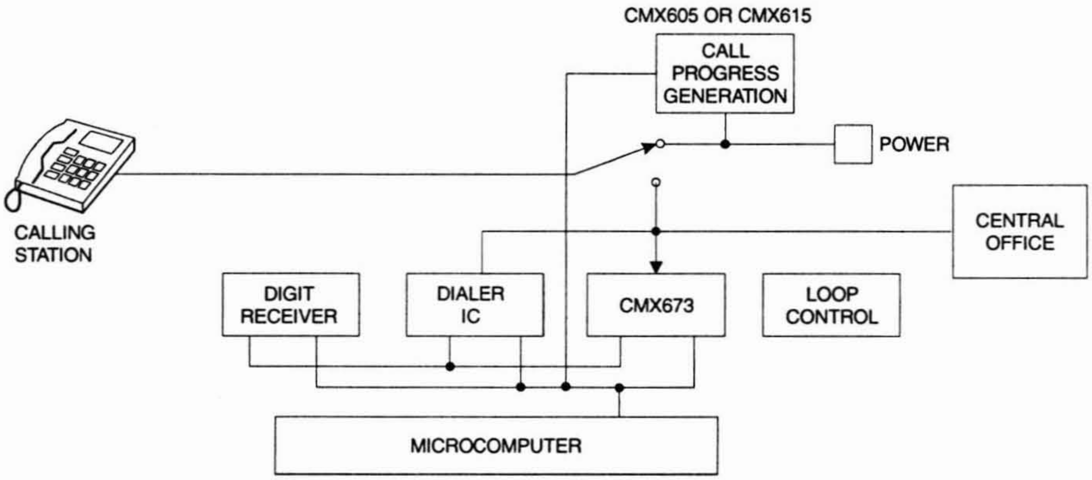

CMX605 OR CMX615
CALL PROGRESS GENERATION
POWER
CALLING STATION
CENTRAL OFFICE
DIGIT RECEIVER
DIALER IC
CMX673
LOOP CONTROL
MICROCOMPUTER

Figure 4: Call Routing in a Speed Dialing System

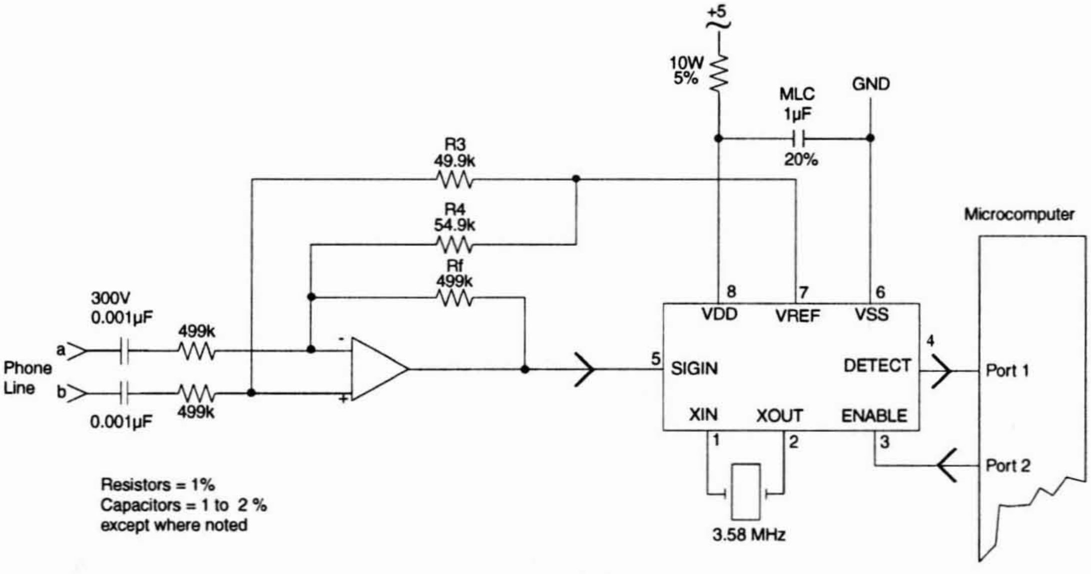
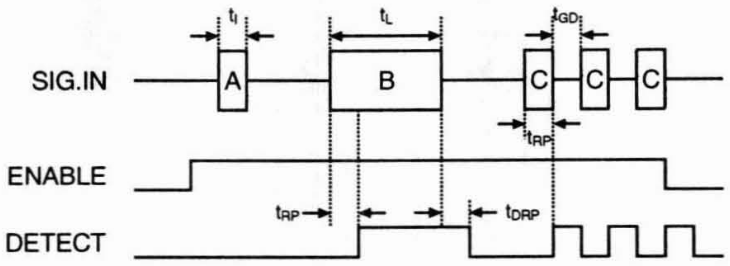

+5
10W
5%
MLC
1µF
20%
GND
R3
49.9k
R4
54.9k
Rf
499k
300V
0.001µF
499k
a
b
Phone Line
0.001µF
499k
-
+
8
VDD
7
VREF
6
VSS
5
SIGIN
DETECT
4
XIN
1
XOUT
2
ENABLE
3
3.58 MHz
Microcomputer
Port 1
Port 2
Resistors = 1%
Capacitors = 1 to 2 %
except where noted

Figure 5: Monitoring Signals from a Balanced Phone Line



KEY

A = Signal within call progress detection range, but not of sufficient duration to be detected

B = Continuous call progress tone. i.e. Dial Tone

C = 3 bursts of 0.1seconds followed by a continuous tone (not shown) in the call progress band. i.e. Recall Dial 1

t_I = Burst length ignored

t_L = Burst length detected

t_{GD} = Call progress tone gap length detected

t_{RP} = Call progress response time

t_{DRP} = Call progress tone de-response time

Figure 6: An Example of Tone Detection (via Tone Cadence) using the CMX673

The minimum level required by the CMX673 is -38dBm. In general, to optimize transient response and to limit spurious DETECTs, it is best to use the least sensitive configuration possible. The gain of the buffer stage shown in Figure 4 is equal to the ratio of Rf to Rin and may be varied to obtain the sensitivity required for a given application. Balanced network input impedance provides rejection of common mode signals. If component values are changed to obtain different gain, then the parallel combination of Rf and R4 must be kept equal to R3 to maintain proper balance. Closely matching 1% resistor and capacitor values should also be used.

STUTTER DIAL TONE	
Cadence	10 bursts (each 0.1 sec on / 0.1 sec off) then steady on.
Frequencies	350 + 440 Hz
DIAL TONE	
Cadence	On, Steady
Frequencies	400, 425, 350 + 440, 600 x 120, 33 Hz
AUDIBLE RING	
Cadence	2 sec. on, 4 sec. Off or 1/3 sec. on, 1/3 sec. off, 1/3 sec. on, 2 sec off …
Frequencies	400, 425, 440 + 480, 420 x 40, 450 ,400 x 25 Hz
LINE BUSY	
Cadence	0.5 sec. On, 0.5 sec. Off, …,
Frequencies	400, 425, 480 + 620, 600 x 120, 450 Hz
RECORDER (Busy Circuits)	
Cadence	0.25 sec. On, 0.25 sec. Off, or 0.5 sec. On, 1 sec off, …
Frequencies	400, 425, 480 + 620, 600 x 120, 450 Hz

Table 1: Some Common Call Progress Tone Cadences and Frequencies

TONES	330	440	480	620	Power per frequency at exchange[b] where tone is applied[c]	Cadence
Dial Tone	X	X			-13dBmO	Continuous Tone
Dial tone – Modern PABX only	X	X			-16dBmO	Continuous Tone
Recall Dial Tone	X	X			-13dBmO	3 burst of 0.1 seconds followed by a continuous tone [e]
Recall Dial Tone – Modern PABX only [g]	X	X			-16dBmO	3 burst of 0.1 seconds followed by a continuous tone [e]
Busy Tone			X	X	-24dBmO	Burst 0.5 seconds / silence 0.5 seconds
Busy Tone – Modern PABX only			X	X	-21dBmO	Burst 0.5 seconds / silence 0.5 seconds
Reorder Tone			X	X	-24dBmO	Burst 0.25 seconds / silence 0.25 seconds
Reorder Tone – Modern PABX only			X	X	-21dBmO	Burst 0.25 seconds / silence 0.25 seconds
Audible Ringing Tone		X	X		-19dBmO	Burst 2 seconds / silence 4 seconds
Audible Ringing Tone – Modern PABX only		X	X		-16dBmO	Burst 1 seconds / silence 3 seconds
Call Waiting Tone		X			-13dBmO	Burst of 0.3 seconds every 10 seconds
Call Waiting Tone – Modern PABX only [g]		X			-16dBmO	Station Call Waiting : Burst of 0.3 seconds
					-16dBmO	Outside Call Waiting: 2 bursts of 0.1 seconds [e]
					-16dBmO	Urgent Call Waiting: 3 bursts of 0.1 seconds [e]
Busy Verification		X			-13dBmO	A 2.0 second burst followed by 0.5 second bursts every 10 seconds
Busy Verification – Modern PABX only [g]		X			-14dBmO	Bursts of 1.5 to 2.0 seconds followed by… [f]
Executive Override – Modern PABX only [g]		X			-14dBmO	Burst of 3.0 seconds
Confirmation Tone	X	X			-13dBmO	Burst of 0.1 seconds / silence 0.1 second / burst 0.3 seconds
Confirmation Tone – Modern PABX only [g]	X	X			-16dBmO	3 bursts 0.1 seconds [e]

(a) Frequency Limits are ±0.5% of the nominal frequency.
(b) PABX tone levels are measured at the PABX interfaces (typically at customer premises). Power levels are 2dB lower for private line interfaces.
(c) Power level tone tolerances are +1.5dB
(d) Tolerance level for PABX dial tone is +0.75dB.
(e) Bursts are separated by 0.1 seconds
(f) Burst of 1.5 to 2.0 seconds before attendant intervenes, followed by repeated bursts of 0.5 to 0.8 seconds, 8 to 20 seconds apart
(g) Tones applied at PABX station or private line interfaces and not at the exchange interfaces.

Table 2: Call Progress Tone Cadence and Frequencies - Taken from the CCITT Blue Book (Fascicle ii.2 - Suppl. No. 3)

MX•COM, INC. MiXed Signal ICs

APPLICATION

SPM 12kHz and 16kHz Blocking Filters

This application note presents SPM (Subscriber Pulse Metering or Tax Metering) detection and methods to attenuate SPM burst signals. Common hybrids or SLICs (subscriber line interface circuit) input circuits have limited dynamic range and are adversely affected by large amplitude SPM signal bursts. The SPM pulses drive analog signals into the VDD or supply rails resulting in distortion of analog voice signals.

The following design example demonstrates SPM signal detection prior to attention by a blocking filter. The output of the blocking filter is then presented to common interface circuits. This approach provides reliable SPM detection without compromising the limited dynamic range of the hybrid; SLIC or hand set circuit.

Inductive components shown in the schematics are from Midcom; a supplier of wire wound products for the telecommunications industry.

1. Single Subscriber SPM Circuit

The following example uses MX-COM's CMX631A SPM detector IC and Midcom SPM blocking filters.

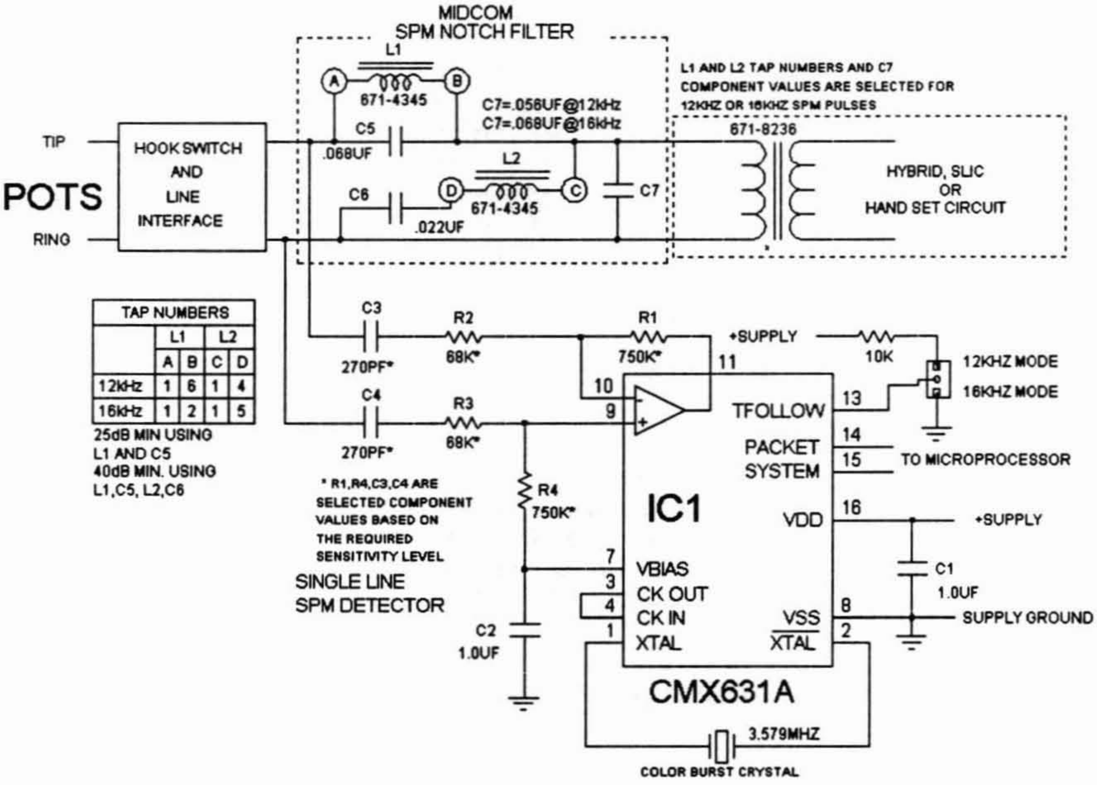

MIDCOM
SPM NOTCH FILTER
L1
A
B
671-4345
C5
.068UF
C7=.056UF@12kHz
C7=.068UF@16kHz
L2
C6
D
C
671-4345
.022UF
C7
L1 AND L2 TAP NUMBERS AND C7
COMPONENT VALUES ARE SELECTED FOR
12KHZ OR 16KHZ SPM PULSES
671-8236
HYBRID, SLIC
OR
HAND SET CIRCUIT
TIP
POTS
RING
HOOK SWITCH
AND
LINE
INTERFACE
TAP NUMBERS
L1
L2
A B C D
12kHz 1 6 1 4
16kHz 1 2 1 5
25dB MIN USING
L1 AND C5
40dB MIN. USING
L1,C5, L2,C6
C3
270PF*
R2
68K*
R1
750K*
C4
270PF*
R3
68K*
+SUPPLY
10K
12KHZ MODE
16KHZ MODE
11
10
9
13
TFOLLOW
14
PACKET
SYSTEM
15
TO MICROPROCESSOR
* R1,R4,C3,C4 ARE
SELECTED COMPONENT
VALUES BASED ON
THE REQUIRED
SENSITIVITY LEVEL
R4
750K*
IC1
16
VDD
+SUPPLY
SINGLE LINE
SPM DETECTOR
7
VBIAS
3
CK OUT
4
CK IN
1
XTAL
C1
1.0UF
8
VSS
SUPPLY GROUND
2
XTAL
C2
1.0UF
CMX631A
3.579MHZ
COLOR BURST CRYSTAL

Figure 1: SPM Single Line Circuit

APPLICATION

Subscriber Pulse Metering (SPM) 12kHz and 16kHz Blocking Filters

Figure 1: SPM Single Line Circuit shows an SPM notch filter and a CMX631A SPM detector. The SPM detector is connected prior to the notch filter to detect SPM pulses. L2 and C6 are optional to provide additional attenuation of SPM pulses up to 40dB. If only L1 and C5 are used approximately 25 dB of attenuation can be achieved. The 671-4345 inductors L1 and L2 have four taps to select different inductance values. Table 1 : Circuit values, indicate which tap numbers to use for 12kHz and 16kHz filters. Refer to the CMX631A data sheet for selecting the correct component values for C3, C4, R2, R3, R1, and R4.

SPM Blocking/Attenuation Filter Selection						
	L1 A#	L1 B#	L2 C#	L2 D#	C7	C8*
12KHZ	1	6	1	4	56nf	unused
16KHZ	1	2	1	5	68nf	22nf

*Note: C8 is across the hybrid side of the iso-xfmr and is not shown

Table 1 : Circuit values

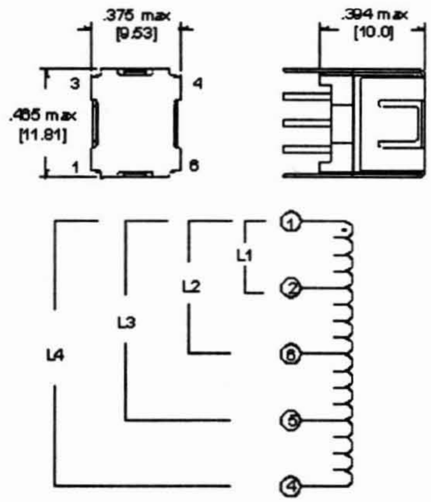


Figure 2: Inductor Schematic/Mechanical

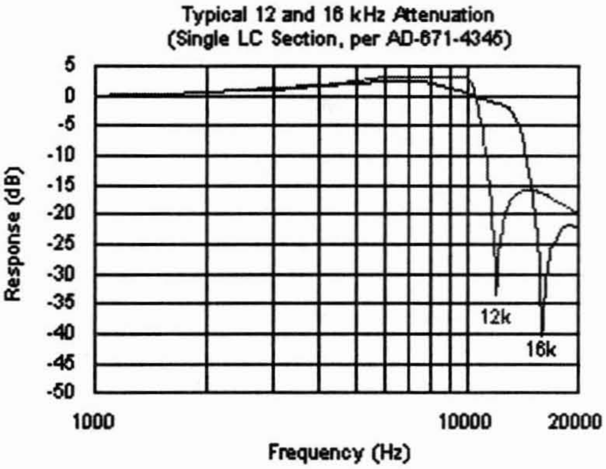


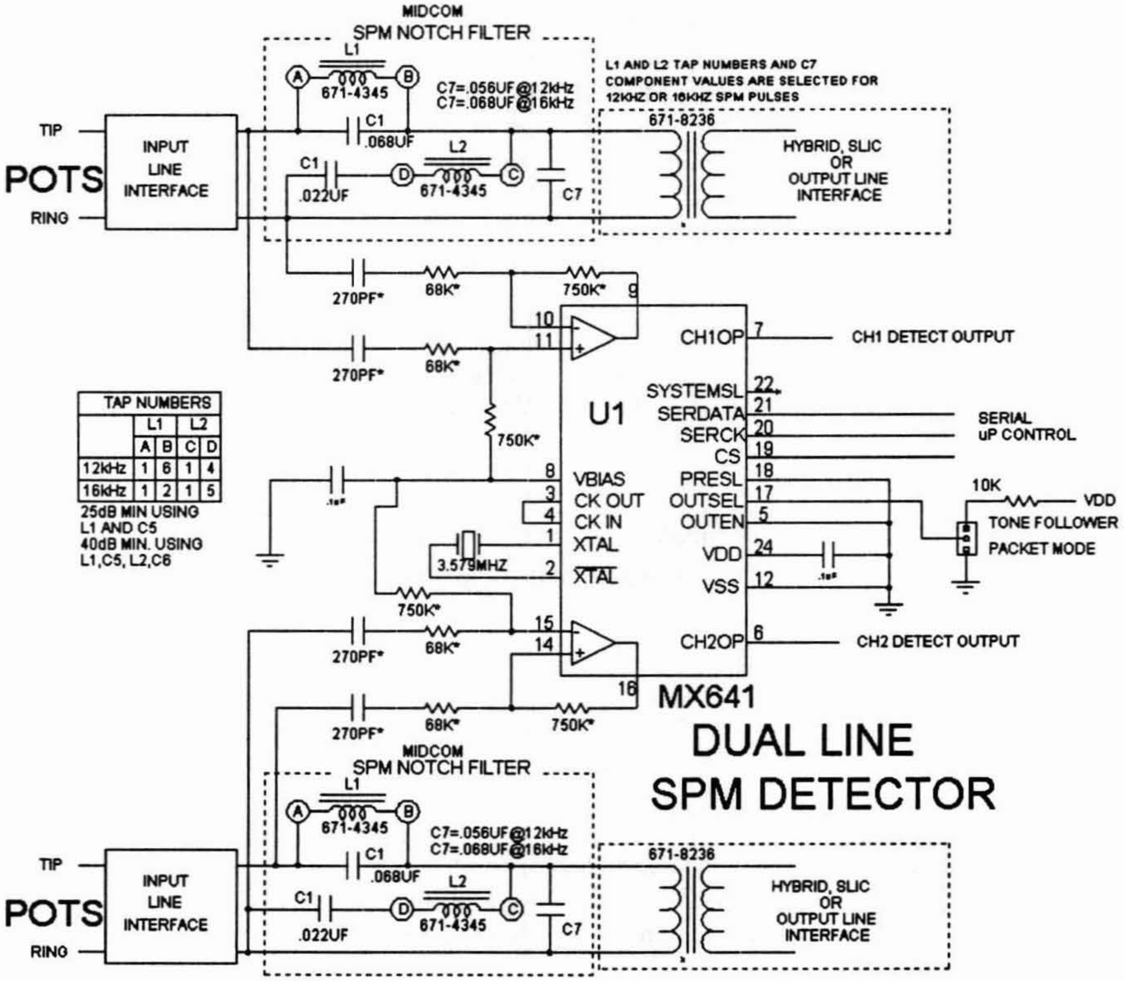
Figure 3: Attenuation

The SPM tone frequency and level are defined by a country's specification. The circuit values and jumper positions are shown for both 12KHz and 16Khz tones. The Line Interface block is designed to meet type acceptance requirement for the countries the equipment will be used in. Reference designs for the Line Interface block is beyond the scope of this application note. Many references can be found on the Internet or in technical publications.

The output of the SPM blocking filter can be connected to a Hybrid; SLIC or hand set circuit. An isolation transformer is shown for reference only and may or may not be required for all applications.

2. Multi Line SPM detection

The circuit shown below is a two-line SPM design for a multi-line card. Figure 4, uses MX-COM's MX641 SPM detector and Midcom inductors for SPM filtering. Circuit connections after the SPM filter are design dependent. The designer must take into account all circuit parameters to insure the design meets regulatory requirements and the needs of the customer.


MIDCOM
SPM NOTCH FILTER
L1
A
B
671-4345
C7=.056UF@12kHz
C7=.068UF@16kHz
L1 AND L2 TAP NUMBERS AND C7 COMPONENT VALUES ARE SELECTED FOR 12KHZ OR 16KHZ SPM PULSES
671-8236
TIP
POTS
RING
INPUT LINE INTERFACE
C1
.068UF
L2
C1
.022UF
D
C
671-4345
C7
HYBRID, SLIC OR OUTPUT LINE INTERFACE
270PF*
68K*
750K*
9
10
11
CH1OP
7
CH1 DETECT OUTPUT
270PF*
68K*
SYSTEMSL
22
SERDATA
21
SERCK
20
CS
19
U1
750K*
SERIAL uP CONTROL
8
VBIAS
PRESL
18
3
CK OUT
OUTSEL
17
10K
VDD
4
CK IN
OUTEN
5
TONE FOLLOWER
PACKET MODE
1
XTAL
VDD
24
3.579MHZ
2
XTAL
VSS
12
.1uF
750K*
15
14
CH2OP
6
CH2 DETECT OUTPUT
270PF*
68K*
16
MX641
270PF*
68K*
750K*
DUAL LINE SPM DETECTOR
MIDCOM
SPM NOTCH FILTER
L1
A
B
671-4345
C7=.056UF@12kHz
C7=.068UF@16kHz
C1
.068UF
671-8236
TIP
POTS
RING
INPUT LINE INTERFACE
C1
.022UF
L2
D
C
671-4345
C7
HYBRID, SLIC OR OUTPUT LINE INTERFACE
25dB MIN USING
L1 AND C5
40dB MIN. USING
L1,C5, L2,C6

TAP NUMBERS	L1		L2	
	A	B	C	D
12kHz	1	6	1	4
16kHz	1	2	1	5

Figure 4 Two-Line SPM Circuit

MX-COM Inc. offers the follow SPM products:

MX623	Line Powered SPM Detector
CMX631A	Low Voltage SPM Detector
MX641	Dual Subscriber SPM Detector
MX651	Single SPM Detector with Anti-Fraud

For additional information please contact MX-COM, Inc. or you may contact Midcom at:

Midcom
121 Airport Drive
P.O. Box 1330
Watertown, SD 57201-6330
USA Sales: sales@midcom-inc.com

Telephone: +1.605.886.4385
Toll Free: 1-800-643-2661(US and Canada)
Fax: +1.605.886.4486The
http://www.midcom-inc.com
Suppliers: matrls@midcom-inc.com

3. Additional Information:

Designing a type accepted POTS (Plain Old Telephone System) interface is beyond the scope of this application note. Many customers seek a low cost solution to meet type acceptance. The circuit design can be simple or quite complex. The design often needs to be versatile so as to meet several countries' standards while also being price competitive. There are many design approaches with each having performance trade off.

3.1 Regulatory Issues:

The document ETS 300 001 contains information regarding SPM may be obtained from:

ETSI (European Telecommunications Standards Institute)

06921 Sophia Antipolis Cedex

France

Phone: 33 92 94 42 00
Fax: 33 93 65 47 16

Other international standards, such as ITU, may also be helpful.

3.2 Telephony Circuit Design:

The Internet offers many great places to find application notes on telephone connected circuit design.

Midcom has a web page that includes some application notes. If you have some favorite web sites or reference books we would appreciate hearing from you. Please forward information to <mxsales@mxcom.com>

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX633/643 Noise Immunity Circuit for the MX633/643 Call Progress Detectors

1. Introduction

The telephone's central office sends call progress signals during the origination of a telephone call. Successful completion of each step of the connection process changes the call process signal. Call Progress Detectors, in computerized telephony equipment, provide quick progress detection for call automation applications.

2. Overview

The MX633 and MX643 are low power, low cost, call progress solutions. Both devices detect Dial Tone, Ring and Busy. The MX643 also detects international Special Information Tones (SIT). Both devices are capable of detecting tones levels down to -40dBm. Some applications are sensitive to noise. This application note provides an evaluation circuit for bread boarding purposes and discusses an approach for limiting the call progress detector's sensitivity to noise in poor signal to noise situations. Refer to the MX633 and MX643 data sheets for full details for device operation.

3. Noise Rejection Circuit

The schematic in Figure 2 page 3, depicts the MX643DW used in conjunction with a LM311 comparator. (The same circuit applies to MX633 use as well.) The comparator circuit (with hysteresis) provides audio signal conditioning for the call progress detector. Noise signals below a set threshold voltage are rejected. The comparator circuit is designed for single supply, +5.0VDC operation.

3.1 Circuit Description

Resistors R16, R3 and C5 form a 2.5 VDC reference bias applied to both inputs of the comparator through 100K Ω resistors, R2 and R4. Resistor R5 provides hysteresis (positive feedback) adjusting the threshold level above or below the 2.5V reference. When R5's value is 10 MΩ the signal level's threshold is approximately 18mVrms. Signals below 18mVrms do not trigger an output from the comparator. A power level of 0dBm represents 775 mVrms across 600 Ωs. Signal amplitudes below -32.7dBm (18mVrms referenced to 0dBm equal to 775mrms) are not presented to the input of the call progress detector.

The noise rejection circuit depicted in Figure 2 page 3, may require some adjustment depending on the application. Component tolerances of 5% for resistors and 10% for capacitors are used but should be set to reflect the requirements of the application.

3.2 Noise Rejection Threshold Adjustment

R5's value can vary to match noise rejection threshold requirements. Changing R5 from 10 MΩs to 20 MΩs results in a 9mVrms threshold. Changing R5 from 10 MΩs to 1 MΩs results in a 170mVrms threshold.

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4. Circuit Layout Hints

4.1 LM311

The comparator circuit is sensitive to noise therefore the printed-circuit layout should be engineered with care to avoid sources of noise.

- Keep leads and traces short.
- Use a ground foil around the LM311 between inputs and outputs.
- Guard against capacitive coupling from high-level signals to the input pins.
- Route the LM311's output signal away from its input pins and pins 5 and 6.
- Place a bypass capacitor as close as practical across the power and ground pins.
- The device providing audio to the LM311 should have a low source impedance (1KΩ or less).

4.2 MX633 / MX643

The Call Progress Detector circuit is sensitive to noise therefore the printed-circuit layout should be engineered with care to avoid sources of noise.

- Keep leads and traces short.
- Use a ground foil around the MX633/643 between inputs and outputs.
- Guard against capacitive coupling from high-level signals to the input pins.
- Place a bypass capacitor as close as practical across the power and ground pins.
- If the supply source also powers digital logic additional filtering on the supply trace going to the MX633/643 should be considered.
- The device providing audio to the MX633/643 should have a low source impedance 10KΩ or less).
- Avoid stray capacitive coupling to crystal pins.

4.3 Audio Filtering

It is a good design practice to add an anti-aliasing filter prior to the LM311's input. The call progress detectors sample input signals at a 9.3 Khz rate. Care should be taken to avoid high frequency signals above 8.4khz as they will alias in the call detector's decoder. An anti-aliasing filter set at 5Khz is recommended in noisy environments where stray coupling of digital noise into the audio path is likely. Refer to Figure 1: Anti-aliasing Filter. If the input audio signal is buffered by an opamp in a previous stage, designers task of adding an anti-aliasing filter is simplified. Adding a capacitor across the opamp's feed back resistor, will form the desired anti-aliasing low pass filter. C2s value is calculated using the following.

$$f_{o\ @\text{-}3dB} = \frac{1}{(2\pi C_2R_2)} \qquad C2 = \frac{1}{(2\pi\ 5KHz\ 100K\Omega)}$$

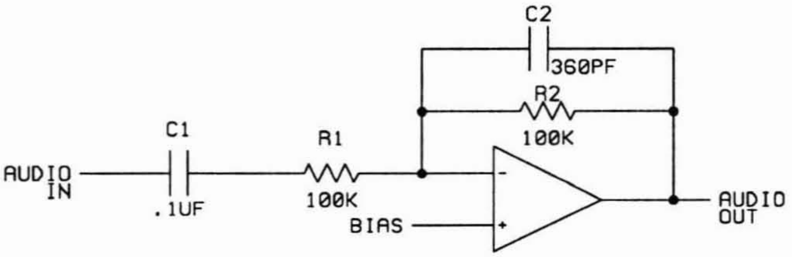


Figure 1: Anti-aliasing Filter

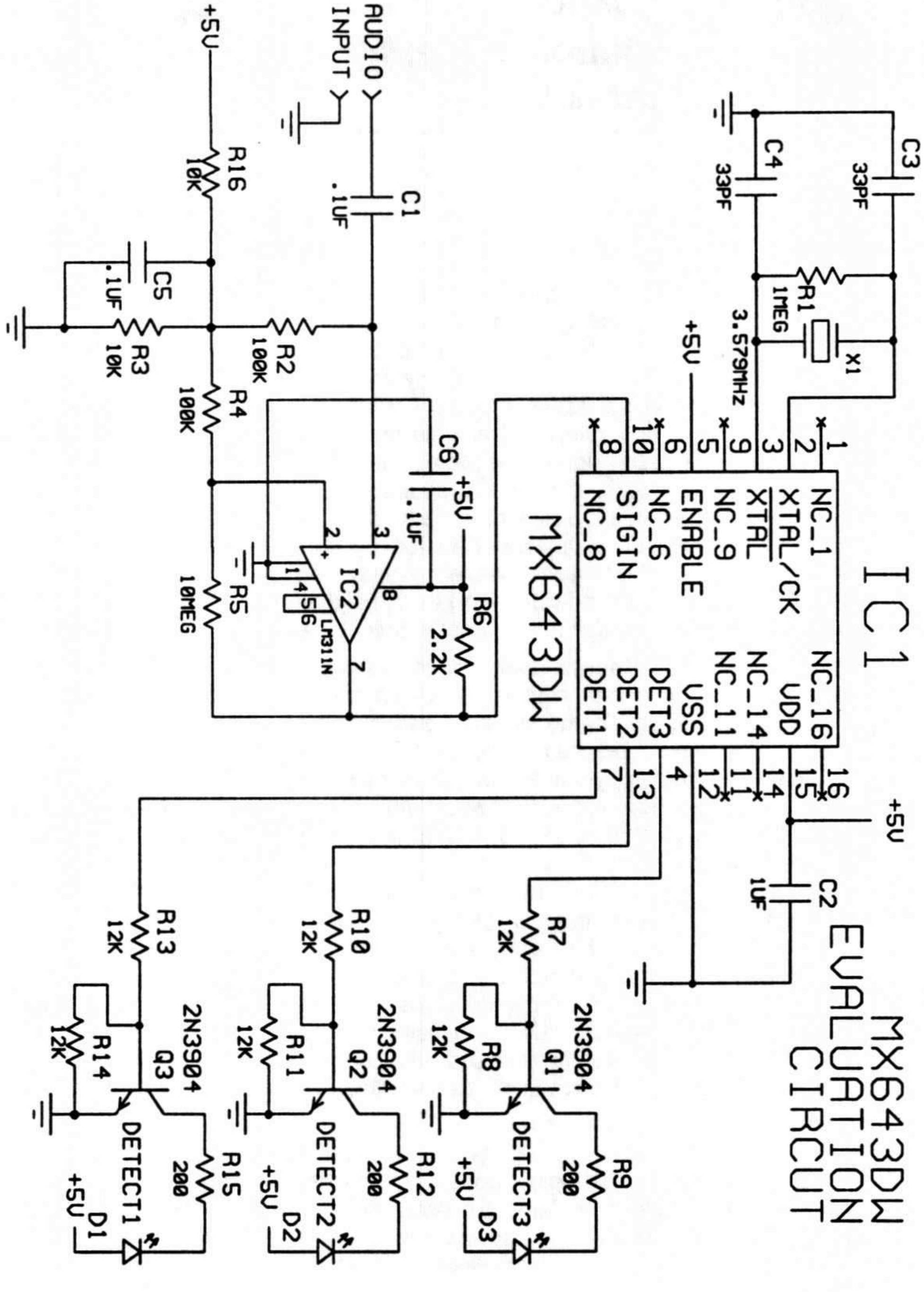

MX643DW
EVALUATION
CIRCUIT
IC1
MX643DW
NC_1
XTAL/CK
XTAL
NC_9
ENABLE
NC_6
SIGIN
NC_8
NC_16
VDD
NC_14
NC_11
VSS
DET3
DET2
DET1
C3
33PF
C4
33PF
R1
1MEG
X1
3.579MHz
+5V
AUDIO
INPUT
C1
.1UF
R16
10K
C5
.1UF
R2
100K
R3
10K
R4
100K
R5
10MEG
C6
.1UF
IC2
LM311N
R6
2.2K
C2
1UF
R7
12K
R8
12K
Q1
2N3904
R9
200
D3
DETECT3
R10
12K
R11
12K
Q2
2N3904
R12
200
D2
DETECT2
R13
12K
R14
12K
Q3
2N3904
R15
200
D1
DETECT1

Figure 2: MX633DW Noise rejection circuit

MX•COM, INC. MiXed Signal ICs

APPLICATION

Continuously Variable Slope Delta Modulation: A Tutorial

1. Introduction

Virtually all means of wireless and wireline speech communication are, or are becoming, digital. Digital coding of speech for transmission or storage clearly has advantages over traditional analog methods. In digital data communication or storage systems, information is transmitted or recorded as a series of binary digits—the receiver or player must only distinguish between a one or zero to exactly recover the original information. In digital voice systems the information is the human voice. Digital speech coding algorithms are judged by their ability to quantize (digitize) speech accurately for transmission and then perform the reverse at the decoder. In other words, the original analog speech signal must be accurately recovered at the receiver. Sounds simple, however, without compression quantized speech can require significantly more bandwidth than analog speech. For wireline or wireless telecom applications, the speech extends from 300 Hz to 3300 Hz. If an analog signal in this band is quantized using a linear Analog to Digital Converter (ADC) sampling just above the Nyquist rate, say 8 KHz, with 256 quantization levels (8 bits) the resulting data rate is 64 Kbits per second. Without exotic modulation/coding, the bandwidth (BW) for the digitally encoded signal is nearly twenty times the original analog signal. Such BW consumption is not practical, particularly for wireless applications.

Engineers working in the field of Speech Coding have been actively searching for methods to reduce the bandwidth consumed by quantized speech signals. Early algorithms attempted to take advantage of the human ear's adaptive dynamic range. The human ear has a built in ability to become more or less sensitive to audible signals—the ear can hear sound pressure levels (SPL) as low as 0 dB SPL (threshold of human hearing) to 120 dB SPL (on set of pain) yet at any one time the dynamic range of human hearing is generally considered to be about 40 dB. In other words, we have a difficult time hearing someone whispering at a rock concert. Some speech coding algorithms exploit this phenomena by using a greater number of progressively smaller quantization levels for low amplitude signals and fewer, more coarse quantization levels for large amplitude signals. This is known as non-uniform quantization. Non-uniform quantization is used in the Public Switched Telephone Network (PSTN) where it is called μ-law Pulse Code Modulation (PCM). A slightly more complex approach takes advantage of strong correlation between adjacent speech samples, quantizing the amplitude *difference* (delta) between two samples as opposed to the entire sample amplitude. This *difference* signal requires fewer quantization levels for the same signal quality and consequently, reduces the required bandwidth. Algorithms employing this technique are classified under the broad category of differential quantization or differential PCM (DPCM). Further bandwidth conservation is possible through more complex algorithms. For example, combining adaptive quantization with DPCM results in the commonly used coding algorithm, adaptive DPCM (ADPCM).

Delta modulation (DM) and Continuously Variable Slope Delta modulation (CVSD) are differential waveform quantization techniques. Both employ two level quantizers (one bit). CVSD is basically DM with an adaptive quantizer. Applying adaptive techniques to a DM quantizer allows for continuous step size adjustment. By adjusting the quantization step size, the coder is abled to represent low amplitude signals with greater accuracy (where it is needed) without sacraficing performance on large amplitude signals.

CVSD is used in tactical communications where "communication quality[1]" is required yet the option for security must be available. MIL-STD-188-113 (16 Kb/s and 32 Kb/s), and Federal Standard 1023 (12 Kb/s CVSD) are examples of a tactical communication systems using CVSD. With the tremendous worldwide growth in wireless technology, secure communication is becoming important to everyone. In addition to point-to-point communication, CVSD is commonly used in digital voice recording/messaging and audio delay lines.

This paper attempts to describe CVSD quantization, focusing on its application to coding of speech. Before discussing the details of CVSD, the basics of uniform and non-uniform quantization (non-adaptive) will be reviewed. Next, the subject of differential quantization will be explained, showing that DM and CVSD are equivalent to one bit DPCM and ADPCM, respectively. Finally, some application suggestions for MX•COM CVSD codecs will be presented.

---

[1] ***Communication quality*** is a qualitative expression widely considered synonymous with "acceptable speech communication." It is not intended to imply "high-fidelity," only that intelligible conversation can take place.

2. Waveform Quantization [1, 3, 5, 9]

Waveform quantization is a process of assigning discrete levels to a sampled analog signal. In the context of this paper the signal of interest is speech, although the concepts are applicable to signals in different frequency bands. The term "quantization" implies a relationship between the amplitude of a discrete sample and its numeric value. This relationship may be linear, non-linear, or differential.

2.1 Sampling [5, 9]

Before a signal can be quantized it must first be sampled. Sampling is the act of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is called the sampling frequency. As the sampling rate increases, the sampled signal begins to approximate the original continuous signal. As the sampling frequency decreases, samples move further apart in time, eventually the original signal cannot be reconstructed from the sampled version. The limit on how far apart these samples can be, without losing information, is the basis for Shannon's sampling theorem.

Shannon's sampling theorem [5] was originally stated as follows: "If a function $f(t)$ contains no frequencies higher than f cycles per second it is completely determined by giving its ordinates at a series of points spaced ($1/2f$) seconds apart." A mathematical version of this theorem can be obtained by convolving the Fourier transform of the signal to be sampled with the Fourier transform of an infinite sequence of impulse functions

$$F_S(\omega) = \frac{1}{2\pi}[F(\omega) * S(\omega)] \tag{1}$$

or,

$$F_S(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S(\tau)F(\tau - \omega)d\omega \tag{2}$$

Where, $F_S(\omega) =$ sampled signal spectrum

$F(\omega) =$ original signal spectrum

$S(\omega) =$ spectrum for a sequence of impulses

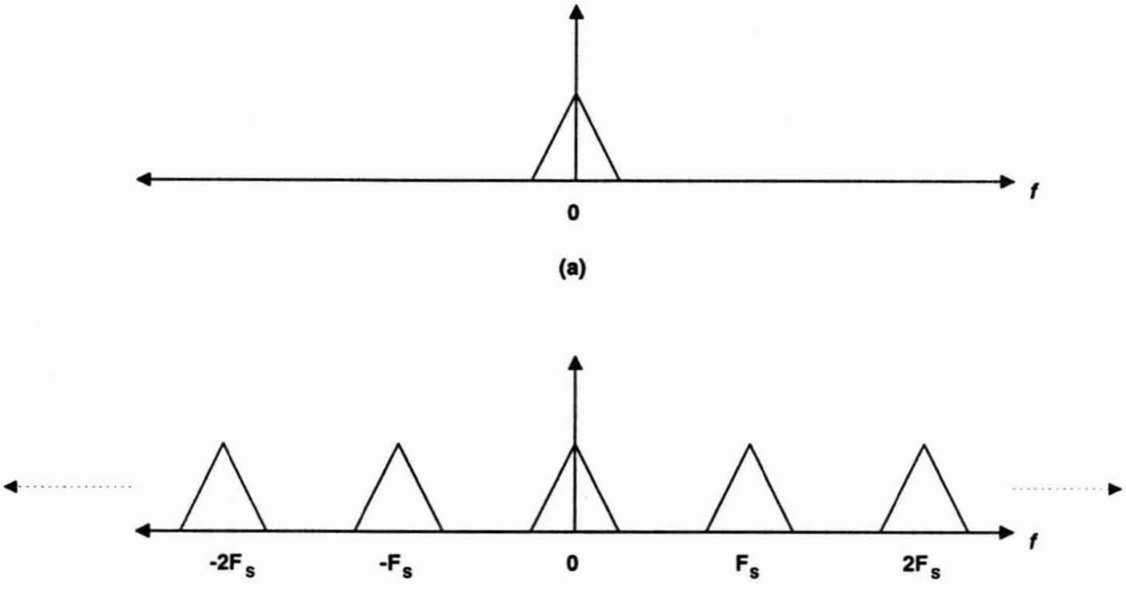
$\omega = 2\pi f$ (radian frequency).

The result of the convolution in equation (2) is the original signal spectrum repeated at multiples of the sampling frequency, see Figure 1. Notice that if the sampling frequency is less than twice the bandwidth of the original signal the replicas centered at multiples of the sampling frequency will overlap and distort the original. This undesirable phenomenon is *aliasing*. To avoid aliasing,

$$f_S \geq 2B. \tag{3}$$

Where, $f_S =$ sampling frequency in Hz

$B =$ bandwidth of original signal in Hz.



(a)

(b)

Figure 1: Fourier transform of (a) continuous time signal and (b) sampled signal.

Shannon's sampling theorem is mathematically accurate. Although, in most cases it is not practical to sample a signal at exactly twice it's highest frequency. Band-limiting is necessary to avoid aliasing. For $f_s=2B$ the band-limiting filter must have a so called "brick wall" roll-off at frequency B. A filter that matches this requirement is physically unrealizable. Several factors contribute to the actual sampling frequency used. Generally there is a compromise between the complexity of the band-limiting filter versus the cost of the analog to digital converter (ADC). As f_S becomes closer to $2B$, the band-limiting filter requires more stages to give the desired roll-off. As f_S increases, the required conversion time necessitates a faster ADC. Cost for ADCs is inversely proportional to conversion time, as conversion time decreases, cost rises.

2.2 Uniform Quantization [3, 4, 9]

Figure 2 illustrates the transfer characteristic of a seven level uniform quantizer. To represent the quantized output $q(n)$ as a binary number would require 3 bits. Once a signal has been sampled it is discrete in time. However, the amplitude remains continuous. The quantized version of a signal is obtained by applying the sampled signal to a binary encoder where the discrete voltage levels are assigned to the nearest binary numbers. The complete process, combining sampling and amplitude quantization, is known as PCM.

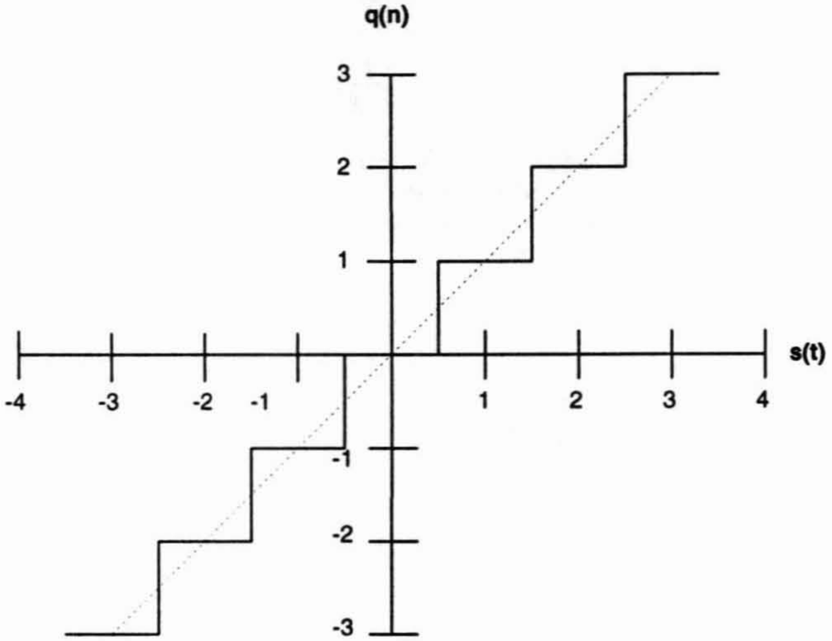


Figure 2: Uniform quantizer transfer characteristic.

The noise introduced by PCM is primarily due to the rounding to the "nearest" binary number. If a signal is quantized to eight levels (3 bits) using a quantizer transfer characteristic similar to the one shown in Figure 2, the finest resolution is the full scale magnitude divided by eight. In general,

$$\frac{A}{2^n} = \alpha . \tag{4}$$

Where, A = full scale amplitude

n = number of bits per sample

α = difference between quantization levels (i.e. finest resolution).

The uncertainty error due to rounding is based on the assumption that there is a continuous range of values within α, all of which are equally likely to have been the actual value of the original signal (uniform distribution). The error signal ε is the difference between the original signal amplitude and the quantized sample value. As a result, the mean square uncertainty error can be solved for by finding the expected value of error squared over the range of $-\alpha/2$ to $\alpha/2$

$$E(\varepsilon^2) = \frac{1}{\alpha} \int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \varepsilon^2 d\varepsilon . \tag{5}$$

Where, E = expected value operator

ε = difference between actual and quantized signal levels.

Performing the integration in equation (5) yields an expression which is equivalent to quantization noise power

$$N_{OUT}^2 = \frac{\alpha^2}{12} . \qquad (6).$$

Taking the square root of both sides gives the root mean square (RMS) noise voltage

$$N_{OUT} = \frac{\alpha}{2\sqrt{3}}. \tag{7}$$

The maximum signal-to-noise ratio (SNR) for a uniformly quantized signal can be calculated by finding the ratio of the full scale quantization level to the noise voltage in equation (7). The full scale quantization level is simply the total number of quantization levels multiplied by the minimum quantization increment α

$$S_{OUT_{MAX}} = \frac{\alpha(2^n)}{2}. \tag{8}$$

Where, n = number of bits in quantizer.

The ratio of equations (7) and (8) yields the SNR

$$SNR = \frac{2^n}{\sqrt{3}}. \tag{9}$$

In dB,

$$SNR_{dB} = 4.77 + 6.02n\,. \tag{10}$$

Equation (10) is an objective measure of quality in systems employing uniform quantization. It should be noted: the SNR calculated in equation (10) is a theoretical maximum. In practice other factors (e.g. power supply noise) tend to reduce the final SNR. Also, the human voice is considered to have about 40 dB of dynamic range, however, during most conversations it is typically about 20 dB down from maximum. In other words, we generally do not shout during normal conversation. Consequently, the average signal to noise ratio for uniformly quantized speech is about 20 dB less than what would be calculated using equation (10).

Another objective measure of quality which can be derived in a similar manner is dynamic range. Dynamic range pertains to the resolution of a quantization scheme. It is the ratio of the full scale amplitude to the smallest quantized amplitude change,

$$DR = \frac{1}{2}\left(\frac{\alpha 2^n}{\alpha}\right) = 2^{n-1}. \tag{11}$$

In dB,

$$DR_{dB} = 6.02(n-1)\,. \tag{12}$$

2.3 Non-uniform Quantization [1, 7, 9]

To this point the discussion has been based strictly on uniform quantization (linear speech coding). That is, waveforms are quantized such that all signal levels have the same resolution. An alternative to linear quantization is to make α fine for low level signals and coarse for high level signals, introducing a non-uniform quantizer characteristic. This type of quantization can result in improved dynamic range for a given number of bits and effectively raise the SNR for lower level signals. The drawback is lower maximum SNR—equations 9 and 10 are not valid for non-uniform quantization. Figure 3 shows a transfer characteristic for a seven level non-uniform quantizer. Notice, when compared to the uniform quantizer transfer characteristic shown in Figure 2, there are three quantization levels for the input $s(t)$ between zero and one, where there is only one with the uniform quantizer.

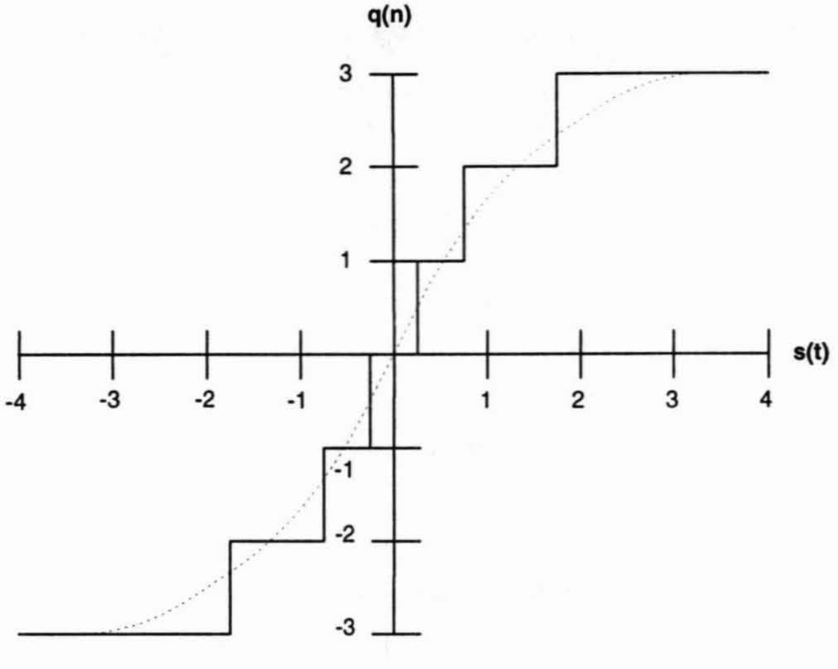


Figure 3: Non-uniform quantizer transfer characteristic.

A complete digital communication system, incorporating non-uniform speech coding, compresses the quantized signal at the transmitter then expands the signal back to linear form at the receiver. The compressed signal requires fewer bits and therefore consumes less BW. Ideally, the expander transfer function is the exact inverse of the compressor and is able to reproduce the original uncoded analog signal. In literature pertaining to telecommunications, the words *compressor* and *expander* are generally combined in to a single word; *compandor.*

Companding is on of the most popular forms of non-uniform quantization. When compared to uniform quantization, it allows for bandwidth compression without degradation in dynamic range, at the expense of peak signal to noise ratio. For example, a signal uniformly quantized to 14 bits, using equations (10) and (12), would have a peak SNR and DR of approximately 89 dB and 78 dB respectively. If the same signal is non-uniformly quantized (compressed) using only 8 bits (256 levels), the minimum quantization level can be set such that DR of 78 dB can be retained, although the peak SNR will be degraded. Degradation in the peak SNR is due to the course quantization levels used for the large amplitude signals (where fine quantization is not necessary). Low amplitude signals are quantized at finer resolution (more steps, where it is necessary). Consequently, the SNR at low signal levels is improved when compared to uniform quantization with the same number of levels. Essentially, companding strives to make SNR constant over the dynamic range of the quantizer.

2.3.1 μ-Law Companding [1, 9]

Most forms of non-uniform quantization are derived from a logarithmic transfer function. That is, the output signal is proportional to the log of the input signal. In North America and Japan, digital telecommunications networks employ μ-law companding as the standard for PCM encoding (μ=255 for North America). The general form of the transfer characteristic is

$$y(x) = sign(x)\frac{\ln(1+\mu|x|)}{\ln(1+\mu)}. \tag{13}$$

Where, $-1 \le x \le 1$

x = input signal

$y(x)$ = compressed output signal

$sign(x)$ = polarity of input signal.

2.3.2 Uniform versus Non-uniform Quantization [7]

An accepted method of objectively measuring quality in signal processing systems is SNR. In the context of digital coding this would more accurately be called: signal to quantization noise ratio (SQR). Equation (10) was derived to calculate the SNR for uniform quantization assuming maximum input signal. To find SNR for input signal amplitudes less than maximum equation (10) must be rewritten

$$SNR_{dB} = 4.77 + 6.02n + 20\log\left(\frac{S_i}{S_{MAX}}\right). \tag{14}$$

Where, S_i = input signal level

S_{MAX} = maximum signal level.

When the quantization characteristic is not uniform (14) is no longer valid. To clarify the performance of companded quantization, the SNR must be calculated for a full range of input signal levels. For μ-law companding the signal to noise ratio is given by the following equation [9],

$$SNR_{\mu(dB)} = 10\log\left[\frac{3(2^{2n})}{[\ln(1+\mu)]^2\left[1+\frac{1.732}{\mu S_i}+\frac{1}{\mu^2 S_i^2}\right]}\right]. \tag{15}$$

It should be noted that as $\mu \to 0$, equation (15) is equivalent to equation (14), thus $\mu = 0$ implies uniform quantization. Figure 4 compares SNR versus relative input signal power for 256 level non-uniform quantization ($\mu = 255$) and 256 level uniform quantization.

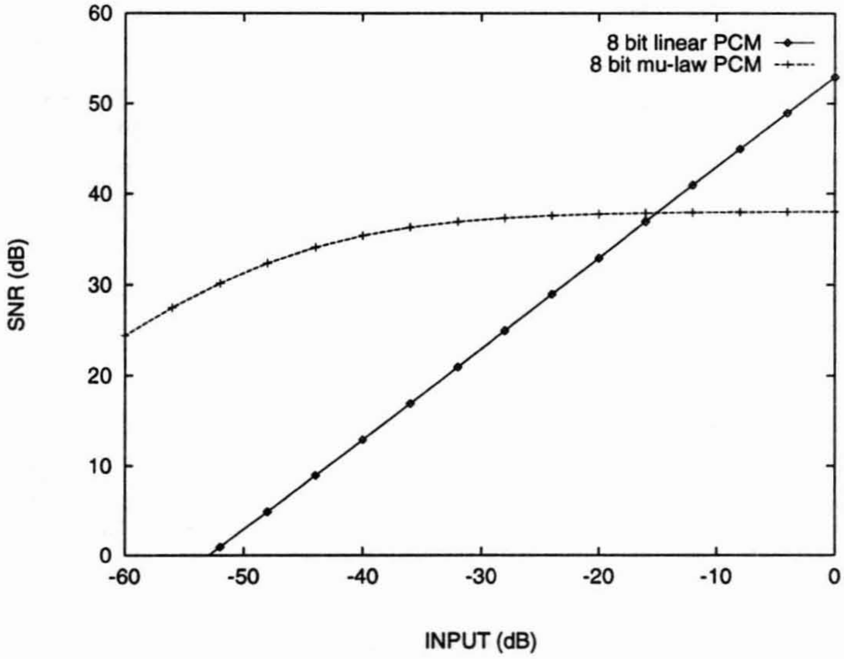


Figure 4: SNR versus input level for 8 bit μ-law and 8 bit uniform quantization.

2.4 Differential Quantization [4, 8]

Differential quantization is a coding technique where the difference between the present sample and the predicted value for the next sample is quantized. This type of quantization is advantageous because the difference signal dynamic range (variance) is less than the unprocessed input signal. Consequently, fewer quantization levels are required to retain the same Signal-to-Noise Ratio (SNR). Alternatively, the number of quantization levels can remain the same allowing the difference signal to be encoded using all the available bandwidth resulting in greater resolution and improved signal quality.

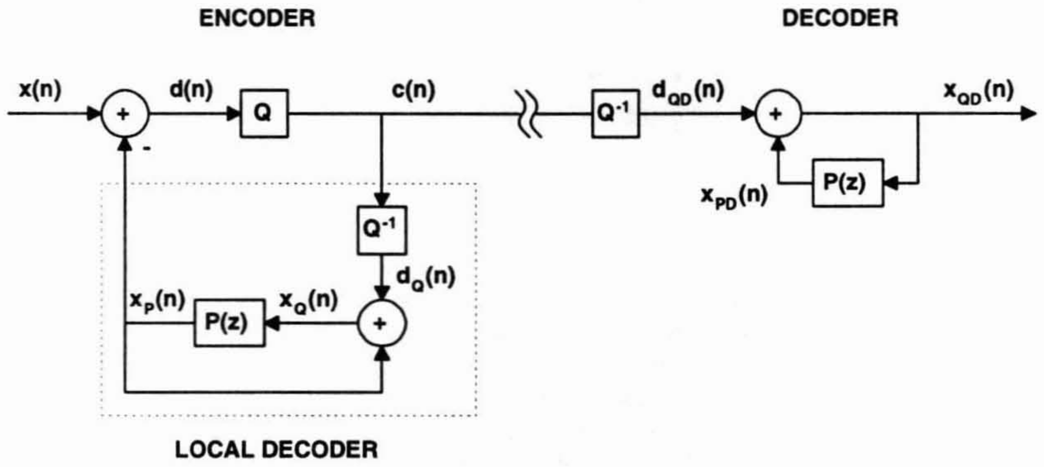


Figure 5: Differential quantization block diagram.

Figure 5 is a block diagram displaying a differential quantization system. All signals are represented in discrete time notation implying that *x(n)* is the discrete time version of *x(t)*. Notice the decoder is in the feedback path of the encoder. Thus, the decoder is performing the inverse of the encoder. The block labeled **Q** converts the difference signal *d(n)* in to a binary representation suitable for transmission and the block labeled $\mathbf{Q}^{-1}$ does the inverse. In reality, the process of converting *d(n)* to *c(n)* and back to $d_{QD}(n)$ is a significant factor in the non-ideal behavior of differential quantization. Nevertheless, fundamental analysis of the system is simplified by assuming blocks **Q** and $\mathbf{Q}^{-1}$ cancel. Employing this assumption, the transfer function of the encoder in z-domain terms

$$H_{ENC}(z) = \frac{C(z)}{X(z)} = Q(z)[1 - P(z)]\,. \tag{16}$$

And the decoder transfer function is

$$H_{DEC}(z) = \frac{X_{QD}(z)}{C(z)} = \frac{1}{Q(z)[1 - P(z)]}\,. \tag{17}$$

If $D_{QD}(z) \cong D(z)$, then $X_{QD}(z) \cong X(z)$ and the entire system transfer function can be written as,

$$H(z) = H_{ENC}(z)H_{DEC}(z) = 1\,. \tag{18}$$

Although equation (18) is based on several assumptions, it shows a differential quantization system patterned after the topology displayed in Figure 5 can be made to produce an output signal which approximates the original input signal. The quality of the approximation is what distinguishes various differential quantization schemes. Generally, high quality approximation does not come without a price.

A crucial element in differential quantization is the predictor $P(z)$. The output $x_P(n)$ of $P(z)$ is a weighted sum of past input samples. The general form is equivalent to a finite impulse response (FIR) filter

$$x_P(n) = \sum_{k=1}^{P} a_k x_Q(n-k)\,. \tag{19}$$

Where, P = order of predictor

a_k = weighting factor (coefficient)

$x_P(n)$ = output of predictor

$x_Q(n) = d_Q(n) + x_P(n)$ (input to predictor).

Applying the z-transform to equation (19) yields the transfer function for the predictor

$$P(z) = \frac{X_P(z)}{X_Q(z)} = \sum_{k=0}^{P} a_k z^{-k}\,. \tag{20}$$

Equations (19) and (20) show that the predictor output is a linear combination of past inputs giving rise to the term "linear prediction." Non-linear predictors (non-linear combination of past input samples) have been studied, however, due to complexity and stability issues, their popularity is limited.

The coefficients a_k are calculated such that $P(z)$ will provide a reasonably accurate model for the behavior of human speech. In 1966 a paper was published by McDonald [6] suggesting coefficients, based on normalized autocorrelation of human speech samples, for predictors of order one to ten. Later, in 1972, Noll [4] published similar data. These two papers are generally referenced in determination of predictor coefficients. Assuming that $P(z)$ does provide a reasonably accurate model for human speech, $x_Q(n) \equiv x(n)$ and $d(n) \rightarrow 0$. In other words, a good predictor should minimize the difference signal $d(n)$. This is the basis for differential quantization. In most DM algorithms the predictor order P is set to one.

The potential for instability in differential quantizers exists in the encoder. As mentioned early, equation (20) is the transfer function of an FIR filter. One of the significant characteristics of FIR filters is, by definition, they are stable (the transfer function has only zeros). However, when an FIR is placed in a feedback path, as is the case with the encoder, the zeros become poles—if one of these poles finds its way outside the unit circle the differential quantizer will be unstable.

3. Delta Modulation [1, 4, 6, 8, 10]

DM is a differential quantization scheme that uses two level quantization (i.e. one bit quantizer). By using a single bit to represent each sample, the sample rate and the bit rate are equivalent. Consequently, sample rate is directly related to signal quality (SNR). Also, BW of the input signal and band-limiting of the output are significant factors in determining signal quality.

The first DM algorithm was conceived in 1946. During the last 50 years, two algorithms; Linear DM (LDM) and CVSD, received a significant amount of attention from those interested in efficient methods to digitize speech. LDM is the most fundamental, least complex form of DM. Hence, this tutorial will attempt to provide an understanding of LDM as a foundation for understanding more complex DM algorithms. The CVSD algorithm, an accepted standard in the tactical community and finding a growing number of applications in "point-to-point" wireless applications, will also be covered.

3.1 Linear DM [1, 4, 6, 8]

The predictor $P(z)$ in LDM is first order and the quantizer **Q** is two level. Figure 6 is a flow diagram describing the LDM encoder and decoder algorithms.

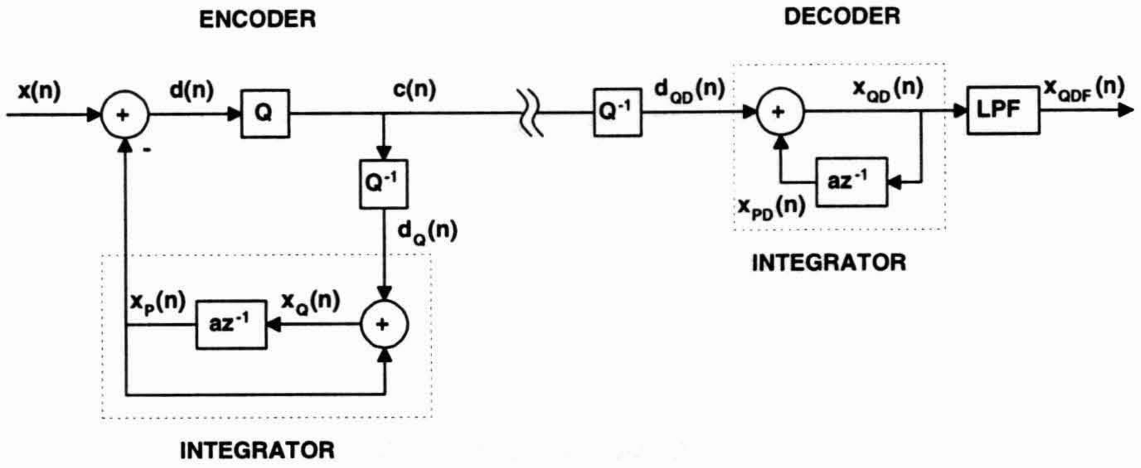


Figure 6: LDM block diagram.

The predictor is shown as a single tap FIR filter with transfer function $P(z) = az^{-1}$. In the encoder, the transfer function between $d_Q(n)$ and $x_P(n)$ can be expressed in the z-domain terms as

$$\frac{X_P(z)}{D_Q(z)} = \frac{az^{-1}}{1 - az^{-1}} \tag{21}$$

In the decoder, the transfer function between $d_{QD}(n)$ and $x_{QD}(n)$ is

$$\frac{X_{QD}(z)}{D_{QD}(z)} = \frac{1}{1 - az^{-1}} \tag{22}$$

Equations (21) and (22) represent discrete time integrators (if $a = 1$). If $a < 1$ they become damped or lossy integrators. McDonald [6] and Noll [4] both suggest $a = 1$ for optimum prediction gain. A pure integrator ($a = 1$) will cause bit errors to propagate longer than if $a < 1$. In practice, a value of $a < 1$ is preferred.

The quantizer **Q** in figure 6 functions like a comparator. When the input $d(n)$ exceeds zero it outputs a logic one, when the input is less then zero the output is a logic zero. Hence, the output of **Q** is a single bit indicating the sign of the magnitude of $d(n)$. The inverse quantizer **Q**$^{-1}$ converts logic levels to delta $d_Q(n)$ as shown in the table below.

sign of $d(n)$	$c(n)$	$d_Q(n)$
-	0	$-\Delta$
+	1	Δ

Table 1: Sign of $d(n)$ with corresponding logic levels and deltas.

The value of Δ plays an important role in the performance of LDM. If Δ is relatively small, tracking of slowly changing, low amplitude signals is quite good at the expense of poor tracking for fast, abruptly changing signals. When DM is not able to keep up with the input signal a phenomena called *slope overload* is exhibited, as shown in Figure 7.

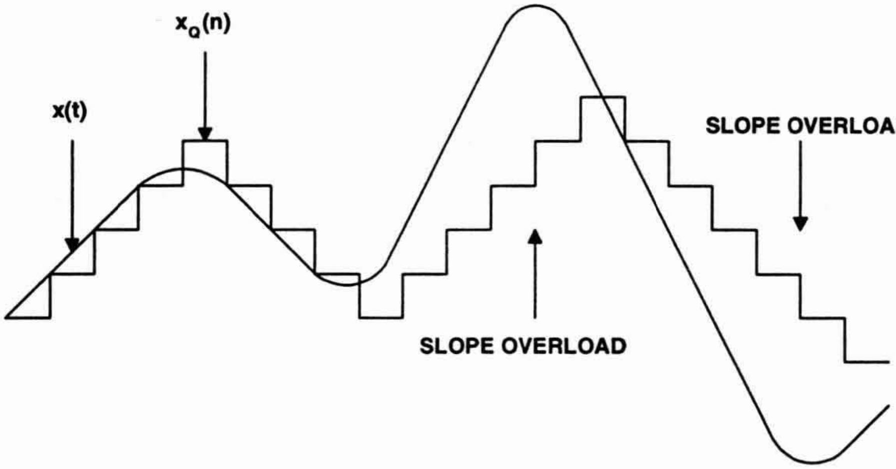


Figure 7: Slope overload in LDM.

Increasing the value of Δ can lessen the effects of slope overload but creates a new problem; *granular noise*. With Δ to large, low amplitude signals will not be quantized at fine enough levels and they appear as *idle channel noise* , see Figure 8. The idle channel pattern is simply an alternating one-zero sequence indicating the input signal amplitude is not changing. Since an alternating one-zero bit pattern has a mean value of zero, the signal out of the decoder will integrate to zero.

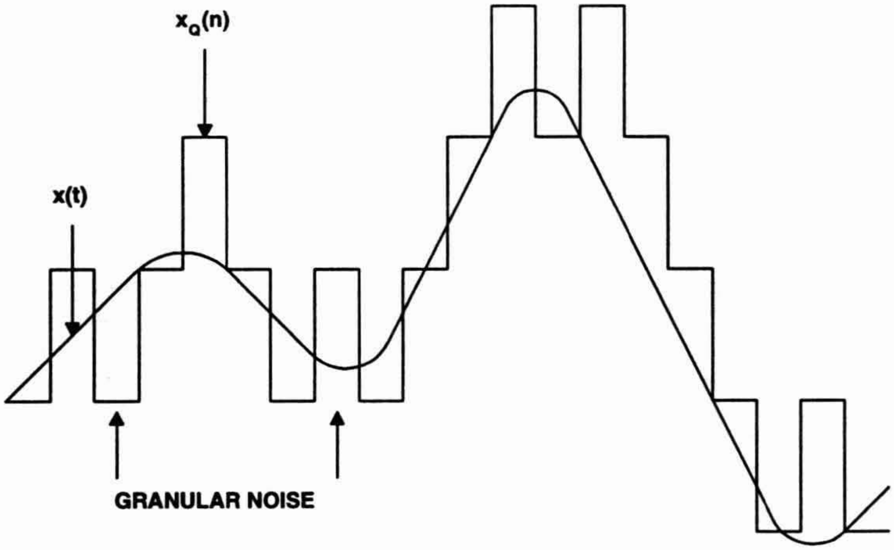


Figure 8: Granular noise in LDM.

3.2 CVSD [2, 4, 10]

Issues with granularity and slope overload can be drastically reduced by making dynamic adjustments to the quantizer step size Δ. Adaptive DM (ADM) algorithms attempt to do this by making Δ small for slowly changing signals and large for rapidly changing signals. The most publicized ADM algorithm is known as CVSD. It was first proposed by Greefkes and Riemens in 1970 [2]. In their CVSD algorithm, adaptive changes in Δ are based on the past three or four sample outputs (i.e. $c(n)$, $c(n-1)$, $c(n-2)$, $c(n-3)$). Figure 9 and Figure 10 show flow diagrams of the algorithms for the encoder and decoder respectively. Notice only the last three samples of $c(n)$ are used here.

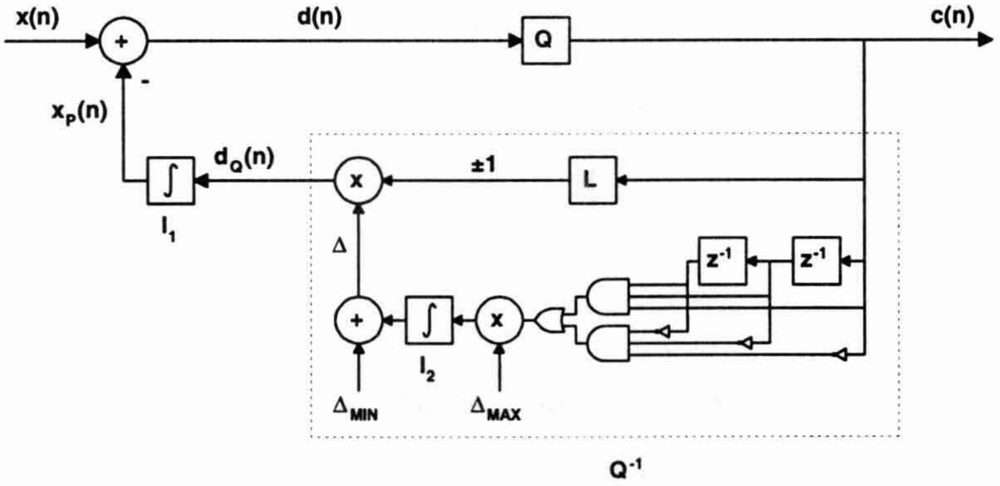


Figure 9: CVSD encoder block diagram.

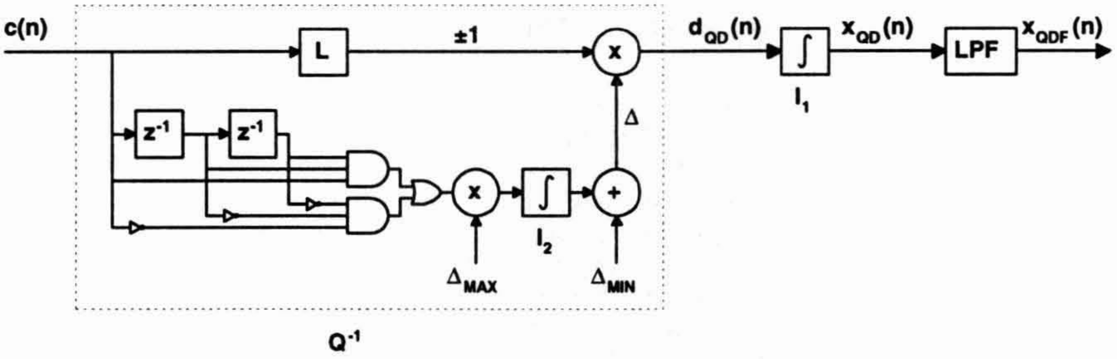


Figure 10: CVSD decoder block diagram.

The block labeled $\mathbf{Q^{-1}}$, previously shown in Figure 6, has been replaced by two cascaded one sample delays (z^{-1}) and logic to determine when three consecutive ones or zeros have occurred. The minimum and maximum step height is set by Δ_{MIN}. and Δ_{MAX}, respectively. When strings of three consecutive zeros or ones have not occurred for a period of time long enough for the output of the integrator $\mathbf{I_2}$ to decay to near zero, the algorithm is equivalent to LDM (section 3.1). The time constants for the integrator $\mathbf{I_2}$ and integrator $\mathbf{I_1}$ are typically 4 ms and 1 ms respectively. In CVSD literature integrator $\mathbf{I_1}$ is referred to as the *principle integrator* and integrator $\mathbf{I_2}$ as the *syllabic integrator*. The so called *syllabic integrator* derives its name from the length of syllable. Actually a syllable is about 100 ms in duration, however, pitch changes are on the order of 10 ms. Consequently, 4 ms seems to work best for the CVSD *syllabic* (*pitch*) time constant. The block labeled **L** performs simple level conversion (i.e. $c(n) = 1$, **L** outputs 1; $c(n) = 0$, **L** outputs -1). This CVSD algorithm is also known as "Digitally Controlled DM" [10].

Figure 11 displays the output of the integrator **I₁** ($x_P(n)$ in the encoder and $x_{PD}(n)$ in the decoder). When compared to Figure 7 and Figure 8 slope overload and granular noise are reduced.

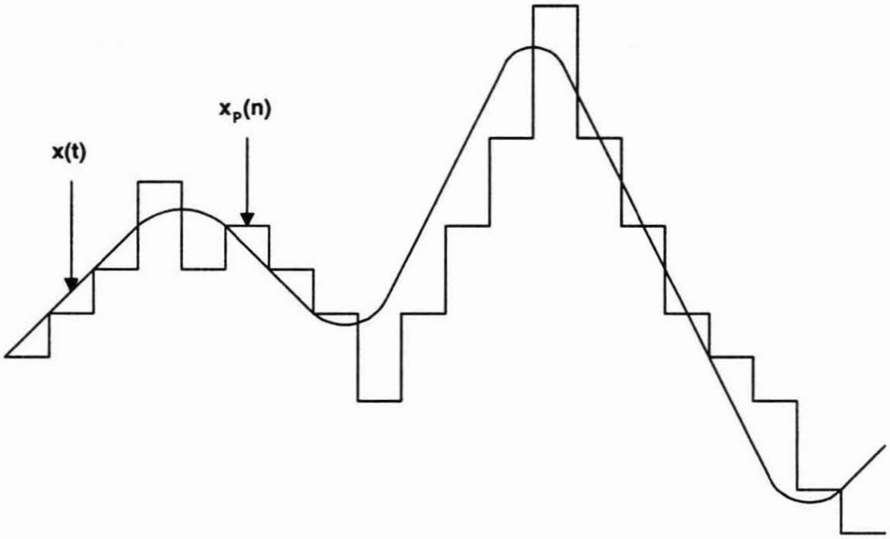


Figure 11: CVSD quantization noise.

3.3 Performance Measurement of DM [1,4]

The maximum SNR for DM speech coders is [1]

$$SNR_{dB} = 10\log\left(\frac{f_S^3}{f_{BW}f^2}\right) - 14.0\,. \tag{23}$$

Where, f_S = data rate (sample rate)

f_{BW} = signal BW (cutoff frequency of LPF)

f = signal frequency.

Most literature on DM coding agrees on the terms involving f_S, f_{BW}, and f in equation (23) but most do not agree on -14 dB. This term varies from -17.0 dB to -11.7 dB depending on a variety of different input signals and assumptions about environment. Nevertheless, equation (23) is considered a maximum because it assumes no slope overload and minimum granular noise, i.e. optimum step size.

The adaptive behavior of CVSD results in a SNR versus input level characteristic similar to non-uniform quantization (mentioned in section 2.3). This non-linear SNR characteristic is due to *companding*, where the quantization level (slope) is adjusted to a larger or smaller value according to past pitch changes of the input signal. The number of past samples (bits) used to make a prediction is normally three or four. Four bit *companding* has proven to be most effective for data rates greater than 32 Kb/s, three bit *companding* seems to work better for data rates less than 32 Kb/s.

Figure 12 shows a typical SNR versus input level characteristic for 32 Kb/s CVSD (four bit *companding* algorithm, input signal = 820 Hz sinewave). Equation (23) predicts a maximum SNR of 27.6 dB which is nearly met in Figure 12 for and input signal level of -15 dbm0 (0 dBm0 = 489 mVrms). Above and below the -15 dBm0 input level granular and slope overload noise start cause distortion. Finally, It should be noted that CVSD does not perform well with continuous tone or data input signals, particularly at data rates below 32 Kb/s.

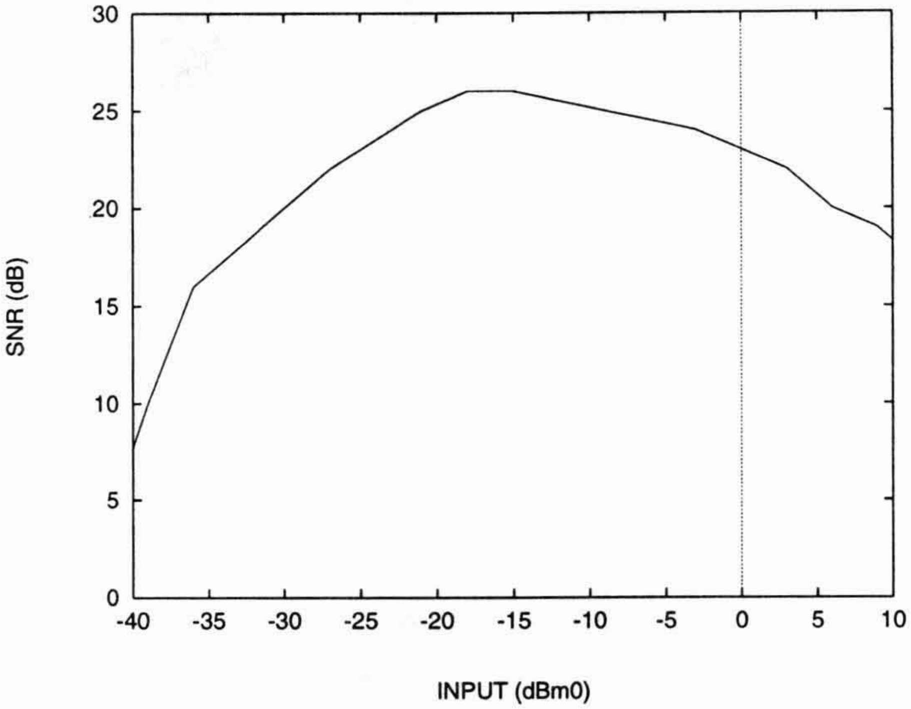


Figure 12: Measured SNR versus input level for 32 Kb/s CVSD (input = 820 Hz sinewave).

SNR is the most used method to objectively quantify performance of speech coding algorithms. However, it does not always correspond with perceived quality, particularly for differential and adaptive algorithms using actual voice as the input. In addition, it is difficult to make reliable SNR measurements in the presence of random bit errors. In an effort to quantify the perceived quality of a speech coding algorithm, *Mean Opinion Score* (MOS) testing was developed [4]. Table 2 summarizes the five point scale used to judge quality and impairment.

Number	Quality	Impairment
5	excellent	imperceptible
4	good	perceptible but not annoying
3	fair	slightly annoying
2	poor	annoying
1	bad	very annoying

Table 2: Mean Opinion Score testing guidelines.

An MOS rating of 4 to 4.5 is considered *Toll Quality* (equivalent to commercial telephony). Where as *Communication Quality* MOS ratings are 3 to 4 (barely perceptible distortion, but no degradation in intelligibility).

Figure 13 compares MOS ratings for μ-law PCM (the standard for *Toll Quality*), CVSD and ADPCM. Notice CVSD performs as well or better than both μ-law PCM and ADPCM in the presence of bit errors. Specifically, CVSD retains quite good MOS ratings at bit error rates exceeding 1%, and at 10% has an MOS rating of 3 (*Communication Quality*). It is this robustness to bit errors (channel noise) that makes CVSD an ideal solution for many wireless speech communication applications.

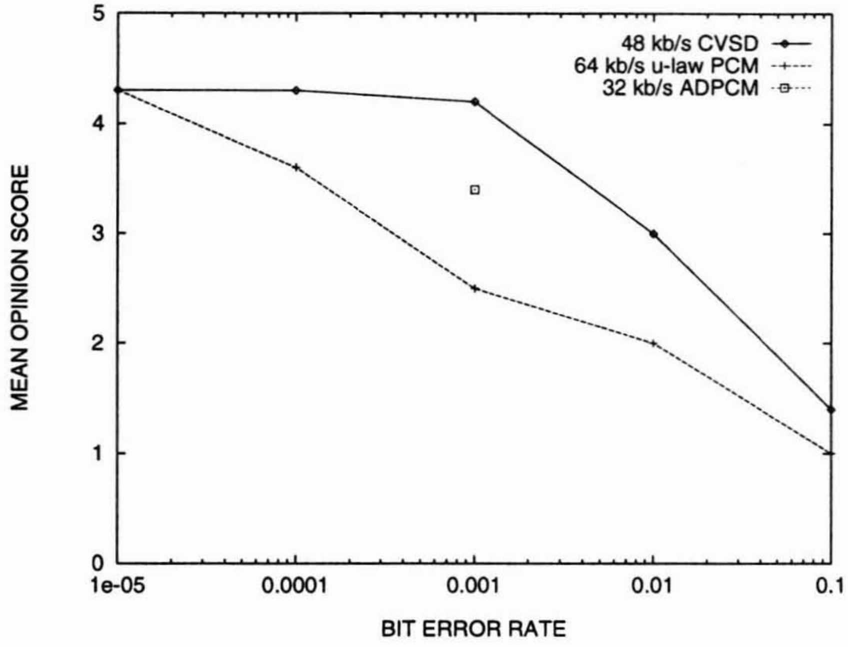


Figure 13: MOS versus bit error rate for ADPCM, μ-law PCM, and CVSD from [4].

4. Summary

CVSD has several attributes that make it well suited for digital coding of speech. One bit words eliminate the need for complex framing schemes. Robust performance in the presence of bit errors make error detection and correction hardware unecessary. Other speech coding schemes may require a digital signal processing engine and external analog to digital/digital to analog converters to convert the analog signal in to a form that can be processed digitally—the entire CVSD codec algorithm, including input and output filters, can be integrated on a single silicon substrate. Despite this simplicity, CVSD has enough flexibility to allow digital encryption for secure applications. Finally, CVSD can operate over a wide range of data rates—it has been successfully used from 9.6 kB/s to 64Kb/s. At 9.6Kb/s audio quality is not particularly good, however, it is intelligible. At data rates of 24 Kb/s to 48 Kb/s it is judged as quite acceptable. And above 48 Kb/s it is comparable to *toll quality*. All of these attributes make CVSD attractive to wireless telecommunication systems (e.g. digital cordless telephones, digital Land Mobile Radio). The defence industry has been using CVSD for decades in wireline and wireless systems as specified in Mil-Std-188-113. More recently, Federal Standard 1023 proposed CVSD for 25 Khz channel radios operating above 30 Mhz. Figure 14 is a block diagram showing a CVSD Codec in a digital mobile radio system.

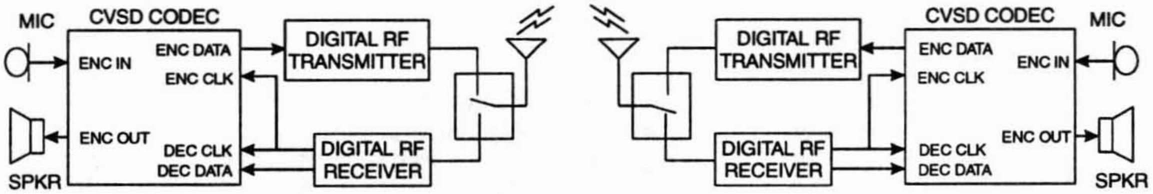


Figure 14: Digital wireless system incorporating CVSD Codec.

This tutorial has attempted to shed some light on the fundamental aspects of CVSD. It has shown that CVSD is a differential adaptive quantization algorithm with one bit coding and first order prediction (one bit ADPCM). In addition, objective and subjective methods of measuring signal quality showing that CVSD performs quite well in the presence of bit errors (noisy channel) have been presented.

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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX609

An Audio Delay circuit based on the MX609 CVSD Codec

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1. Introduction

The schematic diagram shown on the following page is an audio delay circuit based on the MX609 CVSD Codec. In addition to the MX609, the circuit uses a Motorola MCM6287 64K x 1 bit RAM, two 4520 counter ICs, and a 4069 inverter chip. It provides up to two seconds of delay. This circuit provides a starting point for a designer who wishes to implement an audio delay circuit. MX-COM makes no guarantee of its performance and assumes no responsibility for its use in any product.

2. Circuit Operation

In the following operational description, a bar over a signal name is used to indicate an active low signal. For example, W is an active low write enable signal. On the MX609P, Clock Mode 1, pin 22, is tied to VDD and Clock Mode 2, pin 21, is tied to ground to set the encode and decoder clocks for a sampling rate of 32 kb/s. The Encoder Force Idle, Powersave, and Decoder Force Idle inputs, pins 6, 15, and 16, respectively, are tied to VDD to set them inactive. The Data Enable input, pin 7, is tied to VDD to make the encoded data available at the Encoder Output, pin 5. Pin 19, the Algorithm select input, is tied to ground to select a four-bit companding algorithm. The other inputs are the same as recommended for "External Component Connections" shown in the MX-COM data book.

The audio signal to be delayed is input to pin 10 of the MX609, the Encoder Input, and is converted to a serial stream of digital data. The serial data are output on pin 5, the Encoder Output, and connected to pin 13, the D input, of the MCM6287 memory chip. The Decoder Data Clock output from pin 18 of the MX609 is connected to pin 1 of the 4069 inverter. The output of the inverter, pin 2, is connected to pin 10 of the MCM6287, the W input, and to pin 3 of the 4069, the input to second inverter. Pin 4, the inverter output, is connected to the enable input of the first 4520 counter.

The enable input is taken from the second inverter to ensure that the 4520 counters increment after the W signal into the MCM6287 transitions from low to high. The clock inputs of each of the 4520s, pins 1 and 9, are tied to ground so that only the enable inputs control when the counters increment. The reset inputs, pins 7 and 15, are also tied to ground so that they never reset the counters. The individual four bit counters in the 4520s are cascaded to produce a 16 bit counter. The counter outputs, Q15 - Q0, are connected to the address inputs, A15 - A0, of the MCM6287.

There are switches between Q15 and A15 and between Q14 and A14. The switches allow the number of bits of the counter, and therefore the length of the delay, to be adjusted. When the Decoder Data Clock falls from high to low, the counter, and therefore the address, increments. Since the W input to the memory, pin 17, is the complement of the clock, it rises from low to high, latching the encoded data bit at the D input. The E input to the MCM6287, pin 12, is tied to ground so that the memory is always selected. When W is high and the address is stable, a valid data bit appears at the Q output, pin 17, of the MCM6287. The address of the data bit appearing at Q is one greater than the address of the bit that was just written, so the counter must cycle through its entire range before a data bit that has been written into the memory can be read. Therefore, a data bit output from the MX609 at the Encoder Output pin is delayed by the number of clock periods of the range of the counter. The delay is given by:

Delay = (T sec/cycle) * (2N cycles)

Where: T = period of Decoder Data Clock
N = number of bits used in counter

If all 16 bits of the counter are used, and the decoder clock frequency is 32 kHz, then the delay would be:

Delay: = (1/32000) sec/cycle * (216) cycles
= 2.048 seconds

In this example, all locations of the memory are used. If a shorter delay is desired, the switches connecting the counter outputs and address inputs can be opened. If only 14 bits of the counter are used, then the delay is reduced by a factor of four, to 0.512 seconds. The range of delays could be increased even more by adding more switches and by making the sampling clock frequency adjustable. The Q output, pin 9, of the MCM6287 is connected to the Decoder Input, pin 17, of the MX609. The decoder clocks in the serial digital data stream from the memory and converts it to an analog signal, which is output at pin 13, the Decoder Output. The Decoder Output is the delayed audio signal.

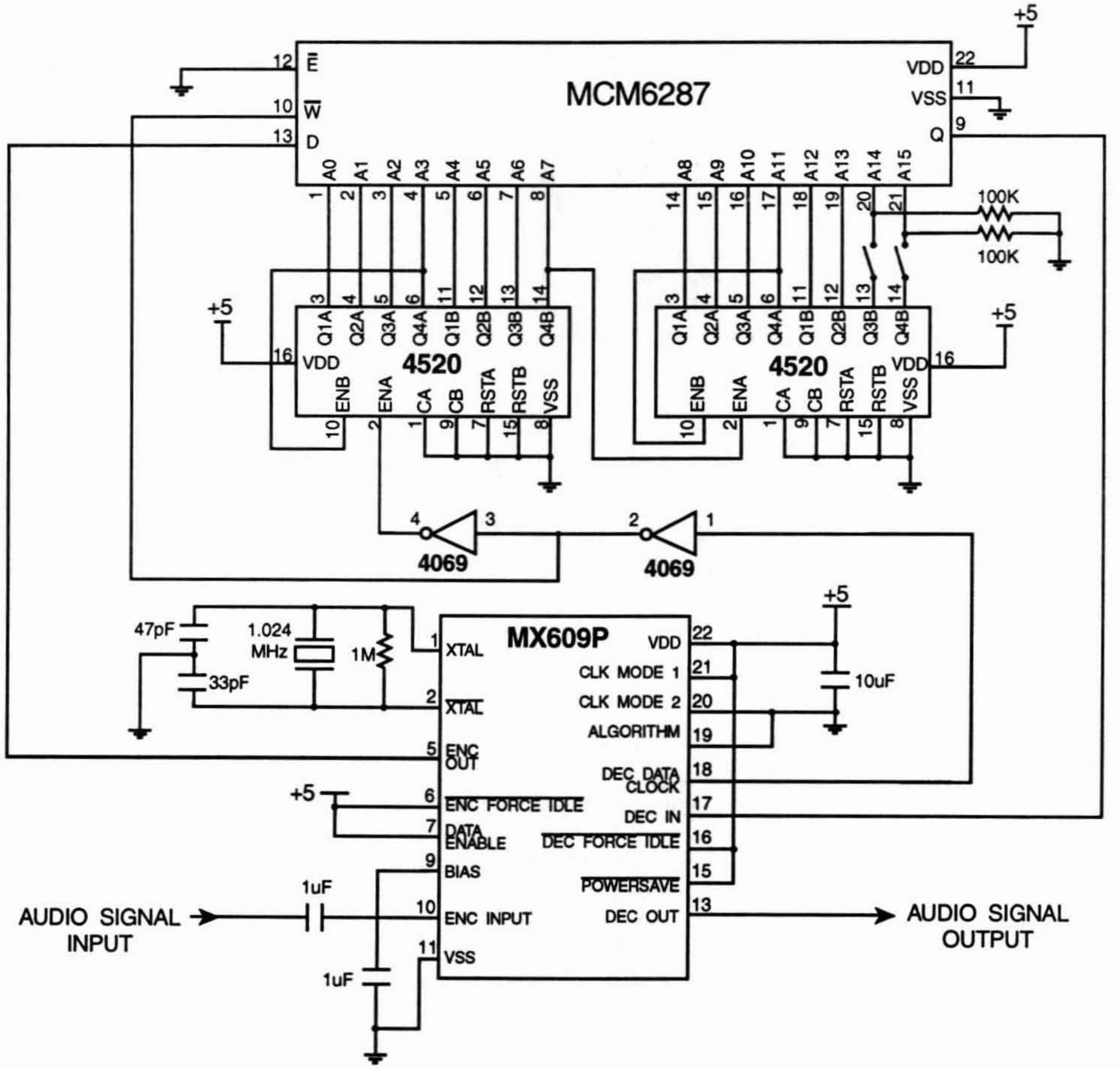
+5
MCM6287
12 E
10 W
13 D
VDD 22
VSS 11
Q 9
A0 A1 A2 A3 A4 A5 A6 A7
A8 A9 A10 A11 A12 A13 A14 A15
100K
100K
4520
4520
Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B
VDD 16
ENB ENA CA CB RSTA RSTB VSS
4069
4069
MX609P
XTAL
XTAL
ENC OUT
ENC FORCE IDLE
DATA ENABLE
BIAS
ENC INPUT
VSS
VDD
CLK MODE 1
CLK MODE 2
ALGORITHM
DEC DATA CLOCK
DEC IN
DEC FORCE IDLE
POWERSAVE
DEC OUT
47pF
33pF
1.024 MHz
1M
10uF
1uF
1uF
AUDIO SIGNAL INPUT
AUDIO SIGNAL OUTPUT

Figure 1: Audio Delay Circuit

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Generation of Non-Standard CTCSS Tones

MX-COM manufactures several integrated circuits that encode and decode CTCSS tones at the EIA RS-220 standard frequencies. In many instances, however, using tones of slightly different frequencies may be desirable. Because these MX-COM ICs use switched capacitor technology, tone frequencies may shifted simply by changing the crystal or clock input. The following five tables list alternative tones that can be encoded and decoded by the MX165C (Table 4), MX365A (Table 2), MX465 (Table 5), and the MX375 (Table 3), and encoded by the MX315A (Table 1).

Each table lists the tone frequencies for three crystal values for each chip. The MX165C, MX315A and MX365A use a nominal crystal value of 1.0 MHz; the table lists tone frequencies for 1.008 MHz and 1.024 MHz crystals as well as for 1.0 MHz. The MX375 and MX465 uses a 4.0 MHz nominal crystal value; these tables lists frequencies for 4.0 MHz, 4.032 MHz, and 4.096 MHz crystals. The column labeled as "Divisor" for each table lists the quotient of the clock frequency divided by the tone frequency. This column can be used to calculate the clock frequency required to generate other tone frequencies. Each table also lists the D5-D0 program code input associated with each divisor and tone frequency group. Each code is listed in both binary and hexadecimal formats. As an example, to encode a 70.0 Hz tone with the program code input D5-D0 = 011111 = 1F Hex, the required clock would be calculated in the following manner:

D5	D4	D3	D2	D1	D0
0	1	1	1	1	1

Divisor = 13908

Tone frequency = 70.0 Hz

Required clock frequency = Divisor * Tone Frequency
= 13908 * 70.0 Hz
= 973560 Hz

When using these ICs in this manner, you must remember the following:

1. When the clock is changed, the audio pass band limits will change proportionately. These changes will be fairly small, however. For example, in the MX165C using a 1.024 MHz crystal, the lower limit will change to (1.024/1.0) * 300 = 307 Hz, and the upper limit will change to (1.024/1.0) * 3000 = 3072 Hz.
2. In the MX375, the frequency inversion carrier frequency will also change proportionately from its nominal value of 3333 Hz. For example, with a 4.096 MHz clock, the carrier frequency will change to (4.096/4.0) * 3333 Hz = 3413 Hz. For proper communication, the transmitter and receiver must use the same inversion carrier frequency.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

MX315A										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						HEX
Divisor	1.0 MHz	1.008 MHz	1.024 MHz	D5	D4	D3	D2	D1	D0	
14912	67.06	67.60	68.67	1	1	1	1	1	1	3F
14415	69.37	69.93	71.04	1	1	1	0	0	1	39
13920	71.84	72.41	73.56	0	1	1	1	1	1	1F
13454	74.33	74.92	76.11	1	1	1	1	1	0	3E
12989	76.99	77.61	78.84	0	0	1	1	1	1	0F
12555	79.65	80.29	81.56	1	1	1	1	0	1	3D
12121	82.50	83.16	84.48	0	1	1	1	1	0	1E
11718	85.34	86.02	87.39	1	1	1	1	0	0	3C
11284	88.62	89.33	90.75	0	0	1	1	1	0	0E
10943	91.38	92.11	93.57	1	1	1	0	1	1	3B
10540	94.88	95.64	97.16	0	1	1	1	0	1	1D
10261	97.46	98.24	99.80	1	1	1	0	1	0	3A
10013	99.87	100.67	102.27	0	0	1	1	0	1	0D
9672	103.39	104.22	105.87	0	1	1	1	0	0	1C
9331	107.17	108.03	109.74	0	0	1	1	0	0	0C
9021	110.85	111.74	113.51	0	1	1	0	1	1	1B
8711	114.80	115.72	117.56	0	0	1	0	1	1	0B
8432	118.60	119.55	121.45	0	1	1	0	1	0	1A
8122	123.12	124.10	126.07	0	0	1	0	1	0	0A
7843	127.50	128.52	130.56	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7316	136.69	137.78	139.97	0	1	1	0	0	0	18
7068	141.48	142.61	144.88	0	0	1	0	0	0	08
6851	145.96	147.13	149.46	0	1	0	1	1	1	17
6603	151.45	152.66	155.08	0	0	0	1	1	1	07
6386	156.59	157.84	160.35	0	1	0	1	1	0	16
6169	162.10	163.40	165.99	0	0	0	1	1	0	06
5952	168.01	169.35	172.04	0	1	0	1	0	1	15
5766	173.43	174.82	177.59	0	0	0	1	0	1	05
5549	180.21	181.65	184.54	0	1	0	1	0	0	14
5363	186.46	187.95	190.94	0	0	0	1	0	0	04
5177	193.16	194.71	197.80	0	1	0	0	1	1	13
4929	202.88	204.50	207.75	0	0	0	0	1	1	03
4836	206.78	208.44	211.75	1	1	1	0	0	0	38
4743	210.84	212.53	215.90	0	1	0	0	1	0	12
4588	217.96	219.70	223.19	0	0	0	0	1	0	02
4433	225.58	227.38	230.99	0	1	0	0	0	1	11
4278	233.75	235.62	239.36	0	0	0	0	0	1	01
4123	242.54	244.48	248.36	0	1	0	0	0	0	10
3999	250.06	252.06	256.06	0	0	0	0	0	0	00

Table 1: MX315A

MX365A										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						HEX
Divisor	1.0 MHz	1.008 MHz	1.024 MHz	D5	D4	D3	D2	D1	D0	
14914	67.05	67.59	68.66	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.90	72.48	73.63	0	1	1	1	1	1	1F
13450	74.35	74.94	76.13	1	1	1	1	1	0	3E
12994	76.96	77.58	78.81	0	0	1	1	1	1	0F
12536	79.77	80.41	81.68	1	1	1	1	0	1	3D
12108	82.59	83.25	84.57	0	1	1	1	1	0	1E
11712	85.38	86.06	87.43	1	1	1	1	0	0	3C
11285	88.61	89.32	90.74	0	0	1	1	1	0	0E
10919	91.58	92.31	93.78	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10279	97.29	98.07	99.62	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.43	104.26	105.91	0	1	1	1	0	0	1C
9333	107.15	108.01	109.72	0	0	1	1	0	0	0C
9028	110.77	111.66	113.43	0	1	1	0	1	1	1B
8723	114.64	115.56	117.39	0	0	1	0	1	1	0B
8418	118.80	119.75	121.65	0	1	1	0	1	0	1A
8143	122.80	123.78	125.75	0	0	1	0	1	0	0A
7869	127.08	128.10	130.13	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7320	136.61	137.70	139.89	0	1	1	0	0	0	18
7076	141.32	142.45	144.71	0	0	1	0	0	0	08
6832	146.37	147.54	149.88	0	1	0	1	1	1	17
6619	151.09	152.30	154.72	0	0	0	1	1	1	07
6374	156.88	158.14	160.65	0	1	0	1	1	0	16
6161	162.31	163.61	166.21	0	0	0	1	1	0	06
5947	168.14	169.49	172.18	0	1	0	1	0	1	15
5764	173.48	174.87	177.64	0	0	0	1	0	1	05
5551	180.15	181.59	184.47	0	1	0	1	0	0	14
5368	186.29	187.78	190.76	0	0	0	1	0	0	04
5185	192.86	194.40	197.49	0	1	0	0	1	1	13
4910	203.65	205.28	208.54	0	0	0	0	1	1	03
4758	210.17	211.85	215.21	0	1	0	0	1	0	12
4575	218.58	220.33	223.83	0	0	0	0	1	0	02
4422	226.12	227.93	231.55	0	1	0	0	0	1	11
4270	234.19	236.06	239.81	0	0	0	0	0	1	01
4148	241.08	243.01	246.87	0	1	0	0	0	0	10
3996	250.28	252.28	256.29	0	0	0	0	0	0	00

Table 2: MX365A

MX375										
				Program codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary codes						HEX
Divisor	4.0 MHz	4.032 MHz	4.096 MHz	D5	D4	D3	D2	D1	D0	
59657	67.05	67.59	68.66	1	1	1	1	1	1	3F
55633	71.90	72.48	73.63	0	1	1	1	1	1	1F
53800	74.35	74.94	76.13	1	1	1	1	1	0	3E
51975	76.96	77.58	78.81	0	0	1	1	1	1	0F
50144	79.77	80.41	81.68	1	1	1	1	0	1	3D
48432	82.59	83.25	84.57	0	1	1	1	1	0	1E
46849	85.38	86.06	87.43	1	1	1	1	0	0	3C
45142	88.61	89.32	90.74	0	0	1	1	1	0	0E
43678	91.58	92.31	93.78	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41114	97.29	98.07	99.62	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38673	103.43	104.26	105.91	0	1	1	1	0	0	1C
37331	107.15	108.01	109.72	0	0	1	1	0	0	0C
36111	110.77	111.66	113.43	0	1	1	0	1	1	1B
34892	114.64	115.56	117.39	0	0	1	0	1	1	0B
33670	118.80	119.75	121.65	0	1	1	0	1	0	1A
32573	122.80	123.78	125.75	0	0	1	0	1	0	0A
31476	127.08	128.10	130.13	0	1	1	0	0	1	19
30379	131.67	132.72	134.83	0	0	1	0	0	1	09
29280	136.61	137.70	139.89	0	1	1	0	0	0	18
28305	141.32	142.45	144.71	0	0	1	0	0	0	08
27328	146.37	147.54	149.88	0	1	0	1	1	1	17
26474	151.09	152.30	154.72	0	0	0	1	1	1	07
25497	156.88	158.14	160.65	0	1	0	1	1	0	16
24644	162.31	163.61	166.21	0	0	0	1	1	0	06
23790	168.14	169.49	172.18	0	1	0	1	0	1	15
23057	173.48	174.87	177.64	0	0	0	1	0	1	05
22204	180.15	181.59	184.47	0	1	0	1	0	0	14
21472	186.29	187.78	190.76	0	0	0	1	0	0	04
20740	192.86	194.40	197.49	0	1	0	0	1	1	13
19642	203.65	205.28	208.54	0	0	0	0	1	1	03
19032	210.17	211.85	215.21	0	1	0	0	1	0	12
18300	218.58	220.33	223.83	0	0	0	0	1	0	02
17690	226.12	227.93	231.55	0	1	0	0	0	1	11
17080	234.19	236.06	239.81	0	0	0	0	0	1	01
16592	241.08	243.01	246.87	0	1	0	0	0	0	10
15982	250.28	252.28	256.29	0	0	0	0	0	0	00

Table 3: MX375

MX165C										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						Hex
Divisor	1.0MHz	1.008MHz	1.024MHz	D5	D4	D3	D2	D1	D0	
14930	66.98	67.52	68.59	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.901	72.48	73.63	0	1	1	1	1	1	1F
13435	74.431	75.03	76.22	1	1	1	1	1	0	3E
12993	76.965	77.58	78.81	0	0	1	1	1	1	0F
12551	79.677	80.31	81.59	1	1	1	1	0	1	3D
12124	82.483	83.14	84.46	0	1	1	1	1	0	1E
11712	85.383	86.07	87.43	1	1	1	1	0	0	3C
11300	88.494	89.20	90.62	0	0	1	1	1	0	0E
10934	91.456	92.19	93.65	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10263	97.435	98.21	99.77	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.429	104.26	105.91	0	1	1	1	0	0	1C
9333	107.147	108.00	109.72	0	0	1	1	0	0	0C
9013	110.954	111.84	113.62	0	1	1	0	1	1	1B
8708	114.84	115.76	117.60	0	0	1	0	1	1	0B
8418	118.793	119.74	121.64	0	1	1	0	1	0	1A
8128	123.028	124.01	125.98	0	0	1	0	1	0	0A
7854	127.328	128.35	130.38	0	1	1	0	0	1	19
7595	131.674	132.73	134.83	0	0	1	0	0	1	9
7320	136.612	137.70	139.89	0	1	1	0	0	0	18
7076	141.323	142.45	144.71	0	0	1	0	0	0	8
6847	146.044	147.21	149.55	0	1	0	1	1	1	17
6603	151.441	152.65	155.08	0	0	0	1	1	1	7
6375	156.875	158.13	160.64	0	1	0	1	1	0	16
6161	162.311	163.61	166.21	0	0	0	1	1	0	6
5963	167.708	169.05	171.73	0	1	0	1	0	1	15
5749	173.936	175.33	178.11	0	0	0	1	0	1	5
5566	179.654	181.09	183.97	0	1	0	1	0	0	14
5368	186.289	187.78	190.76	0	0	0	1	0	0	4
5185	192.864	194.41	197.49	0	1	0	0	1	1	13
4911	203.645	205.27	208.53	0	0	0	0	1	1	3
4743	210.848	212.53	215.91	0	1	0	0	1	0	12
4590	217.853	219.60	223.08	0	0	0	0	1	0	2
4438	225.339	227.14	230.75	0	1	0	0	0	1	11
4285	233.359	235.23	238.96	0	0	0	0	0	1	01
4133	241.97	243.91	247.78	0	1	0	0	0	0	10
3995	250.282	252.28	256.29	0	0	0	0	0	0	00

Table 4: MX165C

MX465										
	Xtal Freq	Xtal Freq	Xtal Freq	Program Codes						
				Binary Codes						Hex
Divisor	4.0MHz	4.032MHz	4.096MHz	D5	D4	D3	D2	D1	D0	
59719	66.98	67.52	68.59	1	1	1	1	1	1	3F
57703	69.32	69.87	70.98	1	1	1	0	0	1	39
55632	71.901	72.48	73.63	0	1	1	1	1	1	1F
53741	74.431	75.03	76.22	1	1	1	1	1	0	3E
51972	76.965	77.58	78.81	0	0	1	1	1	1	0F
50203	79.677	80.31	81.59	1	1	1	1	0	1	3D
48495	82.483	83.14	84.46	0	1	1	1	1	0	1E
46848	85.383	86.07	87.43	1	1	1	1	0	0	3C
45201	88.494	89.20	90.62	0	0	1	1	1	0	0E
43737	91.456	92.19	93.65	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41053	97.435	98.21	99.77	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38674	103.429	104.26	105.91	0	1	1	1	0	0	1C
37332	107.147	108.00	109.72	0	0	1	1	0	0	0C
36051	110.954	111.84	113.62	0	1	1	0	1	1	1B
34831	114.84	115.76	117.60	0	0	1	0	1	1	0B
33672	118.793	119.74	121.64	0	1	1	0	1	0	1A
32513	123.028	124.01	125.98	0	0	1	0	1	0	0A
31415	127.328	128.35	130.38	0	1	1	0	0	1	19
30378	131.674	132.73	134.83	0	0	1	0	0	1	9
29280	136.612	137.70	139.89	0	1	1	0	0	0	18
28304	141.323	142.45	144.71	0	0	1	0	0	0	8
27389	146.044	147.21	149.55	0	1	0	1	1	1	17
26413	151.441	152.65	155.08	0	0	0	1	1	1	7
25498	156.875	158.13	160.64	0	1	0	1	1	0	16
24644	162.311	163.61	166.21	0	0	0	1	1	0	6
23851	167.708	169.05	171.73	0	1	0	1	0	1	15
22997	173.936	175.33	178.11	0	0	0	1	0	1	5
22265	179.654	181.09	183.97	0	1	0	1	0	0	14
21472	186.289	187.78	190.76	0	0	0	1	0	0	4
20740	192.864	194.41	197.49	0	1	0	0	1	1	13
19642	203.645	205.27	208.53	0	0	0	0	1	1	3
18971	210.848	212.53	215.91	0	1	0	0	1	0	12
18361	217.853	219.60	223.08	0	0	0	0	1	0	2
17751	225.339	227.14	230.75	0	1	0	0	0	1	11
17141	233.359	235.23	238.96	0	0	0	0	0	1	01
16531	241.97	243.91	247.78	0	1	0	0	0	0	10
15982	250.282	252.28	256.29	0	0	0	0	0	0	00

Table 5: MX465

The EIA RS-220 specification divides the standard frequencies into three groups. They are tabulated below with the program codes used in MX-COM ICs:

Group A	
Freq	Code
67.0	3F
77.0	0F
88.5	0E
100.0	0D
107.2	0C
114.8	0B
123.0	0A
131.8	09
141.3	08
151.4	07
162.2	06
173.8	05
186.2	04
203.5	03
218.1	02
233.6	01
250.3	00

Group B	
Freq	Code
71.9	1F
82.5	1E
94.8	1D
103.5	1C
110.9	1B
118.8	1A
127.3	19
136.5	18
146.2	17
156.7	16
167.9	15
179.9	14
192.8	13
210.7	12
225.7	11
241.8	10

Group C	
Freq	Code
74.4	3E
79.7	3D
85.4	3C
91.5	3B
97.4	3A
69.3	39
206.5	38

Table 6: EIA RS-220 Specifications Groups A, B, and C

Note that with the exception of the 67.0 Hz tone in Group A, the programming codes are in reverse sequential order in relation to the tone frequencies for each group. Again, with the exception of 67.0 Hz, also note that the first hexadecimal digit for Group A is 0, the first digit for Group B is 1, and the first digit for group C is 3.

For more general information about these ICs, see the MX-COM Product Handbook and the MX-COM MX165C, MX315A, MX365A, MX375, and MX465 Data Bulletins.

MX-COM does not test its CTCSS ICs (MX165C, MX315A, MX365A, MX375, and MX465) at crystal or clock frequencies other than the nominal frequency specified in the Performance Specifications section of the Data Bulletin, and as such, makes no guarantee of the performance of the device when used with a non-specified crystal or clock frequency. MX-COM does not assume responsibility for the use of its ICs in the manner described in this application note in any circuit or product.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Tone Generation - An Application of the MX105A

This Application Note describes how to configure an MX105A as a tone generator. It may be helpful to refer to the current MX105A data sheet before reading this document. The MX105A was primarily designed as a tone detector with user configurable center frequency, detection band width and response/de-response time (refer to the MX105A data sheet for this use). However, it can also be configured as a low distortion sinusoidal tone generator with minimal filtering. Figure 1 depicts a recommended circuit configuration for tone generation. Figure 2 details the circuit of Figure 1 by showing a block diagram of the active circuits in the MX105A used for tone generation.

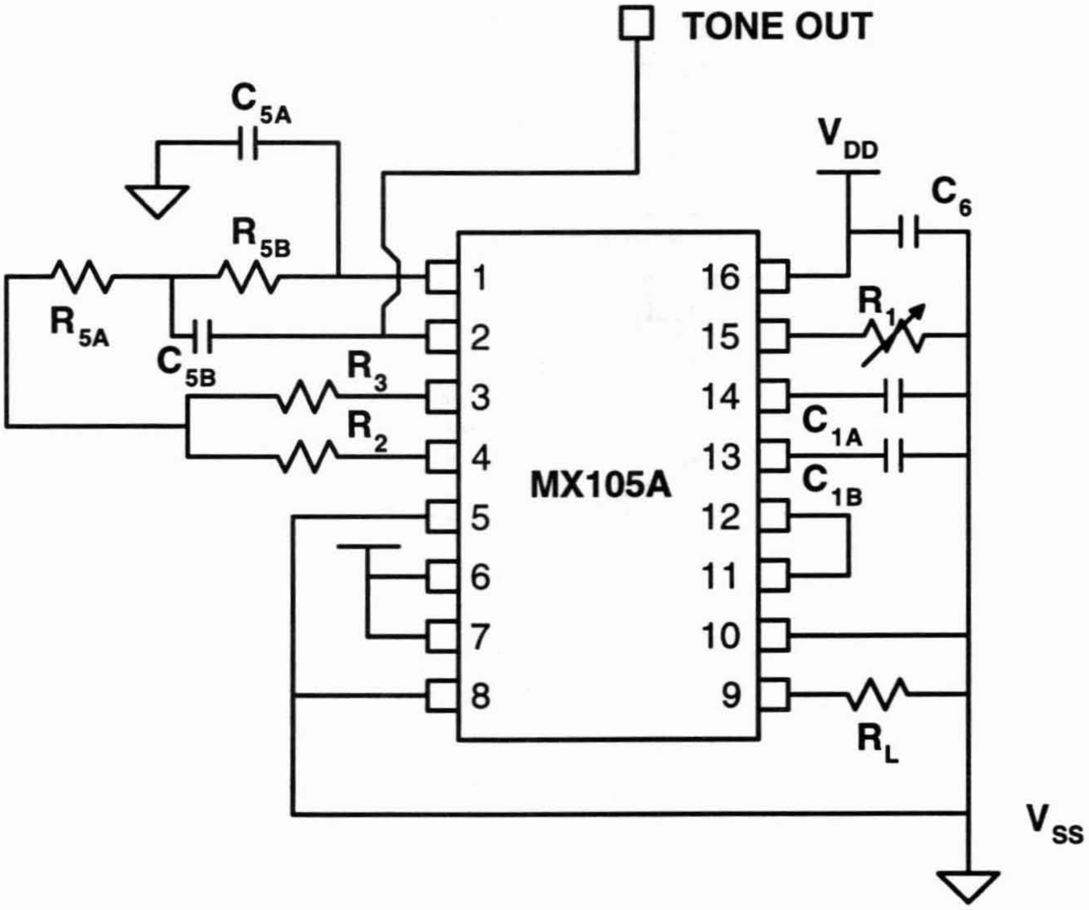

Figure 1. Simple Tone Generation Circuit using MX105A.

1. Circuit Description for Tone Generation.

An RC oscillator (pins 13-15) generates an internal clock at six times the center frequency. This clock is internally decoded to sequentially enable four analog switches configured between pins 3 and 5 (SW3A), pins 3 and 6 (SW3B), pins 4 and 7 (SW2A), and pins 4 and 8 (SW2B). The control signals for these switches are shown in Figure 3. The switch connections to R2 and R3 form a simple Digital to Analog converter to produce a three level approximation of a sine wave (1 1 0 -1 -1 0 . . .) as shown in Figure 3. This waveform is well suited for tone generation as described below. Finally, a simple low pass filter formed with the on chip buffer amplifier smoothes the three level sine wave to produce a low distortion sine wave.

Note: A large value DC blocking capacitor should be used at pin 2 if pins 6 and 7 are driven for tone level control or amplitude modulation as shown in Figure 2.

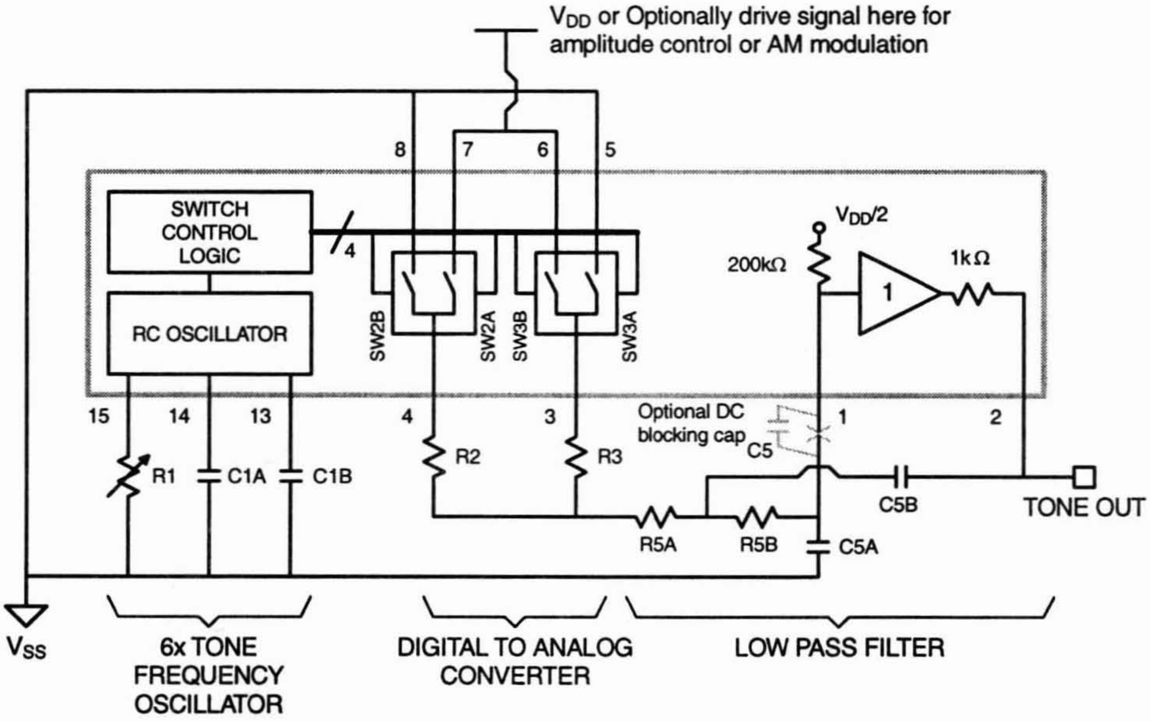
V_{DD} or Optionally drive signal here for amplitude control or AM modulation
8
7
6
5
SWITCH CONTROL LOGIC
4
RC OSCILLATOR
SW2B
SW2A
SW3B
SW3A
$V_{DD}/2$
200kΩ
1
1kΩ
15
14
13
4
3
Optional DC blocking cap
C5
1
2
R1
C1A
C1B
R2
R3
C5B
TONE OUT
R5A
R5B
C5A
V_{SS}
6x TONE FREQUENCY OSCILLATOR
DIGITAL TO ANALOG CONVERTER
LOW PASS FILTER

Figure 2. Block Diagram of Tone Generation Circuit.

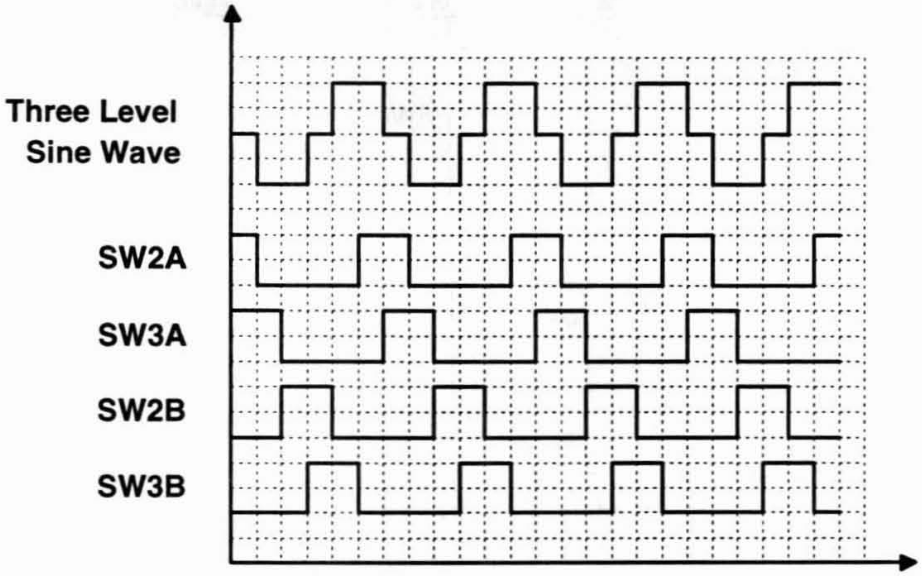

Figure 3. Internal Switch Control Signals and Resulting Three Level Waveform.

1.1 Fourier Series Analysis of the Three Level Waveform.

The periodic three level approximation of a sine wave can be represented by the following formula:

$$f(t) = \begin{cases} A & \text{for } |t| < \frac{T}{6} \\ 0 & \frac{T}{6} < |t| < \frac{T}{3} \\ -A & \text{for } \frac{T}{3} < |t| < \frac{T}{2} \end{cases} \qquad \text{where T is the period}$$

Fourier Series Expansion of f(t) yields the following coefficient formulas after some calculus:

$$\begin{aligned} a_n &= \frac{2}{T}\int_0^T f(t)\cdot\cos\left(n\cdot\frac{2\pi}{T}\cdot t\right)dt \\ &= \frac{2A}{n\cdot\pi}\sin\left(\frac{1}{3}\cdot n\cdot\pi\right)\cdot\left[1+2\cdot\cos\left(\frac{1}{3}\cdot n\cdot\pi\right)\right] \qquad \text{for positive integer n} \\ &= \frac{2\cdot A\cdot\sqrt{3}}{\pi}\left[\frac{1}{1},0,0,0,-\frac{1}{5},0,\frac{1}{7},0,0,0,-\frac{1}{11},0,\frac{1}{13},\ldots\right] \end{aligned}$$

$$b_n = \frac{2}{T}\int_0^T f(t)\cdot\sin\left(n\cdot\frac{2\pi}{T}\cdot t\right)dt = 0 \qquad \text{for positive integer n}$$

These coefficients result in the following fourier series representation:

$$f(t) = \frac{2\cdot A\cdot\sqrt{3}}{\pi}\left[\cos\left(\frac{2\pi}{T}t\right)-\frac{1}{5}\cos\left(5\frac{2\pi}{T}t\right)+\frac{1}{7}\cos\left(7\frac{2\pi}{T}t\right)-\frac{1}{11}\cos\left(11\frac{2\pi}{T}t\right)+\frac{1}{13}\cos\left(13\frac{2\pi}{T}t\right)+\ \ldots\right]$$

This function is plotted in the time domain in Figure 4 and in the frequency domain in Figure 5. It is clear from the frequency domain plot that the first harmonic spur above the fundamental, the fifth, is already about 14 dB down. Thus the required filtering to pass the fundamental while suppressing the harmonics is simplified compared to a square wave.

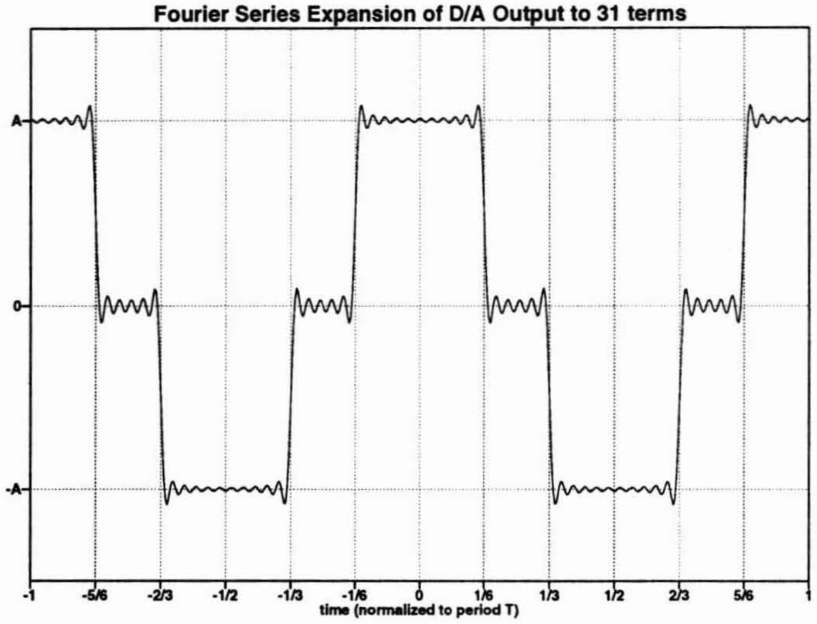

Figure 4. Time Domain Plot

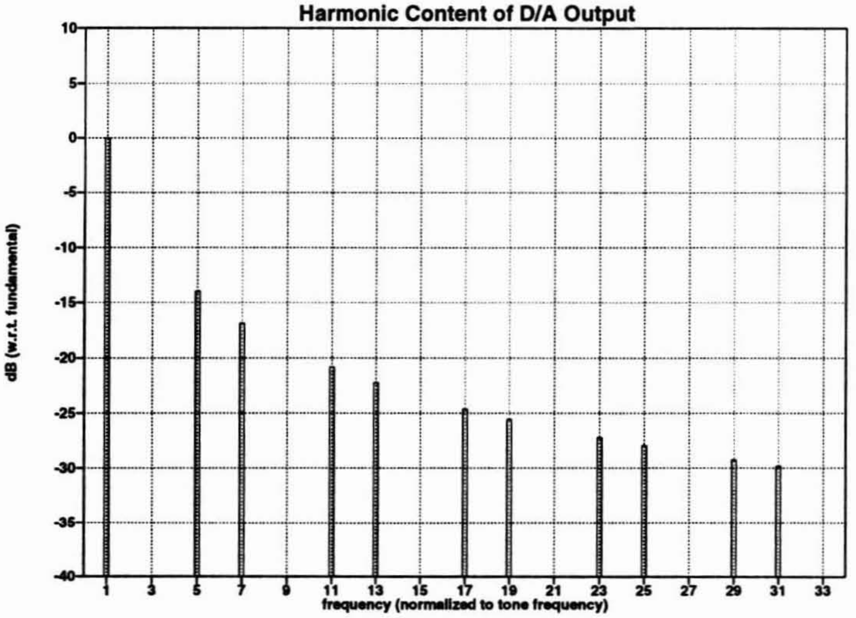

Figure 5. Frequency Domain Plot

1.2 Analysis of the Low Pass Smoothing Filter

A simple second order filter can provide 12 dB per octave roll-off in the filter's stop band. Thus we can expect as much as 27 dB (i.e. $27dB \approx 12 \cdot \log_2(5)$) attenuation of the fifth harmonic and above with such a filter.

This should produce a sine wave with distortion of about 1% (i.e. harmonics more than 40 dB down). More complex filtering can be used if lower distortion is required.

A simple second order low pass filter (formed with R5A, R5B, C5A, C5B, and the internal buffer amplifier between pins 1 and 2) suppresses the harmonics of the three level waveform to produce a low distortion (<1%) sine wave at pin 2. The transfer function of this low pass filter including effects of the input impedance of the MX105A buffer amplifier is:

$$\mathrm{H}(j\omega)=\frac{\left[\frac{\mathrm{Ri}}{\mathrm{R5A}+\mathrm{R5B}+\mathrm{Ri}}\right]\cdot\left[\frac{\mathrm{R5A}+\mathrm{R5B}+\mathrm{Ri}}{\mathrm{C5A}\cdot\mathrm{C5B}\cdot\mathrm{R5A}\cdot\mathrm{R5B}\cdot\mathrm{Ri}}\right]}{\left[\frac{\mathrm{R5A}+\mathrm{R5B}+\mathrm{Ri}}{\mathrm{C5A}\cdot\mathrm{C5B}\cdot\mathrm{R5A}\cdot\mathrm{R5B}\cdot\mathrm{Ri}}-\omega^2\right]+\left[\frac{1}{\mathrm{C5A}\cdot\mathrm{R5A}}+\frac{1}{\mathrm{C5A}\cdot\mathrm{R5B}}+\frac{1}{\mathrm{C5B}\cdot\mathrm{Ri}}\right]j\omega}$$

choosing to let R = R5A = R5B and C5A = 2 C5B and substituting C = C5B results in

$$\mathrm{H}(j\omega)=\frac{\left[\frac{\mathrm{Ri}}{2\mathrm{R}+\mathrm{Ri}}\right]\cdot\left[\frac{2\mathrm{R}+\mathrm{Ri}}{2\mathrm{C}^2\cdot\mathrm{R}^2\cdot\mathrm{Ri}}\right]}{\left[\frac{2\mathrm{R}+\mathrm{Ri}}{2\mathrm{C}^2\cdot\mathrm{R}^2\cdot\mathrm{Ri}}-\omega^2\right]+\left[\frac{1}{\mathrm{C}\cdot\mathrm{R}}+\frac{1}{\mathrm{C}\cdot\mathrm{Ri}}\right]j\omega}$$

From this expression the equation for the pole frequency is: (f_p is plotted in Figure 6 to help in component choices).

$$\omega_p{}^2=\left[\frac{2\mathrm{R}+\mathrm{Ri}}{2\mathrm{C}^2\cdot\mathrm{R}^2\cdot\mathrm{Ri}}\right]\quad\Rightarrow\quad f_p=\frac{\sqrt{\frac{2\mathrm{R}+\mathrm{Ri}}{2\mathrm{C}^2\cdot\mathrm{R}^2\cdot\mathrm{Ri}}}}{2\pi}$$

The equation for the Pass Band DC Gain is: (plotted in Figure 7 to help in component choices).

$$\text{DC Gain}=\frac{\mathrm{Ri}}{2\mathrm{R}+\mathrm{Ri}}$$

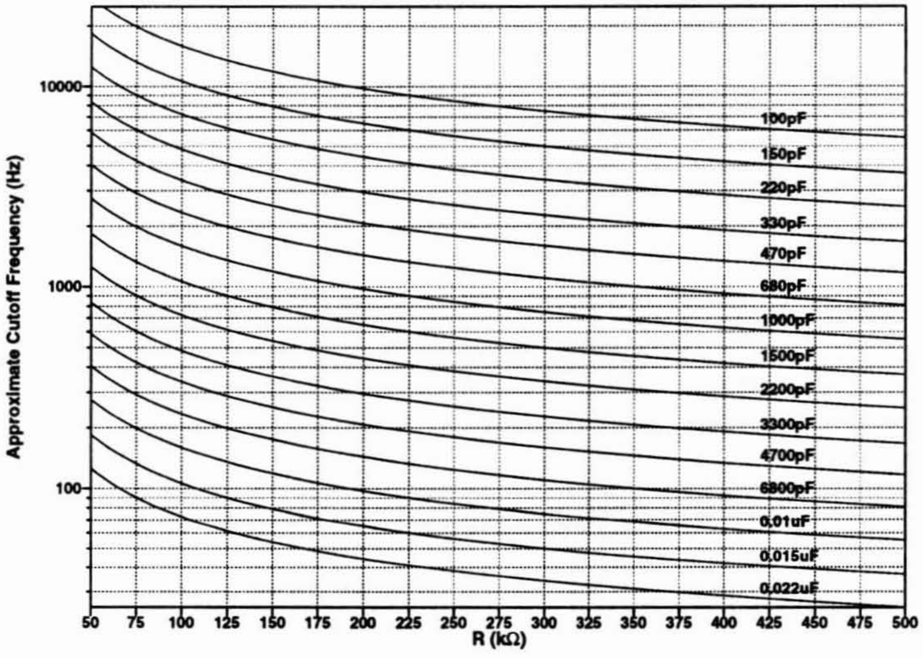

Figure 6. Approximate Cutoff Frequency Design Chart

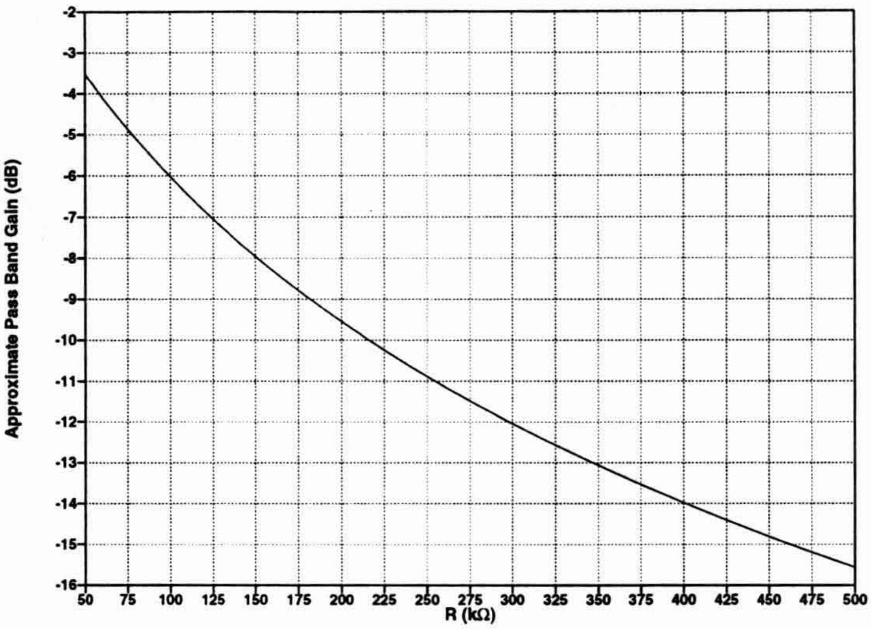

Figure 7. Approximate Filter Gain vs. R

Note that this filter provides attenuation in the pass band due to the input impedance of the buffer amplifier. The filtered tone level will be:

$$\text{Approximate Tone Level (in } V_{p\text{-}p}) = \frac{2 \cdot A \cdot \sqrt{3}}{\pi} \frac{Ri}{2R + Ri} \approx 1.1 \cdot A \cdot 10^{\left(\frac{\text{dB Gain}}{20}\right)}$$

where A is V_{DD} or optionally the level driven into pins 6 and 7 and dB Gain is read from Figure 7.

2. A Worked Design Example - 1700 Hz Tone Generator

The tone frequency is set according to the standard formula in the MX105A data sheet:

$$F_0 = \frac{1}{6 \cdot R1 \cdot C1A \cdot \ln(2)} \qquad \text{with } C1A = C1B$$

To generate a 1700 Hz tone while choosing C1A = C1B = 680pF

$$R1 = \frac{1}{6 \cdot F_0 \cdot C1A \cdot \ln(2)} = \frac{1}{6 \cdot 1800 \cdot 680 \cdot 10^{-12} \cdot \ln(2)} = 208\ \text{k}\Omega$$

Choosing R1 = 150kΩ in series with a 100kΩ potentiometer will allow frequency tuning if required.

Referring to Figure 6 to pick R after choosing C = 680pF for the low pass filter results in:

R = R5A = R5B = 130kΩ

C = C5B = 680pF and C5A = 2 x C5B ≈ 1500pF

Calculating the approximate pole frequency to check design choices:

$$f = \frac{\sqrt{\dfrac{2R + Ri}{C5A \cdot C5B \cdot R^2 \cdot Ri}}}{2\pi} = 1838\ \text{Hz} \quad \text{(seems reasonable)}$$

Calculating the approximate tone level for V_{DD} = 5V results in:

$$\text{Tone Level} = 1.1 \cdot A \cdot 10^{\left(\frac{-7}{20}\right)} = 2.46\ V_{p-p} = 870\ mV_{RMS}$$

If tone amplidude control is required, drive a DC level (A) into pins 6 and 7 and use DC blocking capacitor C5 as shown in Figure 2.

Finally, choose R3 and R2 sufficiently low compared to R so as not to significantly affect the filter's frequency response and gain. For example, choose R3 = R2 = 10kΩ.

The filter graphs and design example are based on the typical buffer input impedance of 200kΩ. This parameter varies from device to device and with supply voltage. The input impedance is approximately proportional to $\frac{4}{V_{DD} - 1}$ and may vary from 160kΩ to 360kΩ at VDD = 5V. These figures are given to help the designer analyze for device variation; they are not guaranteed specifications! Refer to the MX105A for all specifications. A smoothing filter built with an external amplifier may eliminate these issues.

Note: In this design example the filter cut off may vary from 1720 Hz to 2120 Hz and the filter gain may vary from -8.2 dB to -4.6 dB due to the buffer 's input impedance. Even with these variations the second order filter should provide good attenuation of the 1700 Hz tone's 5th harmonic and above.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX029

Dual Digitally Controlled Amplifier

1. Introduction

The MX029 is a single-chip LSI circuit comprised of two individual, digitally controlled gain sections. Control of each gain section is accomplished through the serial interface. Each section has 48 distinct gain steps (+/-48dB of range in 2dB steps) plus MUTE. As shown in Figure 1 both gain stages have switchable inputs. This switching allows for selection of three different input signals on one channel and two on the other channel. One of the channels also has output switching. These features make it very easy to use the MX029 as a summing amplifier.

The MX029 can also be used as a digital to analog converter(DAC). For this application we take advantage of the 48 distinct gain settings. With a single DC input voltage the variable gain of the amplifier can be used to generate an analog output signal. This application note describes both applications, the MX029 as a summing amplifier and DAC.

Whenever the MX029 is used in any application the input signal should be as noise free as possible. Cutting off the serial clock when it is not being used will reduce noise. With high gain settings a very small amount of noise is amplified and becomes a problem.

When serial loading the MX029 make sure that the serial clock, serial data and LOAD/LATCH timing is correct. This seems to be a common problem for users, especially the timing of the LOAD/LATCH line. Use a storage scope to check your timing.

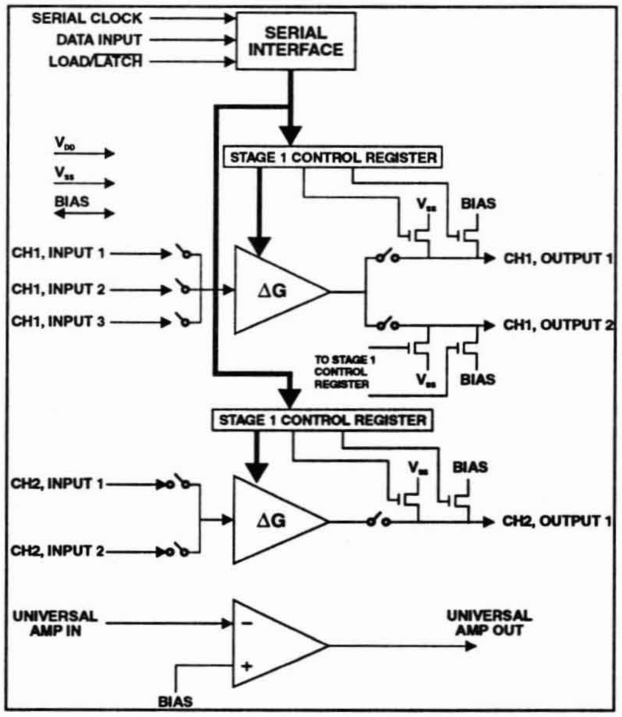
SERIAL CLOCK
DATA INPUT
LOAD/$\overline{\text{LATCH}}$
SERIAL INTERFACE
V_{DD}
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH1, INPUT 1
CH1, INPUT 2
CH1, INPUT 3
ΔG
CH1, OUTPUT 1
CH1, OUTPUT 2
TO STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
STAGE 1 CONTROL REGISTER
V_{SS}
BIAS
CH2, INPUT 1
CH2, INPUT 2
ΔG
CH2, OUTPUT 1
UNIVERSAL AMP IN
−
+
UNIVERSAL AMP OUT
BIAS

Figure 1: Device Block Diagram.

2. The MX029 as a Summing Amplifier

The MX029 can be used as a summing amplifier. Using channel one you can sum up to three different signals. With channel two you can sum two signals. As seen in Figure 2 very few external components are needed for the MX029 to be used as a summing amplifier.

The MX029 has an internal resistor that creates a voltage divider with R_{IN}. The configuration and value of this internal resistor is different in gain and attenuation mode, see Figure 2 and Figure 3. In gain mode the internal resistor is approximately 200KΩ and in attenuation mode the internal resistance is approximately 100KΩ. With a larger value of R_{IN} there will be more of a drop across R_{IN}. On the other hand, if the value of R_{IN} is too small the input source may not be able to drive R_{IN} due to source loading. Recommended values for R_{IN} are 10kΩ to 20kΩ. The equation used to calculate the signal level at the input of the MX029 for a two input summing amplifier is:

$$V_{IN029} = \frac{V_{IN1}(R_{IN2}R_L)}{R_{IN1}(R_{IN2}+R_L)+R_{IN2}R_L} + \frac{V_{IN2}(R_{IN1}R_L)}{R_{IN2}(R_{IN1}+R_L)+R_{IN1}R_L}$$

Where R_L is approximately 200KΩ in gain mode and 100KΩ in attenuation mode.

For a three input summing amplifier use the following equation :

$$V_{IN029} = \frac{V_{IN1}(R'//R_L)}{R_{IN1}+(R'//R_L)} + \frac{V_{IN2}(R''//R_L)}{R_{IN2}+(R''//R_L)} + \frac{V_{IN3}(R'''//R_L)}{R_{IN3}+(R'''//R_L)}$$

Where R' is the parallel combination of R_{IN2} and R_{IN3} (R_{IN2}// R_{IN3}) and R" = R_{IN1}//R_{IN3} and R''' = R_{IN1}//R_{IN2} and R_L is approximately 200KΩ in gain mode and 100KΩ in attenuation mode.

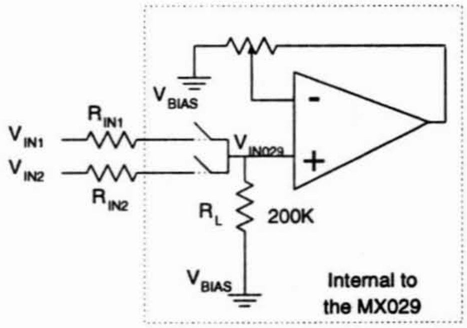

Figure 2: Gain Mode Configuration.

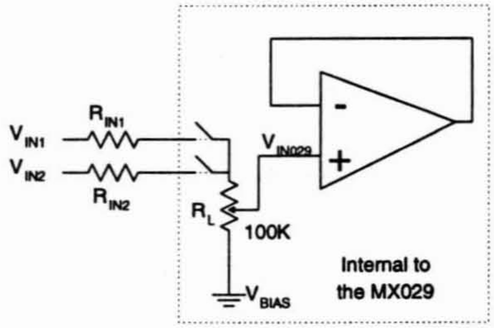

Figure 3: Attenuation Mode Configuration.

3. The MX029 as a digital to analog converter

The MX029 can be used as a digital to analog converter. The input should be DC coupled not AC coupled. If the part is AC coupled it will not function as a DAC.

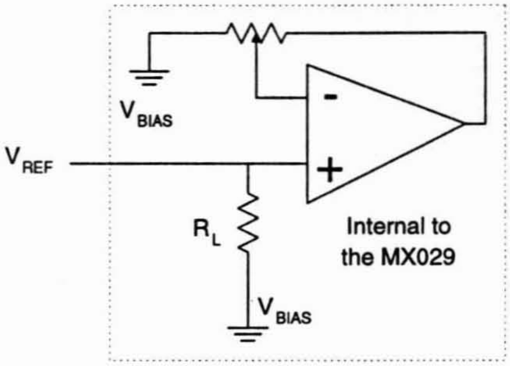

Figure 4: Using the MX029 as a DAC.

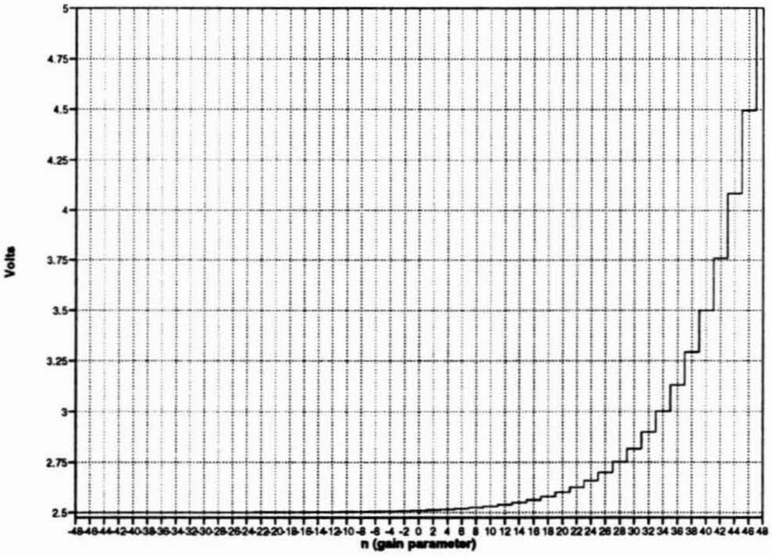

Figure 5: Volts vs. Gain Setting with V_{REF} at 2.51V.

When using the MX029 as a DAC there will be one input voltage(V_{REF}). To generate the output signal this input voltage is stepped up or down using the gain settings of the MX029. Each gain setting corresponds to a step on the output signal, see Figure 5. The minimum duration of each step(sample time) is approximately 8µs (giving a maximum sample rate of 125KHz). This is the time required to load and latch the 14 bits of serial data. This 125kHz sample rate can only be realized with negative gain settings. With gain settings 0dB to +30dB the amplifier's bandwidth will be the limiting factor and the maximum sample rate is approximately 20kHz. With gain settings above +30dB the maximum sample rate will be considerably less.

The analog GND of the MX029 is at $V_{DD}/2$ (V_{BIAS}). With a 5 volt power supply this voltage is 2.5 volts. With V_{BIAS} at $V_{DD}/2$ a sign bit is needed to get output levels above and below V_{BIAS}. see Figure 6. When in gain (attenuation) mode the difference of V_{BIAS} and the reference voltage(V_{REF}) will be amplified (attenuated).

$$V_{OUT} = (V_{REF} - V_{BIAS})10^{\frac{n}{20}} + V_{BIAS}$$

Where n is the gain setting -48 to +48. For n = 0, $V_{OUT} = V_{REF}$, for n < 0, V_{OUT} is between V_{REF} and V_{BIAS}, and for n > 1, V_{OUT} is between V_{REF} and a supply rail.

For example if V_{REF} is 2.4 volts and V_{BIAS} is 2.5 volts, with a gain setting of +24dB the output signal will $(2.4 - 2.5)10^{1.2} + 2.5V = 0.915$ volts.

To calculate the gain of each 2dB step use the following formula:

$$Gain = 10^{\frac{n}{20}}$$

Where n is the gain setting -48 to +48.

Figure 7 is an example of an output signal generated by changing the gain settings where the full dynamic range of the MX029 is used. To generate the output signal above V_{BIAS}, V_{REF} needs to be approximately 10 millivolts above V_{BIAS}. And to generate the output signal below V_{BIAS}, V_{REF} needs to be approximately 10 millivolts below V_{BIAS}. When using input levels 10 millivolts above or below V_{BIAS}, the input referred offset voltage of the amplifier must be compensated for by adjusting V_{REF} accordingly. An input referred offset voltage of 10 millivolts is not uncommon for an MX029. For this reason it is not very practical to use values of V_{REF} that are so close to V_{BIAS}. In this application the higher and lower gain settings will typically not be used. It is important to recognize that above V_{BIAS} the range is approximately 2.5 volts to 4.7 volts and below V_{BIAS} it is approximately 0.3 volts to 2.5 volts. With a sign bit the range is approximately 4.4 volts.

$$n_{MAX} = 20\log\frac{2.2V}{|V_{REF} - V_{BIAS}|}$$

Where n_{MAX} is the maximum gain setting with a particular V_{REF}.

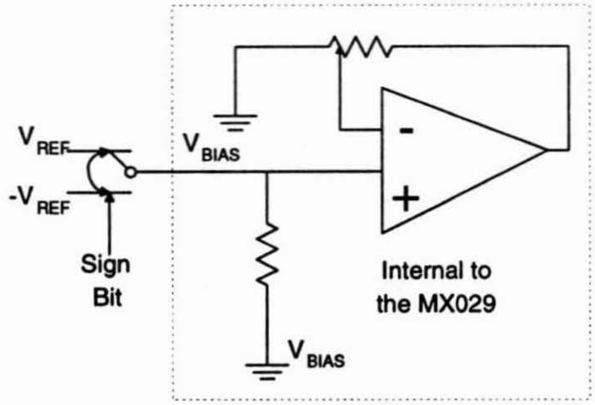

Figure 6: Using two V_{REF}s to generate an output that goes above and below V_{BIAS}.

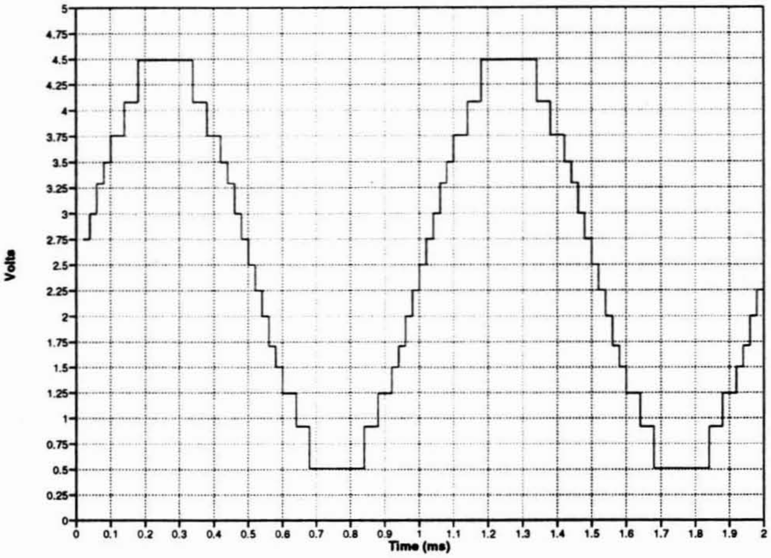

Figure 7: Example Output Signal.

Figure 7 is just one example of an output signal. There are many different output signals that can be generated. Before you start programming the MX029 take some time to think about what input signal level is necessary above or below V_{BIAS} to obtain the output signal that you desire.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Switched Capacitor Interfacing
Anti-Aliasing and Smoothing Filters

1. Introduction

Switched Capacitor Networks (SCNs) are sampled data systems and therefore are governed by the principles of discrete time signal processing. In this context, "discrete time" means the signal is sampled prior to processing. However, the amplitude is continuous – unlike Digital Signal Processing (DSP) systems where both amplitude and time are discrete.

VLSI technology (generally CMOS) has facilitated complete integration of SCNs on a single monolithic chip. Filters utilizing Switched Capacitor techniques (SCFs) are composed of switches, capacitors and opamps. Notice resistors are not mentioned. The resistors normally present in active filters are approximated by switched capacitors. By taking advantage of matching properties of CMOS capacitors, SCFs can be fabricated with low tolerance levels (less than 0.1%) and virtually any order.

The wireless and wireline telecom industries have made extensive use of SCFs. Even with the move towards digital technology and the ensuing popularity of DSP in the communications industry, SCNs are frequently employed where cost and power consumption are critical. SCNs generally have relatively high sampling rates (typically greater than 20 times the bandwidth of the interest). Due to their discrete time nature, aliasing and output smoothing must be addressed. Often a simple single pole filter (R-C network) suffices, but the location of these poles must be carefully thought out during the design process. The world is still analog.

The purpose of this paper is to address the need for anti-aliasing and smoothing filters for SCFs. First, the basics of sampling will be reviewed. The fundamentals of SCNs will follow this, and finally the design of anti-aliasing and smoothing filters for SCFs is addressed.

2. Sampling [3]

Before a continuous signal is processed by a discrete time filter it must first be sampled. Referring to Figure 1, sampling is the process of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is the sampling frequency. As the sampling rate increases (Figure 1) the sampled signal begins to approximate the original continuous signal.

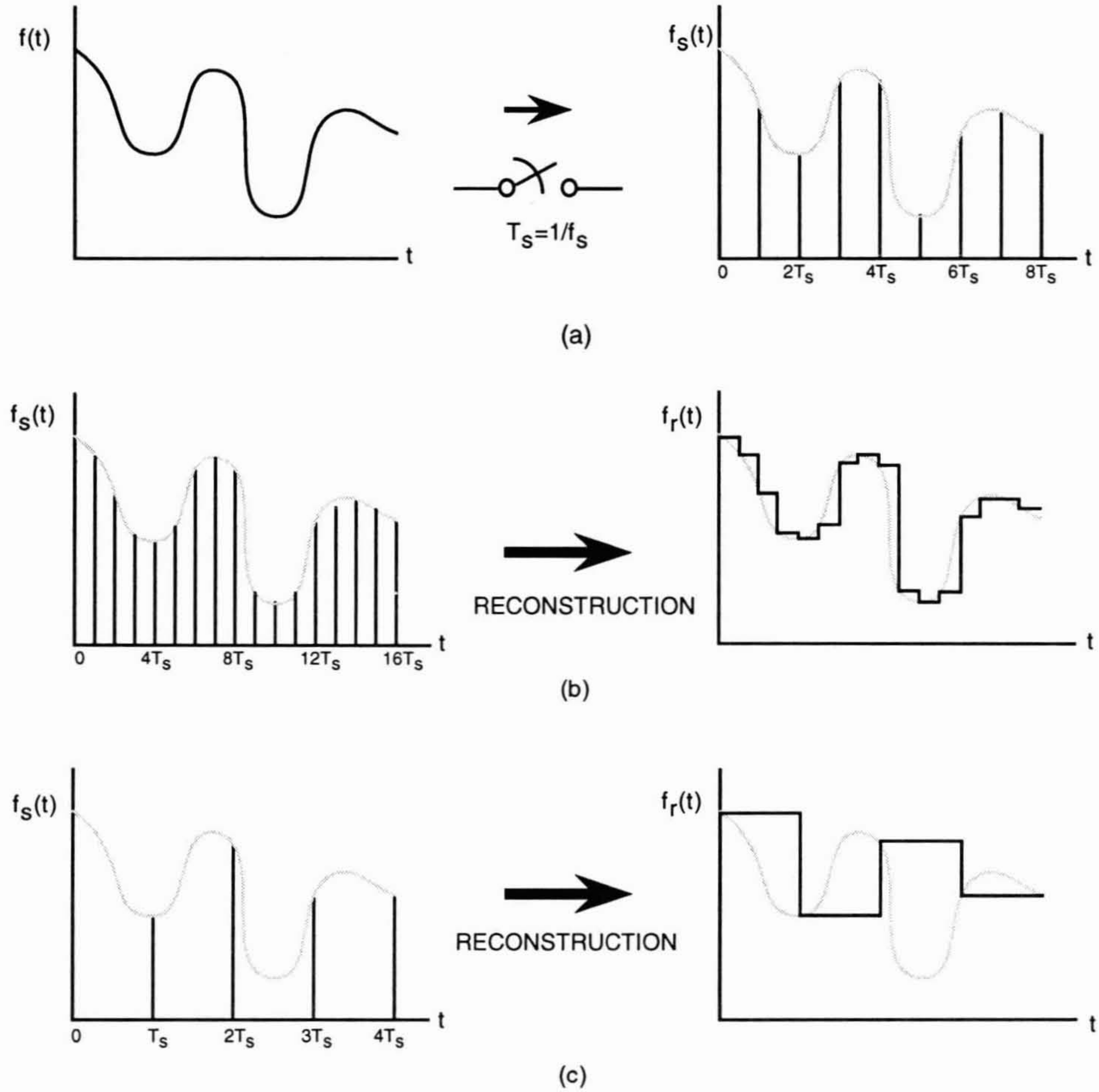

Figure 1: Waveform Sampling:
(a) sampling process, (b) reconstruction with acceptable sampling rate,
(c) reconstruction with unacceptable sampling rate

On the other hand, as the sampling frequency decreases (Figure 1) the samples move further apart in time, yielding a reconstructed signal that does not resemble the original. The limit on how far apart these samples can become without losing information is the basis for Shannon's sampling theorem.

Shannon's original work on sampling and information theory [3] stated the sampling theorem as:

> **"If a function f(t) contains no frequencies higher than *f* cycles per second it is completely determined by giving its ordinates at a series of points spaced (1/2*f*) seconds apart."**

A formal derivation is obtained by convolving the Fourier transform of the continuous signal with the Fourier transform of an infinite sequence of impulse functions.

$$F_S(\omega) = \frac{1}{2\pi}\left[F(\omega) * S(\omega)\right]$$

$$FS(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(x)S(\omega - x)dx$$

Where:

$F_s(\omega)$ = sampled signal spectrum
$F(\omega)$ = original signal spectrum
$S(\omega)$ = spectrum for a sequence of impulses
ω = radian frequency ($2\pi f$)

The result of the convolution is the original signal spectrum repeated at multiples of the sampling frequency as shown in Figure 2. Notice that if the sampling frequency is less than twice the bandwidth of the original signal then the replica centered at the sampling frequency will overlap and distort the original. This undesirable phenomenon is aliasing. Aliasing will be avoided if,

$$f_S \geq 2B$$

Where:

f_S = sampling frequency , Hz
B = bandwidth of original signal, Hz

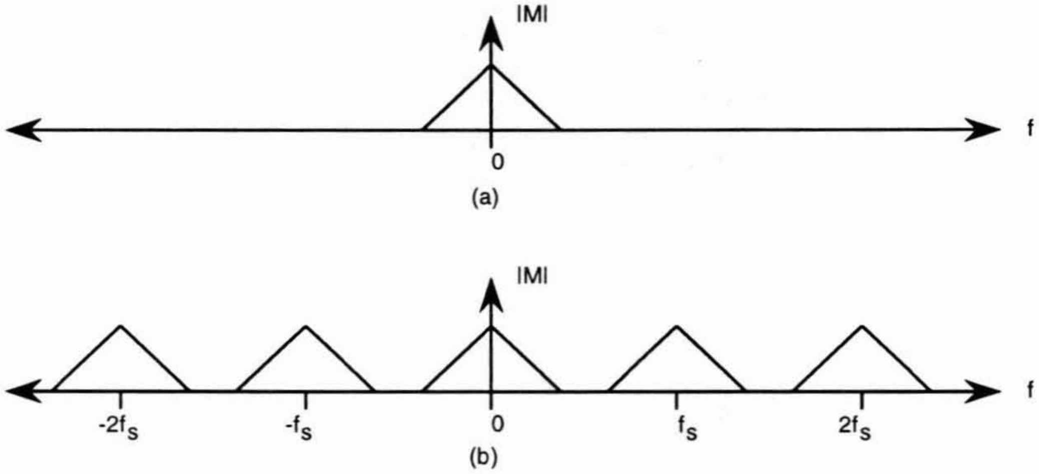

Figure 2: Frequency Spectrum of (a) continuous time signal, (b) sampled signal

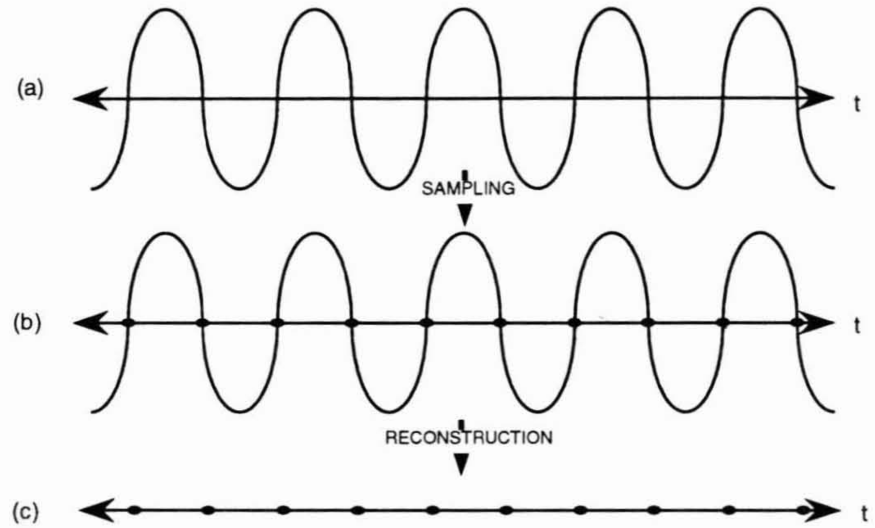

Figure 3: Time domain representation of sampling at f_S = 2B, (a) continuous signal, (b) sampled signal, (c) reconstructed signal

Shannon's sampling theorem is mathematically sound although, in most cases, it is not practical to sample a signal at exactly twice its highest frequency component. Figure 3 shows a sinewave sampled at **2B** samples per second, where **B = 1/T** and **T** is the period of the sinewave. Notice the difference between the reconstructed wave shapes and the original unsampled signal. This type of error is not the result of aliasing, yet it could cause deceptive results. A mathematician might claim that there is no information in a continuous sinewave that never changes amplitude or frequency. This is a fact. However, if a signal is sampled at exactly **2B**, some of the original signal may be lost or distorted.

If the system designer is not concerned with the possibility of losing some of the original signal, and wanted to sample at **2B**, he or she would still be facing the problem of bandlimiting. Bandlimiting is necessary to avoid aliasing. Figure 4 shows the spectrum of a sampled signal. Notice that for f_S = **2B** the bandlimiting filter must have infinite attenuation at the frequency **B**. A filter that matches this requirement is physically unrealizable.

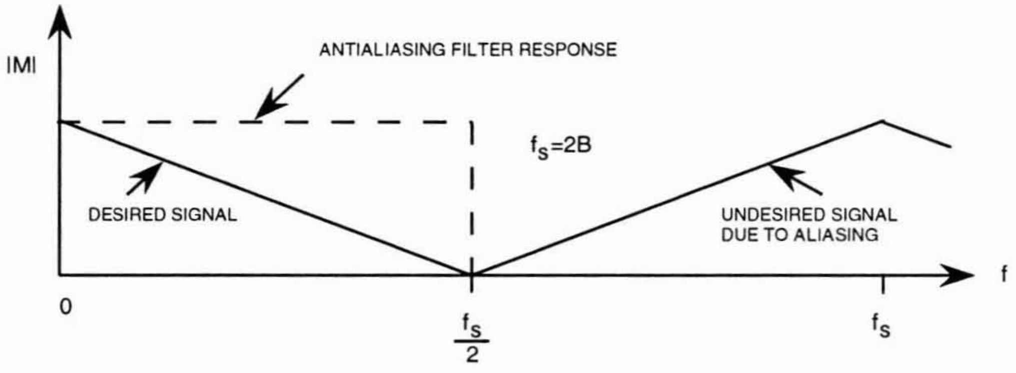
IMI
ANTIALIASING FILTER RESPONSE
f_S=2B
DESIRED SIGNAL
UNDESIRED SIGNAL DUE TO ALIASING
f
0
$\frac{f_S}{2}$
f_S

Figure 4: Anti-aliasing filter required for sampling at exactly 2B

3. SCN Concepts [1]

A single pole active filter (inverting integrator) is shown in Figure 5. This circuit is the primary building block for most active filters.

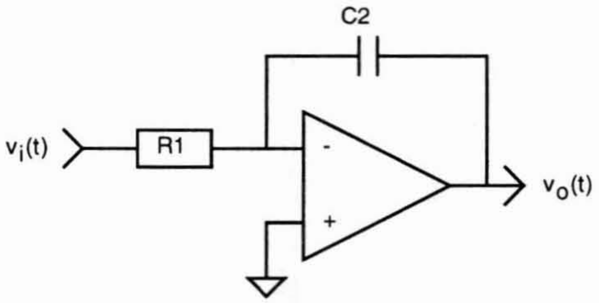

Figure 5: Active R-C Integrator

The output is defined by

$$v_O(t) = -\frac{1}{RC}\int_0^t v_I(\tau)d\tau$$

Hence, the output is an integrated version of the input, scaled by **-1/RC**. The pole frequency is determined by the value of **R** and **C.**

$$fp = \frac{1}{2\pi RC}$$

For a pole frequency of 3000Hz, (5) implies RC=53.05μs. A possible implementation, selecting C2 = 10pF (relatively large capacitor for CMOS technology), requires R=5.305MΩ. A monolithic resistor of this value would consume excessive amounts of silicon and is subject to significant variation with process and temperature. Integrated capacitors are also subject to variation with process and temperature. In addition, capacitor variations are independent of resistor variations.

A more practical realization is shown in Figure 6.

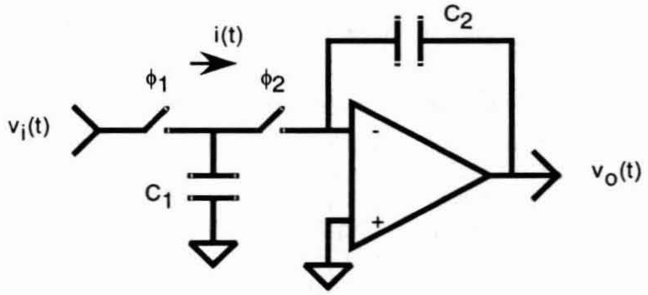

Figure 6: SC Integrator

Notice **R** is replaced by a capacitor and two switches. The function of the resistor is now approximated by transferring charge from $v_i(t)$ to the inverting input of the opamp at intervals determined by clocks $\phi 1$ and $\phi 2$. To ensure complete charge transfer $\phi 1$ and $\phi 2$ must not overlap as shown in Figure 7.

An approximate analysis of Figure 6 reveals the average current through the switches is

$$i = \frac{\Delta q}{T} = \frac{C_1}{T}(v_i - v_1)$$

or

$$i = \frac{1}{R}(v_i - v_1)$$

Where:

$$R = \frac{T}{C_1}$$

Looking back at the previous example for a pole frequency of 3000Hz, using T=10µs (f_{clk}=100kHz), yields C_1=1.885 pF. Hence, the integrator can be realized with two capacitors that track with process and temperature. No longer is the absolute value of the capacitors important, only their ratio.

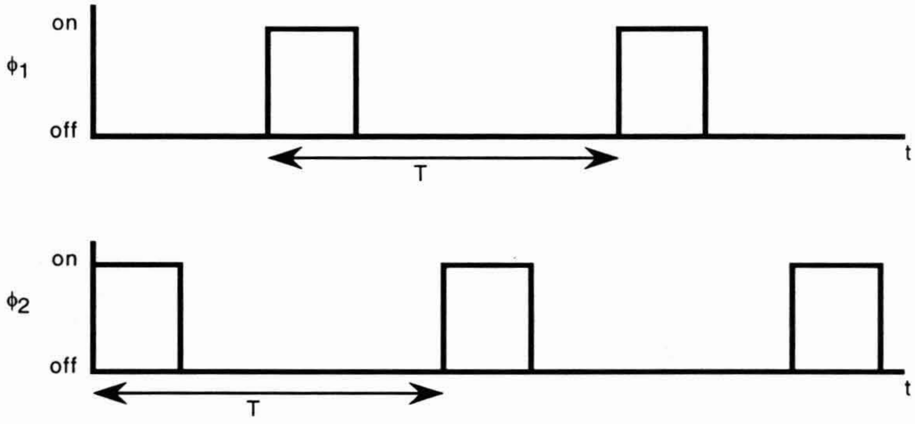

Figure 7: Non-overlapping clocks for SC Integrator

4. Anti-aliasing and Smoothing Filters for SCNs [2]

SCFs approximate active-RC filters by replacing resistors with switched capacitors. As the clock frequency (sampling rate) tends towards infinity the SCF becomes equivalent to the continuous time filter. In other words, higher clock frequency yields a better approximation of the desired response. Also, higher clock frequency lessens the requirements of the anti-aliasing filter (AAF) and smoothing filter (SMF). However, there are upper limits on clock frequency. Although SCFs have been implemented with clock frequencies greater than 1MHz, typical telecom filters (BW less than 10kHz) are clocked at or below 250kHz.

One factor which opposes higher clock frequencies is large capacitor ratios. Referring to the example in section 3.0,

using 1MHz in place of 100kHz, C_1 becomes 0.1885 pf. The ratio between C_1 and C_2 is now 53.05 where it was 5.305. Large capacitor ratios consume more silicon area and are more sensitive to process and temperature variations. Hence, the final sampling rate is a compromise between SCF implementation complexity and SMF/AAF requirements.

SMFs and AAFs can be integrated, but they are subject to the same problems associated with the continuous time RC integrator discussed in section 3.0 and are generally implemented externally. In some cases, where input and output signals are band limited externally, additional circuitry for AAFs and SMFs is not required. A block diagram of a typical SCF system, including AAF and SMF is shown in Figure 8.

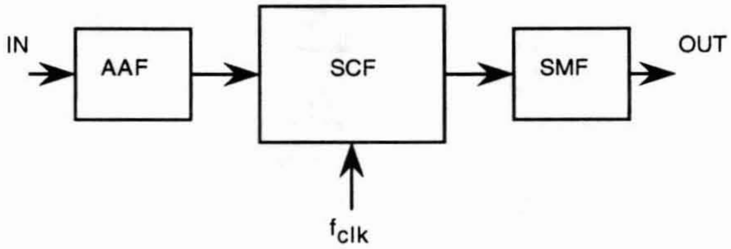

Figure 8: SCF system with AFF and SMF

To determine AAF and SMF requirements the system designer must know the sampling frequency (f_{clk}) and the bandwidth (BW) or cutoff frequency (f_{co}) of the SCF. For discussion purposes, assume f_{clk} =100kHz and f_{co} =5kHz. Recall from section 2.0, if any signal energy is present at the input, with frequency f_S greater than $1/2 f_{clk}$, it will be aliased to $f_{clk} - f_s$. Hence, an input with f_s =99kHz will be aliased to 1kHz. This aliased signal will appear as noise in the passband of the SCF. To eliminate or reduce the effect of this noise the AAF must band limit the input signal to $f_{clk} - f_{co}$ (see Figure 9).

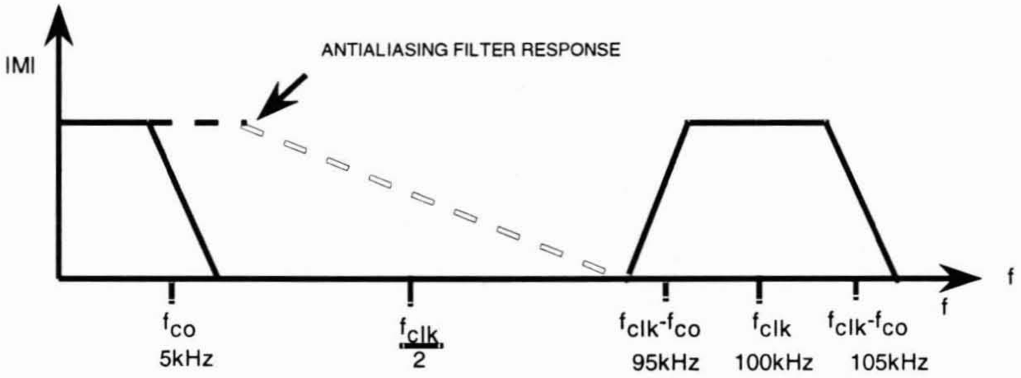

Figure 9: AAF requirements for SCF system

To obtain 20 dB suppression of aliased noise the minimum requirement for the AAF is a first order section (single pole) with it's cutoff frequency set to 9.5kHz (20 dB/decade/pole). Placing the pole at 9.5kHz minimizes the effect on the SCF passband response. To obtain further suppression more poles are necessary.

The single pole AAF can be implemented with a simple RC at the input to the SCF. The values for can be arrived at by using

$$RC = \frac{1}{2\pi f p}$$

Where:

fp = pole frequency

For the AAF response depicted in Figure 9, RC = 16.75ms. Setting C = 0.1µf yields R = 168Ω. The simple RC network should be used with caution–capacitive loading can cause stability problems. Also, the value of the resistor should be insignificant compared to the SCF input impedance.

A superior solution makes use of an additional opamp forming a damped integrator (see Figure 10). Often this opamp will be available on the SCF chip.

The complete network, including R1, C1, R2 and C2, forms a bandpass filter with a frequency response characteristic as shown in Figure 11.

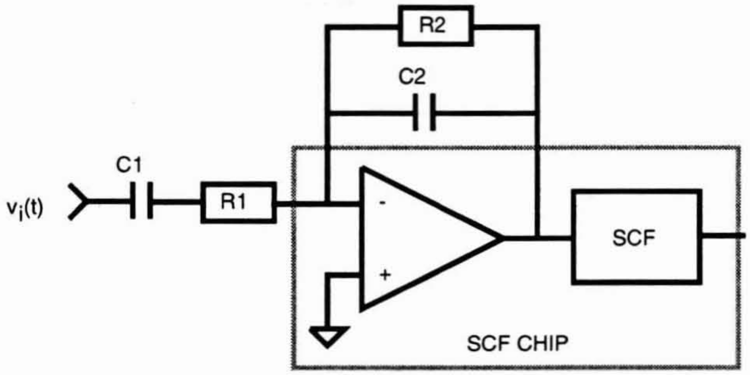

Figure 10: Active RC AAF

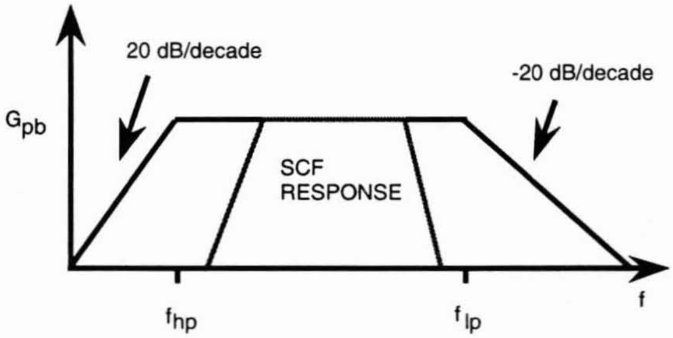

Figure 11: AAF frequency response

The highpass cutoff (f_{hp}) and lowpass cutoff (f_{lp}) are determined by

$$f_{hp} = \frac{1}{2\pi R_1 C_1}$$

and

$$f_{lp} = \frac{1}{2\pi R_2 C_2}$$

The passband gain is set by

$$G_{pb} = \frac{R2}{C2}$$

C_1 is not required if the input signal is biased properly (SCF internal bias = external bias).

To meet the AAF requirements shown in Figure 9 (assuming unity passband gain, f_{lp} = 9.5kHz and f_{hp} = 100 Hz) $\mathbf{R_1} = \mathbf{R_2}$ = 100KΩ, $\mathbf{C_2}$ = 168pf and $\mathbf{C_1}$ = 0.0159µf.

SMF requirements are similar to those of the AAF. The SCF output is a sampled signal and therefore contains replicas of the SCF response at multiples of the sampling frequency. If left unfiltered these replicas appear as high frequency (clock) noise. In some cases this is tolerable. However, in systems where minimum noise is critical the SMF is required.

5. Conclusion

Switched capacitor filters are sampled data systems and hence require anti-aliasing filters at their inputs and smoothing filters at their outputs. The simplest form (and often sufficient) of these filters is the single pole RC network. Other forms such as active RC networks and higher order filters can yield distinct benefits. In any case, application of switched capacitor filters must be viewed at the system level in order to realize optimum performance.

6. REFERENCES

[1] R. Gregorian, K. W. Martin, and G. C. Temes, "Switched-Capacitor Circuit Design," Proceedings of the IEEE, pp. 941-966, August 1983.

[2] L. P. Huelsman and P. E. Allen, Introduction to the Theory and Design of Active Filters, McGraw-Hill, New York, 1980.

[3] A. B. Jerri, "The Shannon Sampling Theorem - Its Various Extensions and Applications: A Tutorial Review," Proceedings of the IEEE, pp. 1565-1596, November 1977.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Crystal Oscillator Circuit Design

In this application note we shall discuss our recommended crystal oscillator circuit, explain each component in the circuit and provide some guidelines on selecting values for these components. Finally, we shall give a few precautions to take in order to avoid in-stability and start-up problems.

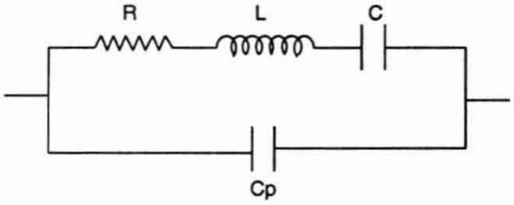

Figure 1. Crystal equivalent Circuit.

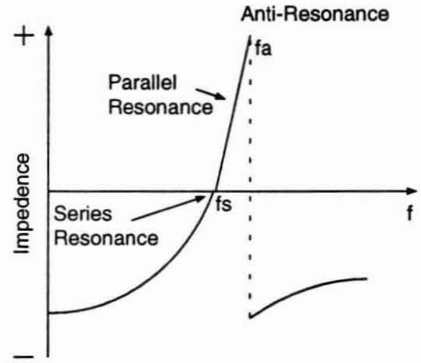

Figure 2. Reactance Vs Frequency plot of a crystal.

Figure 1. shows the crystal equivalent circuit. R is the effective series resistance, L and C are the motional inductance and capacitance of the crystal. C_P is the shunt capacitance due to the crystal electrodes. Figure 2. shows the reactance-frequency plot of the crystal. When a crystal is operating at series resonance it looks purely resistive and the reactances of the inductor and the capacitor are equal (XL = XC). The series resonance frequency is given by the equation

$$fs = \frac{1}{2\pi\sqrt{LC}}$$

When the crystal is operating in parallel resonant mode it looks inductive. The frequency of operation in this mode is defined by the load on the crystal. The crystal manufacturer should specify the load capacitance C_L for parallel resonant crystals. In this mode the frequency of oscillation is given by the equation.

$$f_a = \frac{1}{2\pi\sqrt{L\frac{C_L C_P}{C_L + C_P}}}$$

In parallel resonance mode the crystal can be made to oscillate anywhere on the f_s - f_a slope of the reactance plot, shown in Figure 2, by varying the load of the crystal. All of MX-COM's crystal oscillator circuits recommend using parallel resonant mode crystals.

Figure 3. shows the recommended Crystal oscillator circuit diagram. In this type of setup the crystal is expected to oscillate in parallel resonant mode. The inverter which is internal to the chip acts as class AB amplifier and provides approximately 180° phase shift from input to the output and the π network formed by the crystal, R_1, C_1 and C_2 provides additional 180° phase shift. So the total phase shift around the loop is 360°. This satisfies one of the conditions required to sustain oscillation. The other condition, for proper startup and sustaining oscillation is the closed loop gain should be ≥1.

The resistor R_f around the inverter provides negative feedback and sets the bias point of the inverter near mid-supply operating the inverter in the high gain linear region. The value of this resistor is high, usually in the range of a 500KΩ ~ 2MΩ. Some of MXCOM's ICs have this resistor internal, refer to the external component specifications in the data sheet of a particular chip.

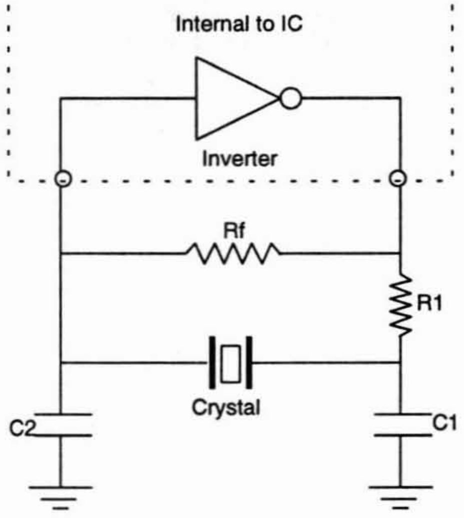

Figure 3. Crystal oscillator circuit.

The capacitors C_1 and C_2 form the load capacitance for the crystal. The optimum load capacitance (C_L) for a given crystal is specified by the crystal manufacturer. The equation to calculate the values of C1 and C2 is

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_S$$

Where C_S is the stray capacitance on the printed circuit board, typically a value of 5pf can be used for calculation purposes. Now C_1 and C_2 can be selected to satisfy the above equation. Usually C_1 and C_2 are selected such that they are approximately equal. Large values of C_1 and/or C_2 increases frequency stability but decreases loop gain and may cause start-up problems.

R_1 is the drive limiting resistor, the primary function of this resistor is to limit the output of the inverter so that the crystal is not over driven. R_1 and C_1 form a voltage dividing circuit, the values of these components are chosen in such a way that the output of the inverter goes close to rail-to-rail and the input to the crystal is 60% of rail-to-rail, usual practice is to make resistance of R_1 and reactance of C_1 equal at the operating frequency, i.e. $R_1 \approx XC_1$. This makes the input to the crystal half that of the inverter output. Always make sure that the power dissipated by the crystal is with-in the crystal manufacturer's specifications. Over-driving the crystal may damage the crystal. Please refer to the crystal manufacturer's recommendations.

Ideally the inverter provides 180° phase shift, but the inherent delay of the inverter provides additional phase shift proportional to the delay. In order to ensure the total phase shift of *n*360° around the loop, the π network should provide 180° less the phase shift due to the inverter delay. R1 can be varied to accomplish this. With fixed C_1 and C_2, the closed loop gain and phase can be altered by varying R_1. In some applications R_1 can be ignored if the above two conditions are met.

Some ICs have all the external components (R_f, R_1, C_1, and C_2) internal to the chip, thus eliminating worries to the circuit designer. In this case simply connect the crystal across the XTAL and XTAL pins.

Hints:

Select a crystal with low effective series resistance (ESR), which helps with crystal start-up problems. Lower ESR increases the loop gain.

Reduce the stray capacitance on the board laycut by shortening the traces. This would help with startup problem and as well as the frequency of oscillation.

Always test the circuit in applicable temperature and voltage ranges to ensure the crystal starts and sustains oscillations and tweak the component values if necessary.

For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of Vdd, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain further crystal oscillator design assistance, consult your crystal manufacturer.

The recommended way to optimize R_1 is first calculate C_1 and C_2 as explained earlier and connect a potentiometer in place of R_1, set its initial setting at approximately equal to XC_1, then vary the potentiometer setting if required until the crystal starts under all conditions and sustains oscillation under steady state condition.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Variable Split-Band Scrambling (VSB)

Variable Split-Band Scrambling (VSB) Furnishes Voice Security

Introduction

Voice scrambling offers tactical security for radio dispatch communications. It takes so long, even for a dedicated eavesdropper, to unscramble your transmissions that the information would be worthless by then.

Unwanted consequences of third-party radio communications eavesdropping include foiled drug busts, unsolved burglaries and pirated business opportunities. Some mobile radio users employ voice privacy and voice security devices to scramble their communications. Most users who need voice security continue to communicate in the clear, however, for several reasons:

(1) Cost --They cannot justify the capital expense.

(2) Technology -- The poor quality of recovered audio and the radio range reduction common to many voice security systems discourage their use.

(3) Availability -- Two principal scrambling alternatives, frequency inversion and digital encryption, are not suitable for many applications. Frequency inversion offers privacy but not security; digital encryption offers high security but with a high price tag.

Semiconductor technology advances have reduced costs and improved the quality of voice security products. Variable Split-Band (VSB) scrambling has become economical because of such advances.

How it works

Filters separate the voice band (400Hz to 2700Hz) into a pair of subbands (32 pairs are possible). (See Figures 1A, 1B and 1C.) A mixer fed with a carrier signal inverts the subbands; a summing amplifier recombines them. Ordinary radio transceivers transmit the resulting variable split-band-scrambled output via an ordinary radio communications channel.

Microprocessor outputs control the split point (the frequency at which the voice band is subdivided) and change it from 4 to 60 times per second. Figure 2 reveals the "rolling code" nature of VSB scrambling. One of more than 65,000 unique user-programmable code keys initializes the pseudorandom sequence of split points. User programming commands the split point's rate of change, or "hop rate," to vary pseudorandomly or in a fixed fashion.

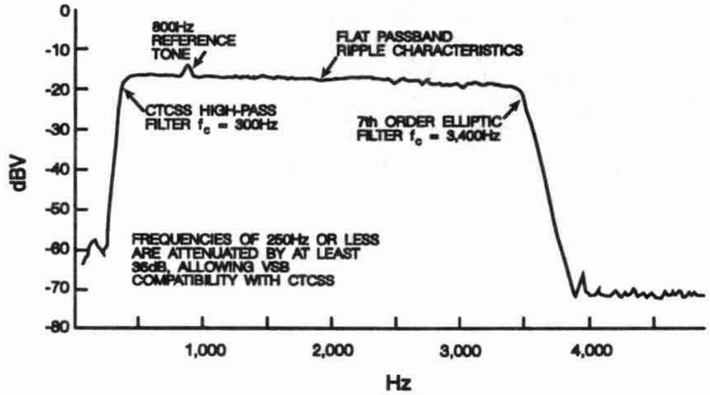

Figure 1A: Audio output of VSB filter array IC in clear mode

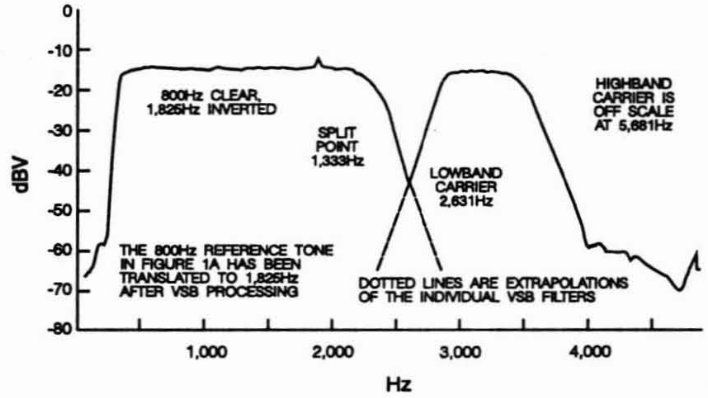

Figure 1B: Audio output of VSB filter arrray IC in "scramble" mode with split point at 2,333Hz

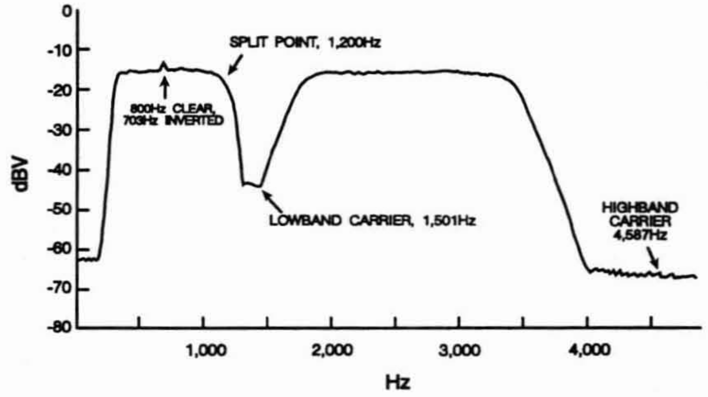

Figure 1C: Audio output of VSB filter array IC in “scramble” mode with split point at 1,200Hz

Filtering Accuracy

Optimum recovered audio quality depends upon highly accurate voice filtering. Two pairs of 7th order, switched-capacitor, elliptic filters in the VSB filter array integrated circuit (IC, on-chip) accomplish all the filtering (See Figure 3).

The transceiver's mic. audio pre-amplifier or receiver audio demodulator output feeds the VSB filter array IC's highband and lowband inputs. Within the IC, audio from each subband passes through a lowpass filter, a frequency inverter and another lowpass filter. A summing amplifier recombines the subbands. The chip includes a highpass filter that permits VSB scrambling to be used with continuous-tone controlled squelch systems (CTCSS) and other sub-audible signaling schemes.

On-chip programmable dividers with a 5-bit logic address control the 32 split points and their highband and lowband carrier frequencies. The VSB microprocessor uses the 5-bit address to generate a rapidly changing sequence of split points. Table 1 shows the exact relationship between each split point and its associated carrier frequencies.

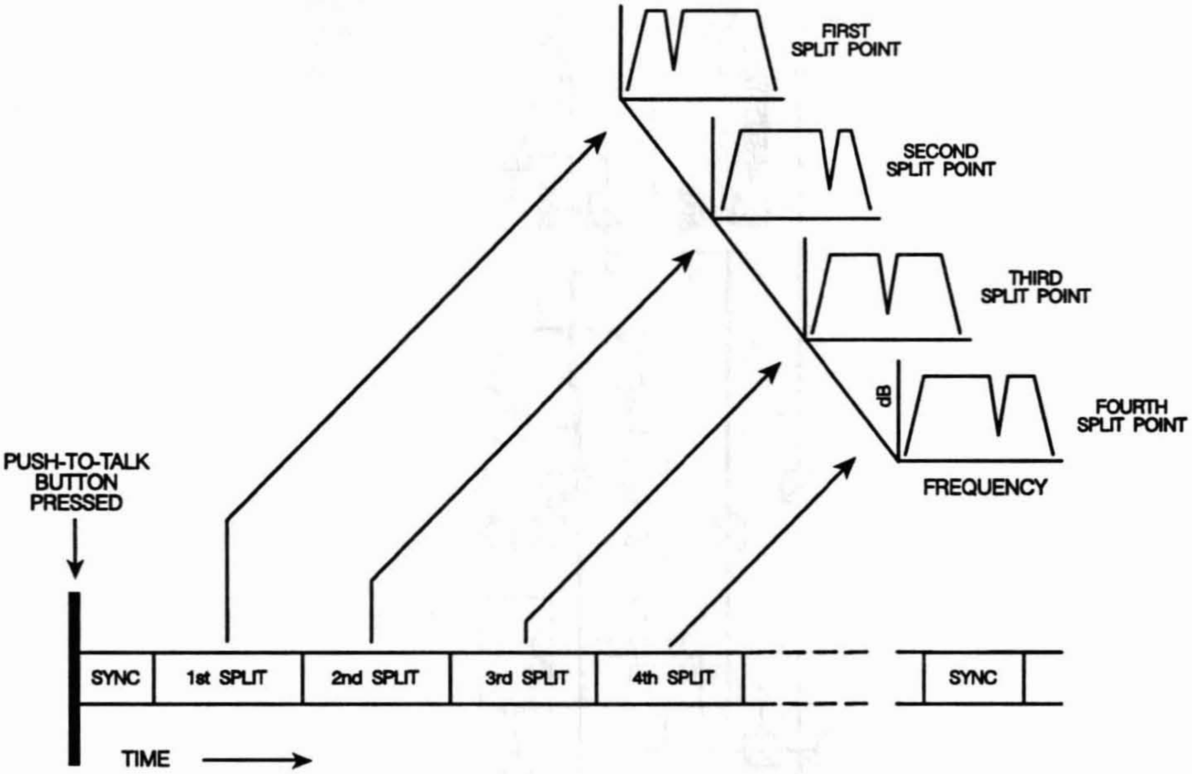
FIRST
SPLIT POINT
SECOND
SPLIT POINT
THIRD
SPLIT POINT
dB
FOURTH
SPLIT POINT
FREQUENCY
PUSH-TO-TALK
BUTTON
PRESSED
SYNC
1st SPLIT
2nd SPLIT
3rd SPLIT
4th SPLIT
SYNC
TIME

Figure 2: The effect of rolling code split points on the transmitted radio spectrum

Microprocessor Control

The VSB microprocessor performs scramble system control functions, including:

- generation of split-point sequences
- control of system synchronization
- monitoring of the push-to-talk (PTT) line
- code key selection
- code key loading
- selection of the secure or clear mode.

The microprocessor generates pseudorandom strings of split points initialized by one of four user-programmable code keys. Non-volatile, electrically erasable, programmable read-only memory (EEPROM) stores the code keys and other user-programmable system information (see Figure 4).

To decode a rolling, VSB-scrambled message properly, the receiver(s) must "hop" in unison with the transmitter from one split point to the next. A continuous synchronization scheme accomplishes this task. The scheme transmits 1200-baud minimum-shift keyed (MSK) data bursts every three seconds. Authorized parties can descramble transmissions even if the beginning of the message is missed, preserving mobile radio's inherent "late joining" feature.

In the absence of valid synchronization bursts, receivers revert to clear mode. The automatic reversion to clear mode ("clear voice override") makes scrambling easier to use in systems that include some radios not equipped for scrambling.

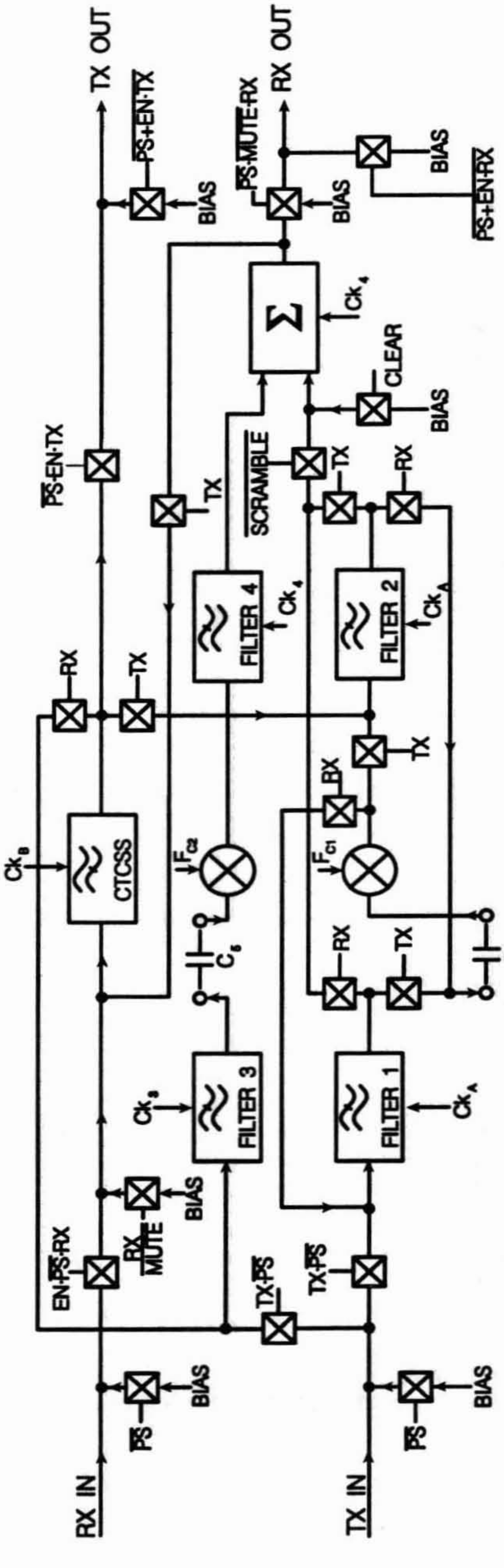
TX OUT
RX OUT
RX IN
TX IN
PS+EN·TX
PS·MUTE·RX
PS+EN·RX
PS·EN·TX
EN·PS·RX
TX·PS
BIAS
CLEAR
SCRAMBLE
RX
TX
MUTE
CTCSS
FILTER 1
FILTER 2
FILTER 3
FILTER 4
Σ
Ck4
CkA
CkB
Ck3
FC1
FC2
C6

Figure 3 - Functional block diagram of the VSB filter array

Figure 3: Functional block diagram of the VSB filter array

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{C1}	High Band Carrier, Hz f_{C2}
00000	2800	3105	6172
00001	2625	2923	6024
00010	2470	2777	5813
00011	2333	2631	5681
00100	2210	2512	5555
00101	2100	2403	5494
00110	2000	2304	5376
00111	1909	2212	5263
01000	1826	2127	5208
01001	1750	2049	5102
01010	1680	1984	5050
01011	1555	1858	4950
01100	1448	1748	4807
01101	1354	1655	4716
01110	1272	1572	4629
01111	1200	1501	4587
10000	1135	1436	4504
10001	1050	1351	4424
10010	976	1278	4347
10011	913	1213	4310
10100	857	1157	4273
10101	792	1094	4166
10110	736	1037	4132
10111	688	988	4065
11000	636	936	4032
11001	591	891	3968
11010	552	853	3937
11011	512	813	3906
11100	471	772	3846
11101	428	728	3816
11110	388	688	3787
11111	350	650	3731

Table 1: ROM Address Programming

Only transmitting VSB units generate synchronizing data bursts, so the system resynchronizes at the transmitting station's command. Transceivers automatically transmit 80ms data bursts every three seconds after beginning a transmission. Each data burst includes:

Unit System Address -- Identifies the scrambler as part of a designated group.

Code Key File Number -- Identifies which of the four stored code keys to use.

Time Of Day -- When mixed with the secret code key, which never is transmitted, time of day tells the receiver on which part of the 50-hour long split-point sequence to begin "hopping."

Synchronization Cue -- Tells the receiver when to change split points.

In the standby mode, VSB scrambling units scan continuously for incoming synchronization bursts that have the proper system address and file number. After receiving one such data burst, a VSB unit uses the time-of-day signal and synchronization cue to descramble the incoming message properly. Unless the receiving unit receives the proper address and file combination, it processes incoming transmissions as though they were unscrambled.

A robust error-detection algorithm, based on the British MPT 1317 signaling protocol, minimizes synchronization errors. As a safeguard, VSB scramblers retain synchronization even if a single synchronization burst is missed. If the scrambler misses two synchronization bursts in a row, the system reverts to the standby mode and scans once again for synchronization burst data.

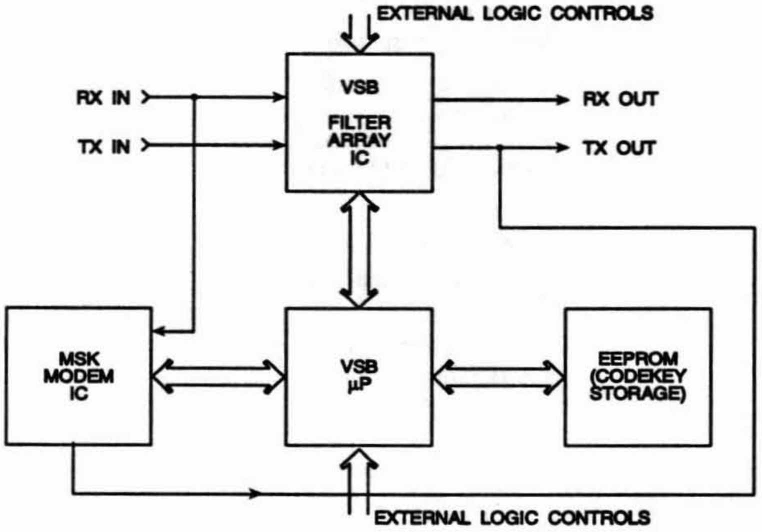

Figure 4: Block diagram of VSB Scrambler mode

Voice Security Market

Potential markets for economical voice security products include:

- *Tax*
- *Towtruck*
- *Marine and other dispatch operations whose managers have been unsatisfied with the price or performance of voice security products*
- *Municipal law enforcement agencies that lack voice security systems or that are committed to a digital encryption system that is too expensive to insall into every radio in the organization.*

Minimum-shift keyed modulation offers excellent narrowband transmission properties and superior noise performance. With MSK modulation, voice intelligibility and synchronization are lost more or less concurrently in fringe reception areas and without an appreciable loss in radio range.

An eavesdropper monitoring a VSB-scrambled transmission hears an unintelligible jumble, interrupted by bursts of digital "static" every three seconds. Consider VSB scrambling's security features:

(1) The split-point sequence permutation, which is based on a mixture of the secret code key and the time-of-day signal, changes automatically every three seconds. The code knowledge that may be obtained from one descrambled three-second sequence cannot be applied to descramble subsequent segments because they are based on different sets of pseudorandom permutations.

(2) The split-point "hop rate" may be varied pseudorandomly, further complicating the task.

(3) Each VSB-equipped radio can transmit and receive four programmed code keys, and VSB systems can accommodate as many as 16 unique code keys. Thus, a unit can transmit on one code key and receive on another.

(4) The code keys may be changed at any time. They never are transmitted. They cannot be deduced by visual or mechanical means.

VSB Scrambling Multiple Codekey Capability

Within a VSB network, up to 16 codekeys can be allocated. Four of the sixteen codekeys can be installed per radio. As illustrated below, this capability can create interesting subgroup segregation possibilities:

Scenario: Public safety departments of medium-sized cities need interagency, as well as private, intradepartmental secure communications.

Solution: A VSB Scrambling codekey allocation scheme allocates seven codekeys (A-G), four to the police force, and two each to the fire department, ambulance service, and detective unit.

User Subgroup	Installed CODEKEYS	Communications Capability
1) HQ/Supv.	All	Monitor all channels
2) Police	A	Intradepartment Only
	B	Police and Fire
	C	Police and detectives
	D	Police and ambulance
3) Fire	B	Police and fire
	E	Intradepartment Only
4) Detectives	C	Police and detectives
	F	Detectives Only
5) Ambulance	D	Police and ambulance
	G	Intrasquad, ambulance and hospital

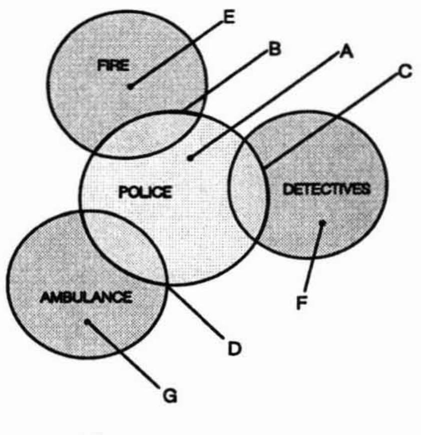

Figure 5: Multiple codekeys extend subgroup segregation possibilities in a medium-sized city's public safety

Given these security features, how difficult is it to descramble such a garbled transmission? According to two experts, it is not easy.

According to Michael Washvill, a voice and data security specialist with a federal agency, "VSB scrambling can be broken, but not in real time. The only practical attack is through trial and error. The scrambled speech must first be recorded, then divided into finite time segments according to the hop rate. Each segment is processed through a variety of split point combinations until clear speech results."

A TRW systems engineer and former U.S. Department of Defense employee, Jim Walker, concurs: "The 'brute force' method of trial and error is the only way to break VSB-scrambled speech. Assuming that the 'bad guys' have a stolen VSB unit and no prior knowledge of the code key or code keys, 50 to 100 minutes of dedicated effort are required to descramble one minute of VSB-scrambled speech. A rule of thumb is 60:1 'grunt time to clear speech time'."

Walker continued, "For most eavesdroppers, the potential rewards do not justify the time and effort. Two additional factors come into play. First, by the time the information is decrypted, will it still be of any use? Second, what percentage of the descrambled radio traffic will be of value?"

Given the time and perseverance required to break a VSB-scrambled transmission, two alternatives become much more attractive to those who want to eavesdrop: Steal a VSB-equipped radio or bribe someone who knows the codekey. Strict code key management procedures reduce system vulnerability to these attack methods.

To reduce the possibility of bribery, restrict code key knowledge to one person. To guard against stolen VSB units, change system code keys on a regular basis by using the VSB keyloader.

The keyloader is a portable tool that reprograms VSB-equipped radios in the field. A technician connects the keyloader's data-loading cable to a VSB-equipped radio and presses the load button to install as many as four new codekeys into each radio. Only the person with codekey management authority can program the keyloader or read its contents.

Tactical vs. Strategic

Voice security requirements can be divided into two broad categories: tactical and strategic. Tactical applications are those in which the secrecy of the message is time-dependent, such as battlefield tactical communications, most municipal police communications and nearly all dispatch communications. The tactical message retains its value for one or two hours at most. VSB scrambling serves tactical security requirements.

James Bramford, in his book The Puzzle Palace, defines strategic communications as "the high-level diplomatic, commercial and military communications that might give away a nation's foreign policy venture, where and with whom it was doing business, or what new weapons were being developed over the next few years." Today's strategic applications demand some form of digital encryption.

In addition to the message security afforded by digital encryption or VSB scrambling, transmission security can be assured through spread-spectrum techniques, such as frequency hopping, which render the radio signal both undetectable and immune to jamming.

Most mobile radio users have tactical voice security requirements. For these applications, VSB scrambling offers a practical, economical alternative to digital encryption systems. VSB scrambling requires no modification of the installed communications network. It has little or no impact on radio range.

As dealers and users become more comfortable with VSB and other new scrambling technologies, foiled drug busts, unsolved burglaries and pirated business opportunities resulting from unauthorized eavesdropping will become things of the past.

Authors:

Steve Kelley and Hank Wallace

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EVALUATION KITS

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EV6021 .... 5 – 5
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EV8000 .... 5 – 7
EV9000 .... 5 – 8
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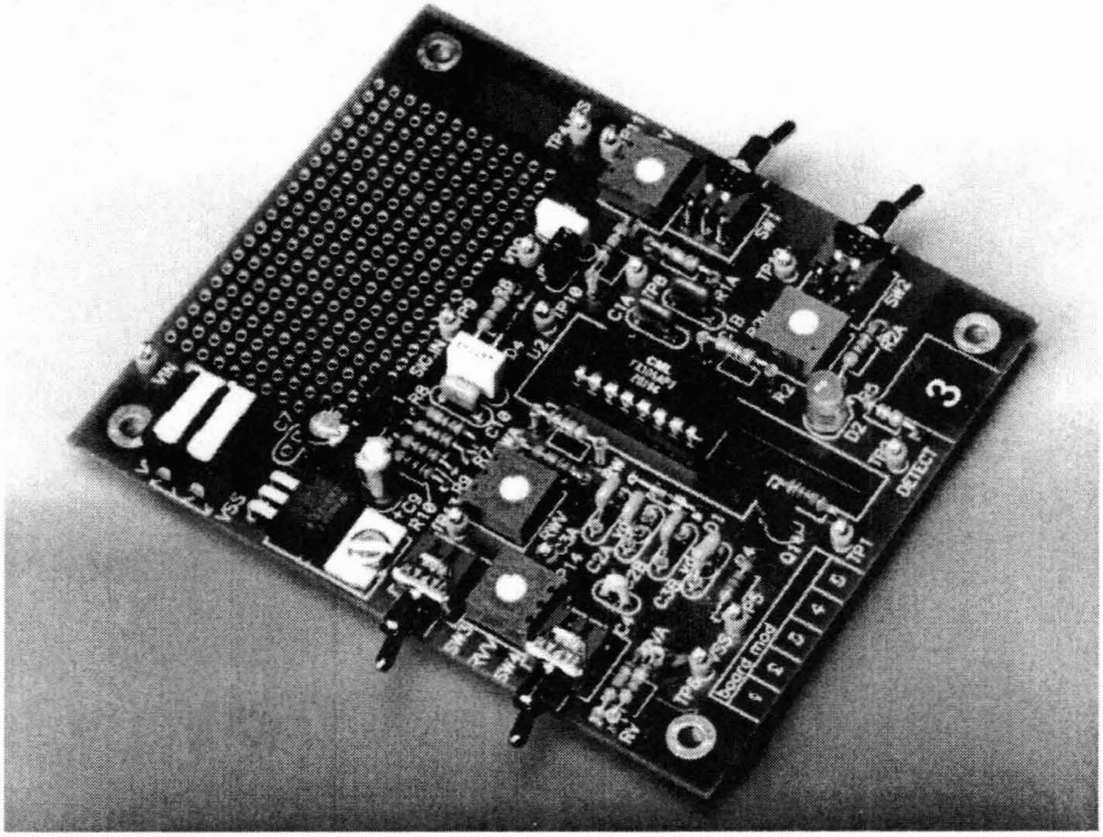
MX·COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

EV1050 Evaluation Kit for use with the MX105A

FEATURES

- For MX105A Product Evaluation
- Easily Adjustable Center Frequency, Bandwidth and Timing
- On-Board Regulator
- Easy Access to Test Points
- Simple Component Selection with Excel Spreadsheet Enclosed
- User's Prototyping Area



The EV1050 Evaluation Kit comprises a single board containing an MX105A. Switches select variable resistors for adjusting the detect frequency, bandwidth and response time. Many of the fixed components are socketed so that they can be changed by the user.

The EV1050 board is powered from a single 8 - 35V external DC power supply; an on-board regulator sets 3.0V or 5.0V operation. An LED indicates the status of the detect output.

The supply current of the MX105A may be measured by removing the appropriate jumper. Test points are provided for the signal input, the VCO output and the detect output. A user prototyping area is provided.

The EV1050 provides an excellent demonstration and prototyping platform for MX105A based projects.

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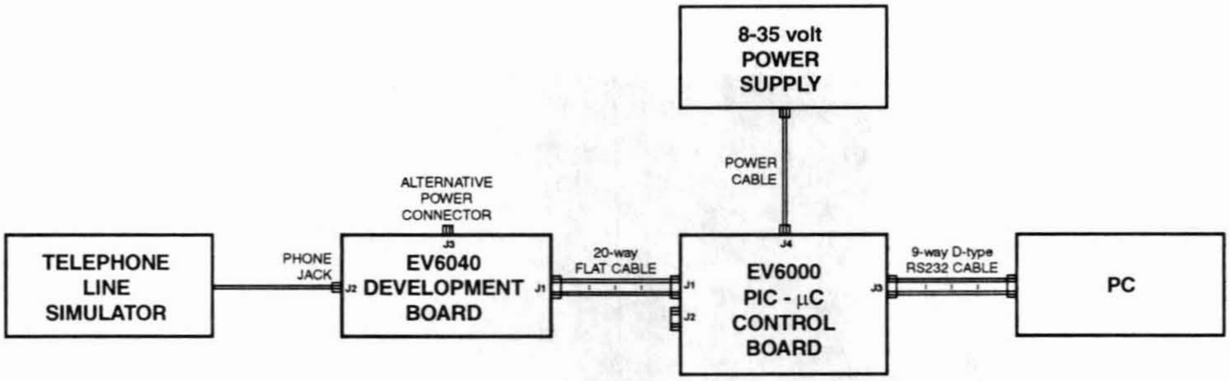
PRODUCT INFORMATION

EV6000 µController Board for use with the EV6040

- **For use with EV6040**
- **Executes Applications Software for the MX604 and MX614**
- **On-Board PIC Programming with Serial Interface and PC Software**
- **Serial (RS232) Interface to a PC**
- **Diagnostic Firmware/Software**
- **Socketed PIC 16-Series µC**
- **8.0V - 35.0V Single Power Supply Operation**
- **On-Board Supply Regulator**


8-35 volt
POWER
SUPPLY
POWER
CABLE
ALTERNATIVE
POWER
CONNECTOR
J3
TELEPHONE
LINE
SIMULATOR
PHONE
JACK
J2
EV6040
DEVELOPMENT
BOARD
J1
20-way
FLAT CABLE
J1
J2
J4
EV6000
PIC - µC
CONTROL
BOARD
J3
9-way D-type
RS232 CABLE
PC

The EV6000 Development Board was designed for use with the EV6040 Development Kit. The EV6040 is used to evaluate the MX604 and MX614.

The EV6000 Development Kit consists of one board containing a socket for a UV-erasable PIC µC which the user may program and control via the RS232 serial interface. With the aid of suitable applications software, the user can demonstrate the use of the MX604 or MX614 in various telecommunication applications.

The EV6000 may be powered from a single 8 - 35V DC power supply. There is an on-board regulator which sets the 3.3V or 5.0V requirement. The PIC µC may be driven from an external clock, or from its own crystal oscillator. Test points provide access to programming voltages. Additional space was designed in for the user to ZIF-socket the PIC µC, if desired. Interconnecting cables are provided for an RS232 link to a PC and for 20-conductor flat cable connections to other MX-COM Development Kits or other parts in a user's system.

This EV6000 Development Kit is designed to be a general-purpose product, which may be used to support other MX-COM Development Kits in the future. Applications software is regularly updated and users should contact MX-COM for further details.

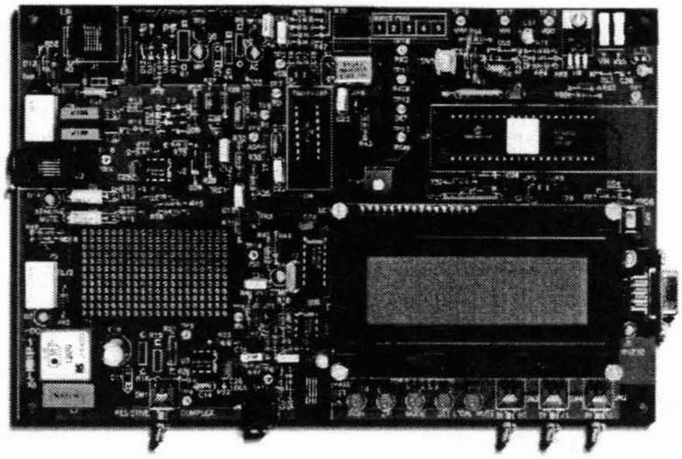
MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

EV6021 Development Kit for the CMX602A

Features

- For CMX602A Product Evaluation
- Adjunct Box or Feature Phone Configuration
- Single Power Supply Operation
- LCD or RS232 Link to PC with Software
- On-Board Regulator
- Socketed Components for Adjustment
- User's Prototyping Area
- Socketed Space for Optional and Telco-Specific Components
- Socketed PIC 16-Series µC
- On-Board PIC Programming with Serial Interface and PC Software
- 2- to 4-Wire Interface with Handset Socket



The EV6021 Evaluation Kit comprises a single board containing a CMX602A, line interface components, PIC µController and the option of using either the on-board 4-line LCD module or interfacing to a PC via a serial communications port. For the latter mode of operation Windows software is supplied. When using the LCD module three switches are used to select the EV6021 mode of operation.

The board is powered from a single 8 - 35V DC power supply; an on-board regulator sets V_{DD}. LEDs indicate control, interrupt and detect line status (ZP, MODE, $\overline{IRQ}$ and DET) and the CMX602A may be driven from an external clock, or from its own crystal oscillator. Important signals can be monitored by test points. The CMX602A is socketed for easy replacement; there is room for the user to fit a ZIF socket. A user prototyping area is provided.

On-board circuitry may be used to implement a wetting pulse and to place an AC or DC load on the line. A hook relay connects the 2- to 4-wire interface/op-amp hybrid for voice communications to the line. An external phone socket for adjunct box demonstration is provided, the connection to which can be disabled with a relay. A mutable local voice input and DTMF generator (for CIDCW acknowledgement tone) are provided. Operation is indicated by LEDs. The CMX602A supply current may be measured by removing a jumper. Where components are telco-specific (line impedance, line protection, AC-load, wetting pulse, etc.) space is provided for the user to add appropriate components.

The EV6021 provides an excellent demonstration and prototyping platform for CMX602A based projects.

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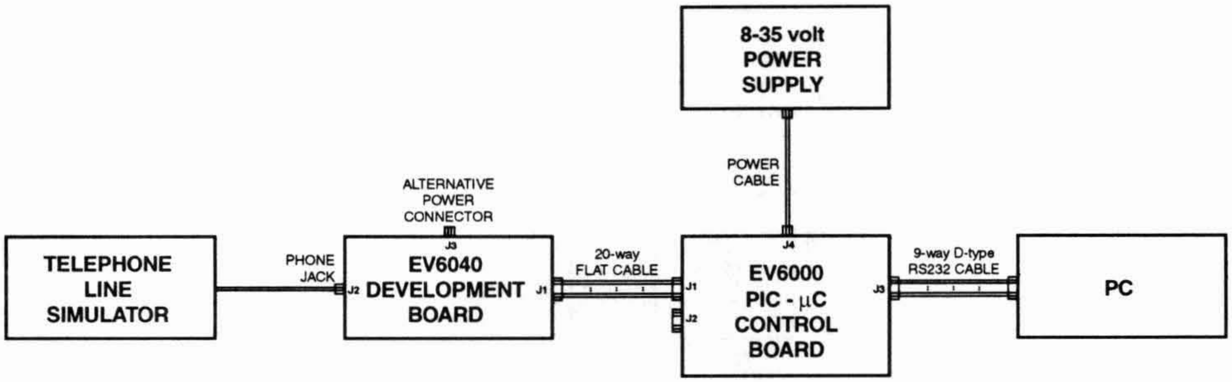
PRODUCT INFORMATION

EV6040 Development Kit for the MX604 and MX614

FEATURES

- **For MX604 (V.23) and MX614 (Bell 202) 1200bps FSK Modems**
- **Reconfigurable Board with Interface to Optional µC Board**
- **Parallel Phone Detector**
- **Easy Access to Test Points**
- **User's Prototyping Area**
- **Space for Optional and Telco-Specific Components**
- **8.0V - 35.0V Single Power Supply Operation**



The EV6040 Development Kit consists of a single board containing an MX604 or an MX614 and the associated line interface components. The EV6040 communicates with the MX-COM µC board (EV6000) or with the user's own µC board. Each of which can demonstrate the use of the MX604/MX614 in various telecommunications applications, when user programmed. The EV6040 board is powered from a single 8 - 35V DC power supply. An on-board regulator sets the 3.3V or 5.0V requirement. LEDs indicate data, control and interrupt line status (DET, $\overline{\text{RDY}}$, RXEQ, M0, and M1) and the MX604 may be driven from an external clock, or from its own crystal oscillator. Easily accessible test points are provided for the monitoring of test signals. A socket is provided for the easy replacement of the MX604/MX614. Additional user prototyping area is also provided on the EV6040 for user added components that are telco-specific (line impedance, line protection, ac-load, wetting pulse, etc.).

On-board relays may be used to implement a wetting pulse, to place an AC or DC load on the line, and to interface the line to a transformer/op-amp hybrid for voice communications. A mutable voice input and a µC controllable or pre-settable DTMF generator are provided. Operation of the relays, the mutable voice-input, and the DTMF generator are indicated by LEDs. The parallel phone detector may be used in adjunct box emulation. The MX604/MX614 supply current may be measured by removing a jumper.

The EV6040 provides an excellent demonstration and prototyping platform for MX604 and MX614 based projects.

MX•COM,INC. MiXed Signal ICs

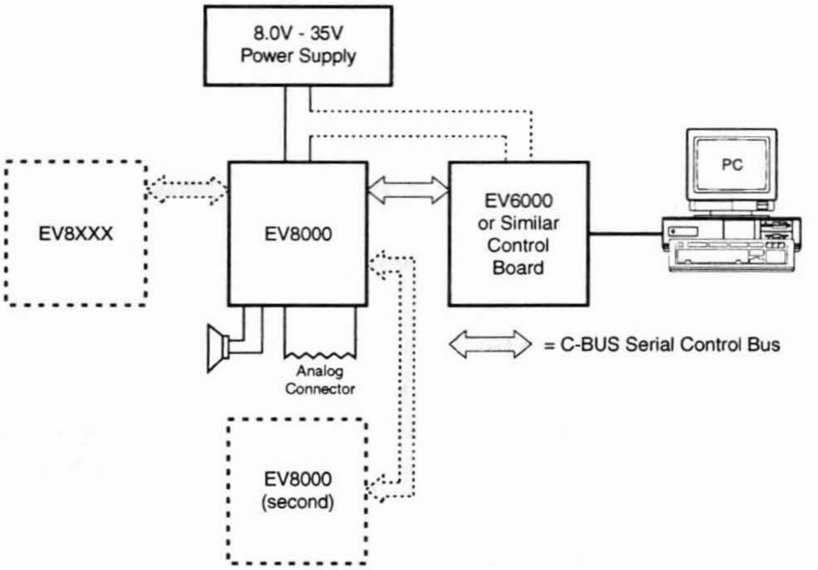
PRODUCT INFROMATION

EV8000

Development Kit for the MX818, MX828, and MX829

FEATURES

- **For MX818 (CTCSS), MX828 (CTCSS, DCS, SelCall), and MX829 (1200/2400bps MSK Modem, Tx/Rx Audio Processor, DTMF Encoder) Product Evaluation**
- **μC Board Interface**
- **On-Board Microphone**
- **On-Board Regulator**
- **Supplied PC Software provides point and click control of device operation.**
- **Easy Access Test Points**
- **8.0V - 35.0V Single Power Supply Operation**
- **8Ω Speaker Output**
- **Sockets for Discrete External Components**
- **User's Prototype Area**



The EV8000 Development Kit consists of a single board containing an MX828 and an MX829. An MX818 is also provided which can be fitted in place of the MX828.

The EV8000 board is powered by a single 8 - 35V DC power supply. An on-board regulator is user configured for 3.3V or 5.0V device operation. Status of the MX829 carrier detect output and the MX828 comparator output are indicated by LEDs and are hardware accessible via a connector. An on-board microphone and 8Ω speaker output are also provided.

The MX828/818 and MX829 may be driven from a common external clock or from a common crystal oscillator. The supply current of either target device may be easily measured. Accessible test points are provided for the monitoring of test signals and prototyping space has been provided.

Serial control bus (C-BUS) signals are made accessible at three connector areas. Two include both C-BUS and MX828/MX829 I/O signals to support experiments for both Tx and Rx ends of a system. The third area includes only C-BUS signals to support daisy chaining of other C-BUS compatible equipment as found in complete system designs.

The EV8000 provides an excellent demonstration and prototyping platform for MX818, MX828, and MX829 based projects.

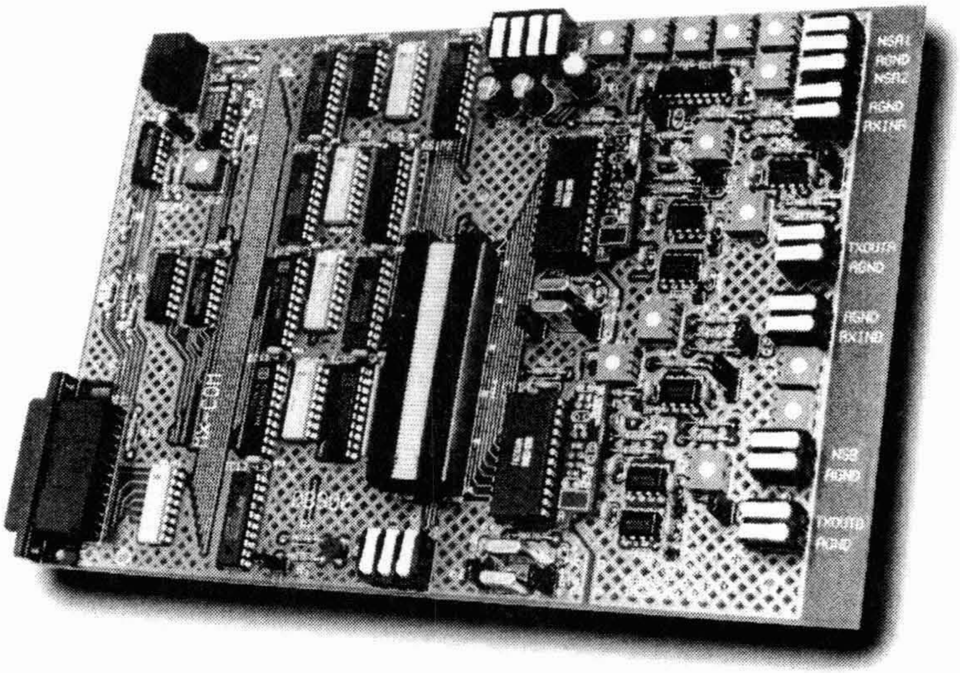
MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

EV9000 Development Kit for the MX909A, MX919B, and MX929B

FEATURES

- **Exercise all modem functions with supplied PC software virtual interface**
- **Supports Narrow Bandwidth GMSK and 4-level FSK modulation**
- **Two baseband modem circuits provide simultaneous Rx and Tx functions**
- **Hardware interfaces support integration into product prototypes**
- **Includes MX909A, MX919B, and MX929B components**
- **User configurable to support different modems and data rates**
- **Adjustable gain, offset, and noise injection ports for error rate testing**
- **Test Points for probe access**



The EV9000 Modem Development Kit is a complete test platform to demonstrate and test the MX909A, MX919B, and MX929B components. These parts include Gaussian filtered minimum shift keying (GMSK) or four level frequency shift keying (4 Level FSK) modems which execute a rich set of communication protocol tasks to maximize performance and minimize end product power consumption and cost. Automated modem functions include: bit and frame synch; forward error correction (FEC); cyclic redundancy checking (CRC); header, intermediate, and last block Tx & Rx; data interleaving for FEC enhancement; and support for protocols such as Mobitex™, RD-LAP™, and ARDIS^{SM}.

The EV9000 Modem Development Kit includes a pair of complete baseband modem circuits; one pair each of the MX909A, MX919B, and MX929B components; PC software; and a hardware interface to connect to the parallel port of your Microsoft Windows™ compatible personal computer. Modem circuits can be easily configured for user selected baud rates and operated using various automated test sequences. Signal injection circuits for each of the two channels include gain and offset adjustments to create a variety of test conditions. Modem circuits can be connected to end system designs via an exposed hardware interface.

GLOSSARY

ADPCM - Adaptive Differential Pulse Code Modulation, a voice CODEC (see CODEC) algorithm popular in telephony applications to carry a voice in a 32kbps data stream.

AGC - Automatic Gain Control, a circuit that adapts to maintain nearly the same output signal level when either low or high input signal levels are applied.

AMPS/NAMPS - Advanced Mobile Phone System is an analog cellular telephone system used in the United States. NAMPS (Narrow AMPS) uses FDMA technique to derive three voice channels from one AMPS channel.

ANI - Automatic Number Identification: Identification of the transmitting party by a pre-assigned number.

ANSI - American National Standards Institute: A voluntary organization in the United States that coordinates standards and their development.

ARDIS™ - An FM radio data system that operates at 9.6kbps and 19.2kbps using four level coded, root raised cosine filtered processing of the digital data stream to enhance bandwidth efficiency. Trademarked by Motorola.

Asynchronous Transmission - A mode of data transmission in which each data bit is not accompanied by a clock signal that indicates the validity of data. Data are sent in groups of a pre-specified length with start and stop bit indicators at the beginning and end of each group with a relatively close, but not identical or synchronized, bit time duration used by both transmitter and receiver.

Bandwidth - The range of those frequencies (maximum-minimum) which carry the significant energy of a signal in a system. The wider the bandwidth of a signal, the higher information carrying capacity (i.e. data rate) it can support for a given incident noise level.

Baseband – Signals whose maximum and minimum frequency components are at or near 0Hz. Baseband signals are typically modulated to much higher frequencies (e.g. radio frequency) after which they can then be better transmitted and propagate through the air or combined , with low interference, on a common medium e.g. coaxial cable.

Baud - A signaling symbol that carries information. Some signaling schemes can carry more than one bit of information per symbol (or baud).

BCD - Binary Coded Decimal: A binary (1,0) numbering system in which the digits 0 through 9 are represented by four bits.

BER - Bit Error Rate: A ratio of the number of transmitted bits that are incorrectly received to the number that are received in total.

Bit Rate - The speed at which bits are transmitted over a data channel, given in bits per second (bps) or thousand bits per second (kbps). In many systems, to improve error resilience and other characteristics of a communication link, the intended data is combined with additional data before transmission over a different medium (e.g. via radio) occurs. In such a case, a distinction is made between the user (original) data and the transmitted (over the air) data.

Carrier - A carrier is a wave capable of being modulated by an information-carrying signal. The use of multiple carriers permits multiple voice frequency signals in the same transmission, as in frequency division multiplexing.

C-BUS - MX-COM's serial control bus used to communicate digital information between a µP or µC and a peripheral IC such as the MX803A, MX818, and MX829. The use of such a serial bus requires far fewer signal pins on an IC and so reduces device size and associated printed circuit board area.

CCIR - International Radio Consultative Committee, a subsidiary organization of the International Telegraphic Union dealing in radio standards.

CCITT - The Consultative Committee on International Telegraph and Telephone is an International Telecommunications Standard Agency. It has been renamed ITU-T.

CD – Carrier Detect: A logic signal that indicates when a modulated signal's (e.g. MSK or RF modulated) carrier is detected.

CDMA - Code Division Multiple Access, a technique for differently coding separate data streams and transmitting them at the same time so they interfere with each other. CDMA receivers make use of the specific coding algorithm to select the one signal of interest from the others. CDMA permits multiple users to successfully simultaneously share a common medium even though, to a significant extent, they generate significant interference.

CDPD - Cellular Digital Packet Data: An industry standard for data transmission. CDPD utilizes analog cellular networks already in place in the United States and Canada to provide 2-way data communications for users of devices such as laptops and PDAs.

Channel, Voice Grade - A signal channel or path which supports a signal frequency range of about 300Hz to 3400Hz and so is suitable for transmission of data or speech in analog form.

CID - Caller Identification or Calling Line Identifier (Type 1): The system that indicates a telephone caller's telephone number before an incoming call is answered.

CIDCW - Caller Identification on Call Waiting or Calling Line Identifier on Call Waiting (Type 2): The system that indicates a telephone caller's telephone number both before an incoming call is answered and during a call when a second incoming call is received.

C-MSG - 'C-Message Weighting': Represents frequency response of typical United States telephone wireline.

CMOS - Complementary Metal-Oxide Semiconductor (an integrated semiconductor manufacturing process). MXCOM uses both Metal-gate CMOS and Silicon-gate CMOS processes.

CODEC - A single device comprising both Encoder and a Decoder. Often used to describe a device that encodes or digitizes a voice signal into digital form and decodes the digital signals produced by this method back into a close rendition of the original analog form.

Compandor - Acronym for Compressor-Expander, a circuit that compresses the dynamic range of an input signal and expands it almost back to its original form on the output. The compression process increases the signal level of weaker signals and so improves their resistance to background noise levels that are added during transmission. Expansion of a compressed signal reduces the weaker signal components back to their original weak levels and, in so doing, further decreases the levels of added background noise to relatively lower levels. In this way, companding achieves improvements of signal to noise level.

Concatenation - Combining multiple data packets or frames in a contiguous series, that is, one immediately following another.

CPFSK - Continuous Phase Frequency Shift Keying

CPM - Continuous Phase Modulation

Crosstalk - Undesired crossover of voice transmissions from one circuit to another.

CS - Carrier Sense: A logic signal supplied by the radio when an RF carrier is detected.

CTCSS - Continuous Tone-Controlled Squelch System: A type of tone decoding used in 2-way radio systems in which a sub-audible tone, taken from a field of 39 in the 67Hz to 250Hz range, is multiplexed continuously with speech to engage repeaters and allocate traffic among talk groups on shared channels. Trademarked by Motorola as Private Line or PL.

CVSD - Continuously Variable Slope Delta Modulation: A method by which a voice signal is digitized for transmission, and then changed back to an analog voice signal for reception.

dB - decibel; dimensionless logarithmic unit that is commonly used to express amplifier gain.

dBm - decibel referenced to 1mW; output power of a signal referenced to an input signal of 1mW.

dBmO - output power, referenced to dBm, with no input signal.

DCE - Data Communications Equipment or Data Circuit-Terminating Equipment: This equipment functions to establish and maintain a connection, and provides signal conversion between a terminal and data or telephone line.

DCS/CDCSS - Digital Coded Squelch: Similar to CTCSS in function but utilizes 83 digital tones to control the same operations. Trademarked by Motorola as Digital Private Line or DPL.

DPCM - Differential Pulse Code Modulation

DPM - Differential Phase Modulation

DQPSK - Differential Quadrature Phase Shift Keying:

$$\frac{\pi}{4}\text{DQPSK} \Rightarrow \text{Shift} = \frac{\pi}{4}$$

DSP - Digital Signal Processing

DTMF - Dual Tone Multi-Frequency: A telephone signaling system employing four tones from a low group and three or four tones from a high group comprising twelve to sixteen different unique tone pairs. Radio applications of DTMF should avoid "twist" (differences in level between tone pairs) and time-limit digits to prevent signaling errors caused by fades.

DVSR - Data/Voice Storage and Retrieval. Trademarked by MXCOM as Radio MailVox.

ECPA - Electronic Communications Privacy Act of 1986: This amendment to Section 2510 of title 18, United States Code, establishes the illegality of intercepting protected (i.e. scrambled) communications.

EIA - Electronics Industry Association: A United States manufacturer's group which, as part of its function, sets and publishes electronics standards.

Eye Pattern / Eye Diagram - An oscilloscope display of the detector voltage waveform in a modem. The openness of an eye gives a representation of the bit error rate (the more open, the less distortion).

FDMA - Frequency Division Multiple Access

FEC - Forward Error Correction

FFSK - Fast Frequency Shift Keying: See MSK

FSK - Frequency Shift Keying: a form of frequency modulation used to transmit two states of a signal as two separate frequencies. FSK is characterized by frequency spacing of 1

Full-Duplex - Simultaneous two-way communication

Gaussian Filter - A filter that has an impulse response similar to the symmetrical bell shape of a Gaussian curve (normal distribution)

GFSK - Gaussian Filtered Frequency Shift Keying: (mod index $\neq 0.5$)

GMSK - Gaussian Minimum Shift Keying: A type of FSK that uses pre-modulation Gaussian filtering to achieve high data rates in an FM communications channel bandwidth.

GPS - Global Positioning System

Half-Duplex - Communications in which both transmit and receive occur , but not at the same time.

HSC - Hexadecimal Sequential Coding: A tone signaling protocol comprising 16 tone states. Ten tone states represent decimals 0-9, a NOTONE, a Repeat tone, a Group tone, an address/DATA frame delineator, plus Reset and control, totaling 16 tone-coded logic states. HSC operation is predicated on a decoding technique able to detect tones in random order. These must be contained within a frame preceded and concluded by NOTONE.

HSC Tonesets -

HSC-A: USA or Metropage™. A Motorola radio Paging system employing sequential tones comprising ten decimal and two special function tones ("R" for repeat and "X" as an alternate address) and NOTONE in a predictive code format.

HSC-C: CCIR toneset. A toneset developed by the International Radio Consultative Committee.

HSC-E: EEA toneset. An EEA (UK) variation of the CCIR HSC toneset, in which the lowest frequency tone is 930Hz and the highest is 2247Hz. Duration is 40ms

HSC-Z: ZVEI German HSC toneset

HSC-ZS: SZVEI or Suppressed ZVEI HSC toneset

IEEE - The Institute of Electrical and Electronic Engineers: One of the functions of this association of engineers is to publish standards defining technical terms.

ITU-T - International Telegraphic Union - Telecommunications (includes the CCITT and CCIR) is an international telecommunications standards agency.

Jitter - Small, abrupt, spurious variations in a waveform due to time, amplitude, frequency or phase

LMR - Land Mobile Radio system

LSI - Large Scale Integration

LTR™ - EF Johnson trademarked trunking system.

MOBITEX - A data transmission protocol developed by Swedish Telecom.

MODEM - Modulator/Demodulator: This is a type of DCE that connects data terminal equipment to a communications line/channel. It converts data to and from the signal form needed for the communication channel.

Modulation Index – In general, it is the ratio of the peak deviation to the modulating frequency. In digital frequency modulation systems, it is the ratio of the difference between mark and space frequencies to the data rate.

$$\text{modulation index} = \frac{f_{\text{MARK}} - f_{\text{SPACE}}}{B}$$

$$\text{where} \quad B = \frac{1}{T_{\text{BIT}}}$$

$$\text{and} \quad T_{\text{BIT}} = \text{Duration of a single data bit}$$

Modulation - The process of translating the frequency spectrum of a message signal, usually accomplished by multiplying the message signal by a sinusoidal carrier signal.

Monolithic - Constructed from a single crystal or piece of material

MSK - Minimum Shift Keying: Continuous phase FSK modulation (also called FFSK) used to transmit two states of a signal as two separate frequencies. The separation of these frequencies is ½ the data rate (i.e. modulation index = 0.5).

Multiplexing - Combining multiple signals for transmission as a group over a single transmission facility.

NMT - Nordic Mobile Telephone: A cellular communication systems used primarily in Europe

PABX - Private Automatic Branch Exchange

PAMR - Public Access Mobile Radio

PCM - Pulse Code Modulation: A process in which an analog signal is sampled and converted to a binary code for transmission

PCMCIA (PC CARD) - Personal Computer Memory Card International Association: This association defines and promotes an interchangeable standard for PC memory and expansion cards. The PCMCIA standard applies to 68-pin I/O or interchange type cards.

PCS - Personal Communications Services

PDA - Personal Digital Assistant: A handheld computer that provides the functions of a notepad or messagepad. PDAs often include data transmission capabilities

PL - Private Line: A Motorola trademarked name for CTCSS

PMR - Public Mobile Radio

PSK - Phase Shift Keying: A form of phase modulation requiring coherent detection. The most straightforward type of PSK shifts the carrier by 0° or 180°.

Psophometric - A weighting curve used to represent the energy density of speech.

PTM/PTL - 'Push To Monitor' or 'Push To Listen': This is a control on two-way portable and mobile radios that allows channel monitoring.

PTT - 'Push To Talk': This is a control on two-way portable and mobile radios that enables transmission.

PSTN - Public Switched Telephone Network:

***Pvt*SQUELCH™** - MX•COM's trademarked combination of CTCSS and voice inversion to provide voice privacy.

QAM - Quadrature Amplitude Modulation: A hybrid amplitude/phase modulation technique that allows the transmission of multiple bits of information during a signaling interval, and requires less bandwidth than normal amplitude or phase modulation techniques.

QPSK - Quadrature Phase Shift Keying. Change in data indicated by 90° phase shift.

Quick Call II™ - A Motorola trademarked 2-Tone sequential signaling format comprising 80 tones arranged in eight tone groups

R2000 - This is a trunked communication system used in France.

RD-LAP™ - An FM radio data protocol that operates at 9.6kbps and 19.2kbps. Trademarked by Motorola.

Repeater - a device used as an intermediate point in a communications system to receive and retransmit signals, often for the purpose of extending range.

SAT - Supervisory Audio Tone used in cellular systems.

SIGATE - Silicon Gate: A CMOS process used in manufacturing ICs that is smaller and more modern than metal gate.

Simplex - A circuit which can communicate information in one direction only.

SINAD - A ratio of the total output power to the power of noise plus distortion only:

$$\frac{\text{signal} + \text{noise} + \text{distortion}}{\text{noise} + \text{distortion}}$$

SIT - Special Information Tones

SMD/SMT - Surface Mount Device / Surface Mount Technology

SMR - Specialized Mobile Radio

SS - Spread Spectrum: The spreading of a signal over a wider bandwidth than the minimum required for transmission of the information

Synchronous Transmission - A type of data transmission in which the sending and receiving ends operate continuously at the same frequency and in phase

TACS/ETACS - Total Access Communications Systems is a cellular system used in the United Kingdom. ETACS is used in Europe and Japan

TDMA - Time Division Multiple Access

TIA - Telecommunications Industry Association: A United States manufacturer's group which, as part of its function, sets and publishes telecommunications standards.

Type 99™ - A General Electric trademarked 2-Tone sequential format comprising 30 tones.

Trunking - A system sharing communication channels.

UART - Universal Asynchronous Receiver Transmitter.

VCO - Voltage Controlled Oscillator

VLSI - Very Large Scale Integration

VOGAD - Voltage Operated Gain Adjusting Device: Similar in concept to an AGC (Automatic Gain Controlled) amplifier, used to ensure full modulation of all speech levels.

VOX - Voice Operated Switching

VSB - Variable Split Band: A type of high-level analog scrambling which splits and inverts the voice band. VSB is utilized in MX-COM's IC and board level products.

PACKAGE INFORMATION

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Summary of Available Package styles

Consumer Suffix	MX-COM Suffix								
Old	New & CMX	1st Letter	2nd Letter	3rd Letter	# pins	Description	Pin Pitch mil(mm)	Stand-off Height(max) mil(mm)	Body Width Mil(mm)	Material
P	P1 P2 P3	P			8, 14 16	Plastic Dual In Line(PDIP)	100(2.54)		300(7.62)	Plastic
P	P6	P			22	Plastic Dual In Line(PDIP)	100(2.54)		400(10.16)	Plastic
P	P4 N/A P5	P			24 28 40	Plastic Dual In Line(PDIP)	100(2.54)		600(15.24)	Plastic
J	J1 J2	J			14 16	Ceramic Dual In Line package (CDIP)	100(2.54)		300(7.62)	Ceramic
J	J3	J			22	Ceramic Dual In Line package (CDIP)	100(2.54)		400(10.16)	Ceramic
J	J4 J5	J			24 28	Ceramic Dual In Line package (CDIP)	100(2.54)		600(15.24)	Ceramic
DW	D4 D3 D2 D1	D	W		16 20 24 28	wide-body Small Outline Package (SOIC)	50(1.27)	105(2.67)	300(7.59)	Plastic
	D5	D	S		24	Small Shrink Outline Package (SSOP)	25.6(0.65)	79(2.0)	209(5.3)	Plastic
	D6					Small Shrink Outline Package (SSOP)	25.6(0.65)	79(2.0)	209(5.3)	Plastic
LS	L2	L	H		24	Plastic Leaded Chip Carrier (PLCC) Hook	50(1.27)	146(10.4)	400(10.16)	Plastic
	L6	L	H		44	Plastic Leaded Chip Carrier (PLCC) Hook	50(1.27)			Plastic
LH	L3	L	H	8	28	Plastic Leaded Chip Carrier (PLCC) Hook	50(1.27)	180(4.57)	450(11.3)	Plastic
LG	L1	L	G		24	Plastic Leaded Chip Carrier with GULLWING leads	50(1.27)	98(2.5)	400(10.16)	Plastic
L	L5	N/A			24	Plastic Leaded Chip Carrier with STRAIGHT leads				
	N/A	K			24	Ceramic LeadLess Chip Carrier (CLLCC))	50(1.27)	88(2.23)	400(10.16)	Ceramic
	N/A	K			28	Ceramic LeadLess Chip Carrier (CLLCC)	50(1.27)	70(2.23)	465(12.06)	Ceramic
	M1	N/A			28	Ceramic Leaded Chip Carrier (CLCC) - Hook				

Consumer Suffix		**MX-COM Suffix**			**Summary of Available Package styles**					
Old	New & CMX	1st Letter	2nd Letter	3rd Letter	# pins	Description	Pin Pitch mil(mm)	Stand-off Height(max) mil(mm)	Body Width Mil(mm)	Material
	N/A	K			44	Ceramic LeadLess Chip Carrier (CLLCC)	50(1.27)	70(1.77)	650(16.51)	Ceramic
	E1				28	Thin Narrow body shrink Small Outline package (TSSOP)	25.6(0.65)	47(1.19)	175(4.44)	Plastic
	E2	T	N		24	Thin Narrow body shrink Small Outline package (TSSOP)	25.6(0.65)	47(1.19)	175(4.44)	Plastic
	E3				20	Thin Narrow body shrink Small Outline package (TSSOP)	25.6(0.65)	47(1.19)	175(4.44)	Plastic
	E4				16	Thin Narrow body shrink Small Outline package (TSSOP)	25.6(0.65)	47(1.19)	175(4.44)	Plastic
	L4	T	G		48	Thin Quad Flat Pack with gullwing leads TQFP)	20(.51)	63(1.6)	275(6.98)	Plastic
	L7				44	Quad Flat Pack with gullwing leads (QFP)	31(0.80)	63(1.6)	394(10.00)	Plastic
		S				Bare Die; no package				

NOTE: The letters A, B, and C following a product number refer to the product revision.

1 PURPOSE/SCOPE

1.1 This specification relates to the tape and reel packaging of integrated circuits for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchasher to use the product.

2 APPLICABLE DOCUMENTS

2.1 EIA-481: Revision A Taping of Surface Mount Components for Automatic Placement.

3 DEFINITIONS

Note: For 3.1 -3.13, refer to Figure 1 and for 3.14 - 3.18, refer to Figure 4.

3.1 W: Carrier Tape Width

3.2 t: Carrier Tape Thickness

3.3 P_O: Pitch of Sprocket Holes

3.4 D: Diameter of Sprocket Holes

3.5 E: Distance from center of sprocket holes to edge of carrier tape

3.6 F: Distance from center of sprocket hole to center of pocket

3.7 P_2: Distance from center of pocket to center of divider

3.8 A_O: Inside length of pocket

3.9 B_O: Inside width of pocket

3.10 Ko: Depth of pocket cavity

3.11 P: Pitch of component pockets (center to center)

3.12 B_1: Outside width dimension of pocket

3.13 D_1: Diameter of pocket center holes

3.14 G: Inside width of reel

3.15 T: Outside width of reel

3.16 C: Sprocket hole diameter of reel

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3.17 N: Hub diameter of reel

3.18 A: Diameter of reel

3.19 R: Minimum hub diameter (see Fig.5) allowed

3.20 LG: 24 lead gull wing PLCC

3.21 LH: 24 lead J-lead PLCC

3.22 DW-16: 16 lead SOIC

3.23 DW-24: 24 lead SOIC

3.24 TN: Thin Shrunk Small Outline Package(TSSOP)

3.25 D3-20: 20 lead SOIC

3.26 DS-24: Shrunk Small Outline Package(SSOP)

4 TAPE AND REEL CHARACTERISTICS

4.1 Dimensions (all dimensions in Millimeters)

Table 1: Carrier Tape Dimensions(reference Figure 1)

Dim	LG	LH	DW-16	DW-24	TN-24	D3-20	DS-24
W	24 ± 0.3	24 ± 0.3	16 ± 0.3	24 ± 0.3	16 ± 0.3	24 ± 0.3	16 ± 0.3
t(max)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
P_o	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1
D	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5+0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0
E	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1
F	11.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1
P_2	2.0 ± 0.1	2.0± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1
A_o	15.8 ± 0.1	11.5 ± 0.1	10.9 ± 0.1	10.9 ± 0.1	6.95 ± 0.1	10.9 ± 0.1	8.2±0.1
B_o	15.8 ± 0.1	11.5 ± 0.1	10.7 ± 0.1	16 ± 0.1	8.3 ± 0.1	13.3 ±0.1	8.6±0.1
Ko	2.9 ± 0.1	4.1 ± 0.1	3.0 ± 0.1	3.0 ± 0.1	1.6 ± 0.1	3.2 ± 0.1	3.0 ± 0.1
P	20 ± 0.1	16 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1
$B_{1(max)}$	16.5±0.1	20.1	12.1	20.1	9 ± 0.1	20.1	9 ± 0.1

Dim	LG	LH	DW-16	DW-24	TN-24	D3-20	DS-24
K_1	N/A	N/A	N/A	N/A	1.2±0.1	2.7±0.1	2.3±0.1
D_1	1.5 min	1.5 min	1.6+1.0/-0.1	1.55 +1.0/-0.05	1.6+1.0/-0.1	1.5 min	1.5 min

Table 2: Reel Dimensions (reference Figure 4)

Dim	LG	LH	DW-16	DW-24	TN-24	D3-20	DS-24
A(max)	360	360	360	360	180	360	360
C	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2
N R(min per EIA)	50 (50)	80 (50)	80 (40)	80 (50)	50 (40)	80 (50)	80 (40)
G	24.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0
T	30.4	30.4	22.4	30.4	22.4	30.4	22.4

4.2 Components on a reel

	360MM DIAMETER	180MM DIAMETER
LG	700	
LH	700	
DW-16	1200	
DW-24	1200	
D3-20	1200	
DS-24		1000
TN-24		1000

4.3 Polarity and Orientation of Components in Carrier Tape

4.3.1 All components are placed such that pin-1 is adjacent to the sprocket holes, as shown in Figure 6.

4.3.2 The mounting side of the component is oriented to the bottom side of the carrier tape as shown in Figure 2.

4.4 Placing of Components in Carrier Tape

4.4.1 The Cover Tape does not cover the sprocket holes

4.4.2 The tapes in adjacent layers do not stick together in the finished reel.

4.4.3 The adhesive of the cover tape does not affect the mechanical and electrical characteristics and marking of the components.

4.4.4 Components do not stick to either the carrier tape or the cover tape.

4.4.5 The tapes will withstand storage without danger of emitting any vapors which might impair soldering or chemically deteriorate the components or component leads.

4.4.6 When the tape is bent to the minimum radius of R mm, as shown in Figure 5 and Table 2, the tape is not damaged and the components remain in their position and orientation in the tape.

4.4.7 The carrier tape is conductive.

4.4.8 The cover tape is antistatic.

4.4.9 The peel strength of the cover tape is 60-90 grams, measured at an angle of 175° to 180° and a peel speed of 184 mm/minute, with respect to the carrier tape along its longitudinal axis.

4.5 Packaging

4.5.1 At the start of each carrier tape, a minimum of 75 empty compartments are passed before placing components into the carrier tape compartments.

4.5.2 At the end of the tape (carrier plus sealed cover), there is a trailer tape which is a minimum of 40 empty components.

4.5.3 The tape releases from the reel hub as the last portion of the carrier tape unwinds from the reel.

4.5.4 The tape is prevented from unreeling by winding an additional strip of cover tape around the outside of the reel between 2 and 3 times. Secure the tape on the reel with a small tab of self-adhesive tape.

4.5.5 All reels display the following information:

MX-COM or Customer Specific device type
Quantity on reel
Date Code
Static Sensitive warning label
Barcode Label per customer request

4.6 Storage Conditions and Shelf Life

4.6.1 Ideal storage conditions are 15°C to 20°C with a relative humidity of 60-70%.

4.6.2 Maximum estimated shelf life when stored at ideal conditions is 18 months.

PACKAGE INFORMATION
TAPE and REEL SPECIFICATIONS

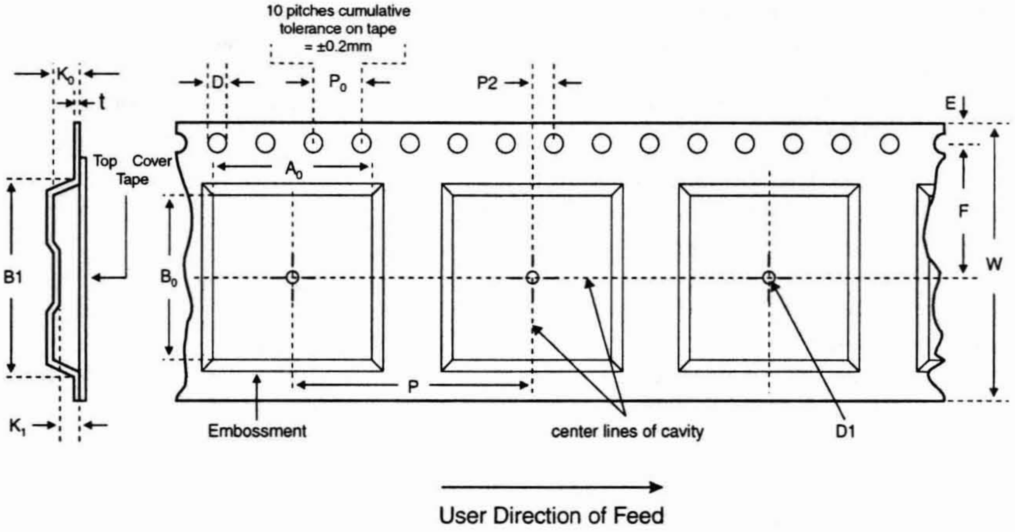

10 pitches cumulative
tolerance on tape
= ±0.2mm
K0
t
D
P0
P2
E
Top Cover Tape
A0
B1
B0
F
W
P
K1
Embossment
center lines of cavity
D1
User Direction of Feed

Figure 1. Embossed Carrier Dimensions

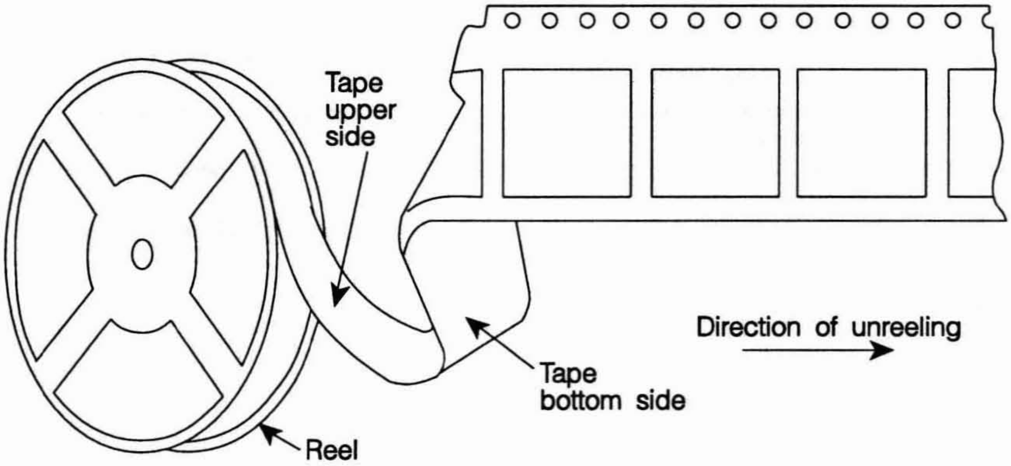

Tape
upper
side
Direction of unreeling
Tape
bottom side
Reel

Figure 2. Tape Top and Bottom Orientation

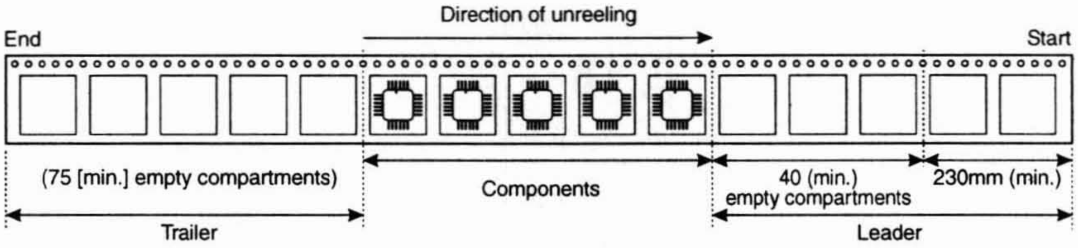
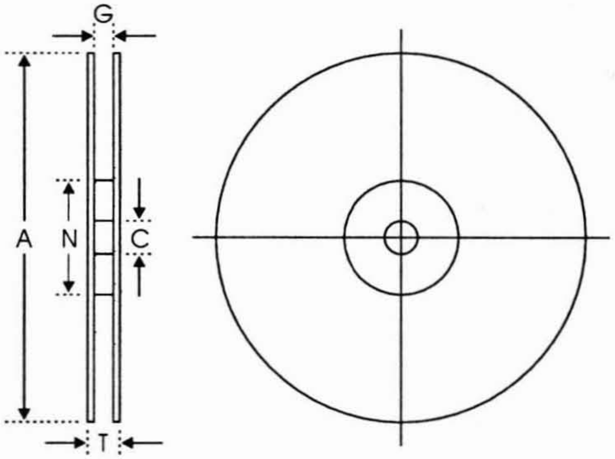

Direction of unreeling
End
Start
(75 [min.] empty compartments)
Components
40 (min.)
empty compartments
230mm (min.)
Trailer
Leader

Figure 3. Layout of Tape



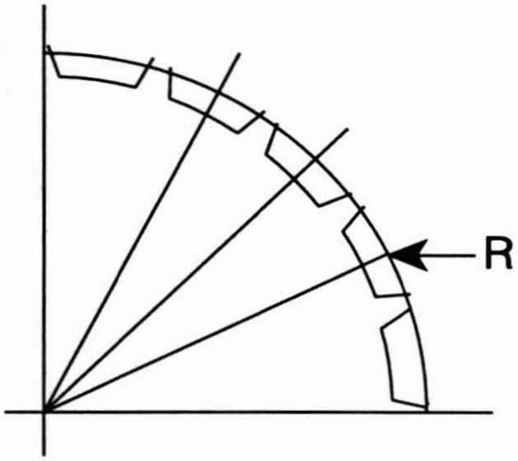
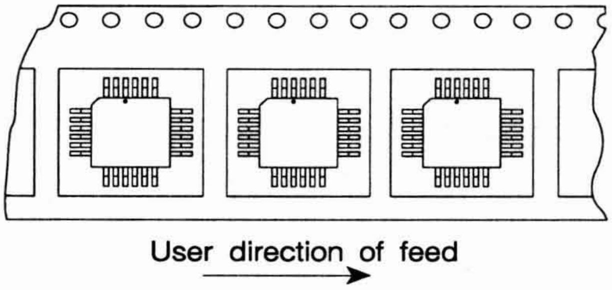


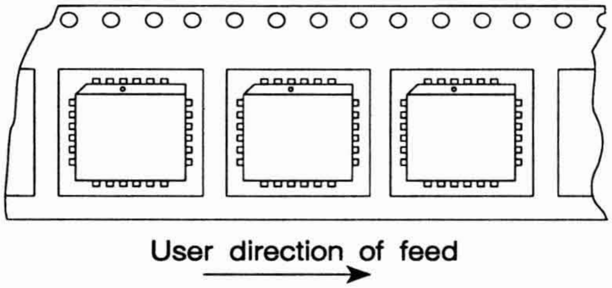
Figure 4. Reel Dimensions

Figure 5. Minimum Radius = 50mm

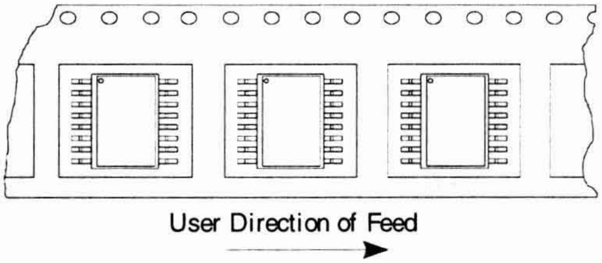
LG Package


User direction of feed

LH Package


User direction of feed

DW Package


User Direction of Feed

Fgure 6. Component Orientation

Package Style	Quantity
LH	45
LH8	38
DS-24	59
DS-28	47
DW-14	46
DW-16	46
DW-20	38
DW-24	30
J-14	25
J-16	25
J-22	18
J-24	15
J-40	8
P-14	25
P-16	25
P-22	18
P-24	15
P-40	8
TN	62

MX•COM, INC.

COMMUNICATION ICs

Wireless Modems
Wireline Modems
Telecom Signal Encoders/Decoders
Tone Signal Encoders/Decoders
CVSD Voice CODECs
Voice Scramblers

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